Examination in Integrated A/D and D/A Converters, ETI220

14.00-19.00, Friday, August 27, 2010

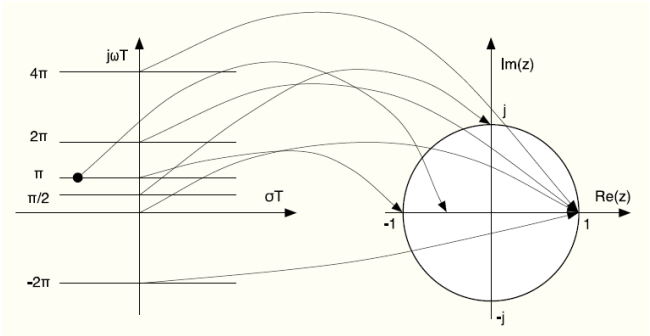
I. Basic questions about converters

a) If we sample a time span of 10ms and obtain 2^{15} samples, what is the highest frequency we can resolve?

b) Explain what we intend with spectrum folding, and why it is a major concern in convert design. Can it also be used intentionally?

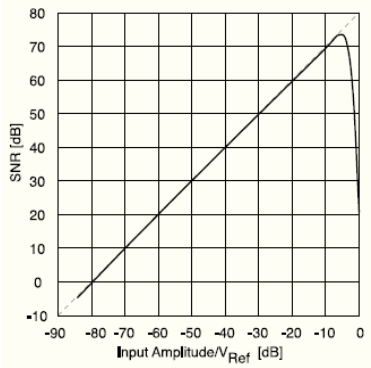
c) What are the major noise sources limiting the SNR of an A/D converter?

d) What does this figure describe?



e) Looking at the fft response of an A/D converter, how can we determine whether the energy present in a given bin is due to noise or distortion?

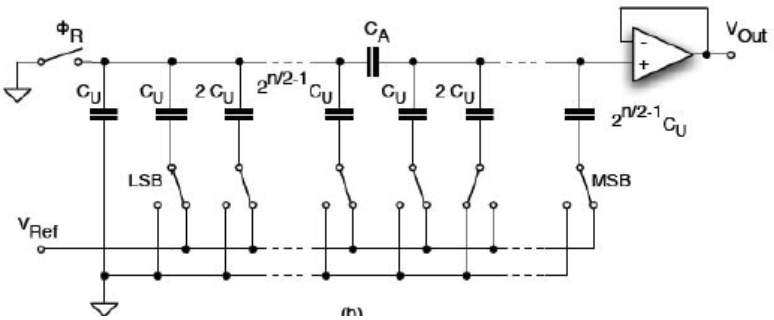
f) What kind of converter typically displays this kind of SNR vs. the amplitude of the input signal?



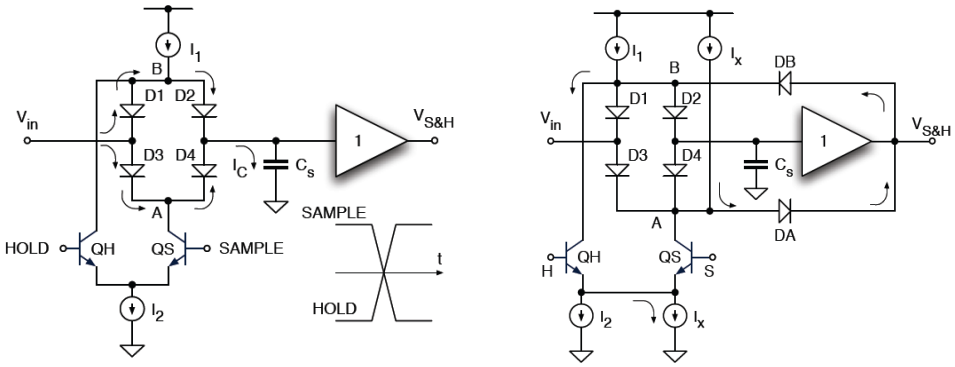
II. Specific questions about converters

a) Describe a pipeline A/D converter, and explain in detail how a 1.5b pipeline A/D converter stage works.

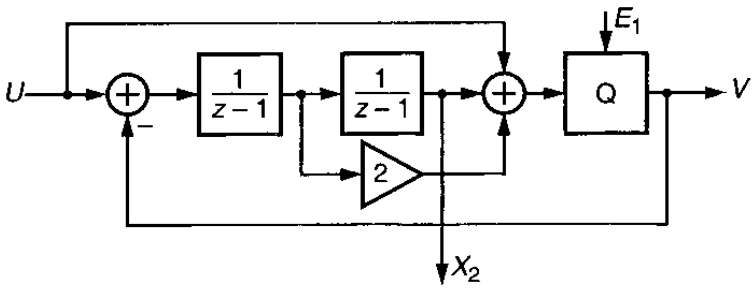
b) What kind of converter is this? Explain how it works and derive its transfer function. Explain the role of C_A, and why C_A can be regarded as a critical component.



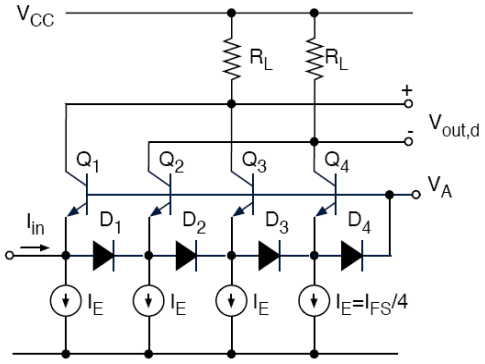
c) A diode-bridge is shown below on the left. Explain how it works. On the right we see an improved version – explain how it works, and why it is an improvement.



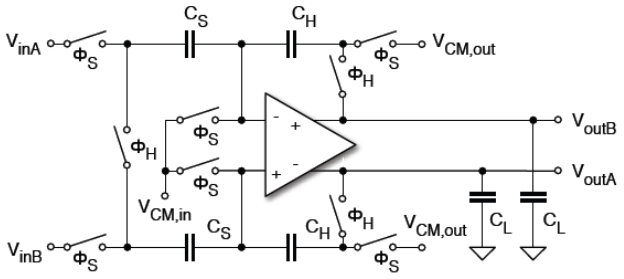
d) Below you see a Delta-Sigma modulator. Find the signal transfer function STF=V/U, the quantization-noise transfer function NTF=V/E, and show that X_2 is independent of U. What is the order of this modulator?

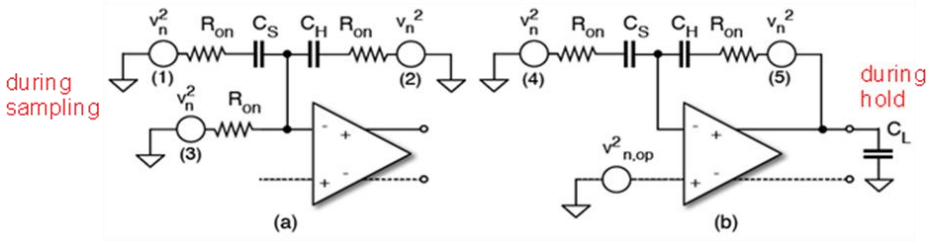


e) Explain what conversion is implemented by the circuit below, and how it works.

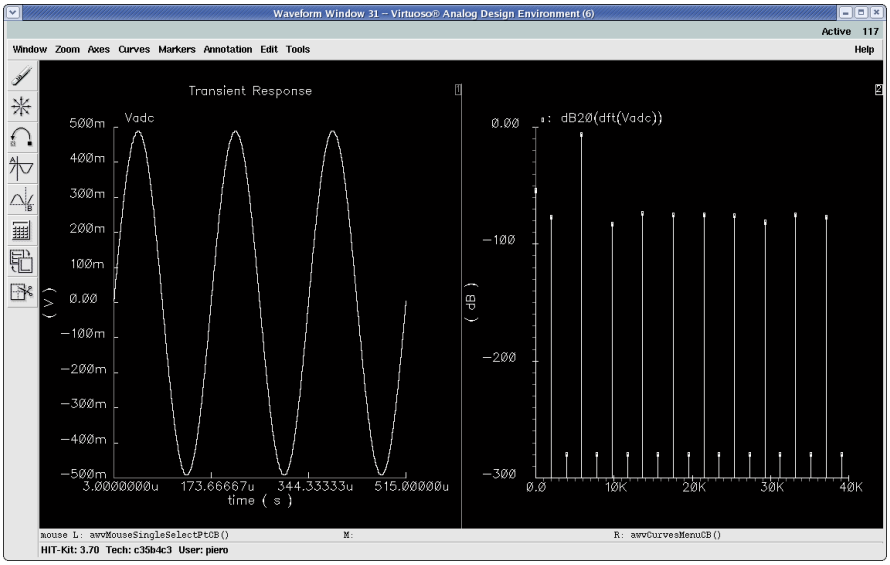


f) Below you see a charge-transfer Sample & Hold circuit, with the (single-ended) circuits for noise analysis during Sample and during Hold. Assume that the amplifier noise is $v_{n,op}^2 = 4kT\gamma'/g_m$, the amplifier gain $A = \omega_T/s$ and $\omega_T = g_m/C_L$. Find the total noise at the output of the amplifier caused by both switches and amplifier, accounting for both Sample and Hold phases.





g) In the next page you see a sinusoid quantized with some resolution, together with its fft. The frequency of the sinusoid is (3/1024)·2MHz, the sampling frequency is 2MHz, and the simulation time is 512μs.
We notice that the quantization noise power is not distributed evenly in all bins – in fact, every other bin does not contain noise at all (notice that a level close to -300dB is practically zero). Explain why this is so (by the way, the same effect would be noticed if the signal frequency was (5/1024)·2MHz, or (7/1024)·2MHz, etc). Hint: the sinusoid has a DC level of exactly zero, and the reference voltages are V_{ref} and $-V_{ref}$, i.e. symmetrical around zero.


Waveform Window 31 – Virtuoso® Analog Design Environment (6)
Active 117
Window Zoom Axes Curves Markers Annotation Edit Tools Help
Transient Response
Vadc
500m
400m
300m
200m
100m
0.00
−100m
−200m
−300m
−400m
−500m
3.0000000u
173.66667u
344.33333u
515.00000u
time (s)
1: dB20(dft(Vadc))
0.00
−100
−200
−300
(dB)
0.0
10K
20K
30K
40K
mouse L: awvMouseSingleSelectPtCB()
M:
R: awvCurvesMenuCB()
HIT-Kit: 3.70 Tech: c35b4c3 User: piero