# Examination of Integrated A/D and D/A Converters

**14.00-19.00, Friday, Dec. 19, 2008**

I. Basic questions about A/D converters

a) Express the *rms* voltage of a full-scale sinusoidal input signal in terms of the quantization step $\Delta$ for an $n$-bit A/D converter.

b) Does the bandwidth over which the quantization noise is spread depend on the sampling frequency $f_s$? If so, express their relation. Furthermore, what conditions should be satisfied in order to assume that the quantization noise has a white spectral density?

c) What is the Nyquist bandwidth of an A/D converter, and what is its relation with the sampling frequency $f_s$?

d) Assume the A/D converter is non linear. If there is a sine wave of frequency $f_{in}$ at the input, and the sampling frequency is $f_s$, at what frequencies should you expect to see discrete tones at the output (in general)?

e) What is the kT/C noise, and why is it so important in converters?

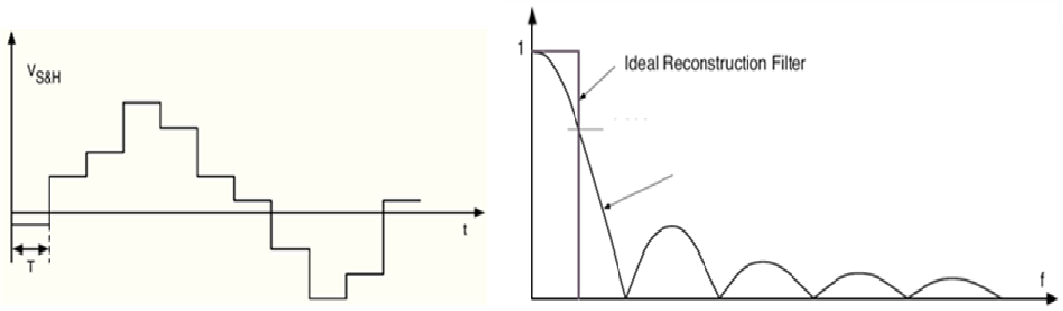
f) Yet another limit in the SNR of A/D converters is set by "jitter". What do we mean by that? Assume you desire an SNR of at least 90dB when sampling a 100MHz sine wave. What is the maximum acceptable time jitter to comply with the specifications?

II. Basic questions about D/A converters

a) The signal waveform after the sample-and-hold (S&H) of a D/A converter is shown on the left in the figure below, and the amplitude response of the ideal and the real S&H are shown on the right. Remembering that the transfer function of the real S&H is

$$H_{S\&H}(s) = \frac{1 - e^{-sT}}{s\tau}$$

where T=1/$f_s$ ($f_s$ = sampling frequency) and $\tau$ is a suitable gain factor. Derive an expression for the amplitude of $H_{S\&H}(j\omega)$, and find the frequencies at which $H_{S\&H}(j\omega)$ is null. How much has $H_{S\&H}(j\omega)$ dropped at ½ of the Nyquist frequency, compared to its low-frequency value?




b) What is a reconstruction filter, and why is it often needed after a D/A converter? Does it help to have a large ratio of $f_s$ to $f_B$, where $f_B$ is the signal bandwidth?

III. Basic questions about ΣΔ converters

a) What are the key ideas behind ΣΔ converters? What are the main advantages of ΣΔ converters over Nyquist converters?

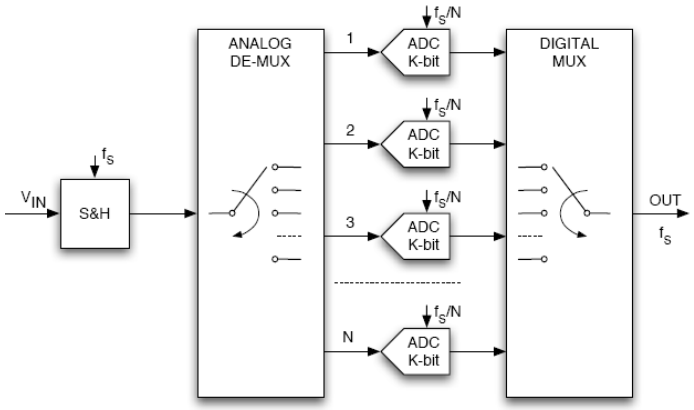
b) Why is it difficult to replace a full-flash converter with a ΣΔ converter?

c) What particular implementation of a ΣΔ converter is intrinsically linear (excluding second-order effects), and why?

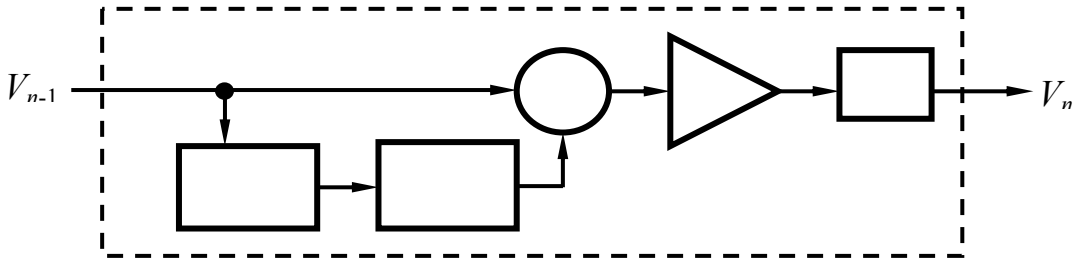
d) What is the "individual level averaging" technique, and what is it good for?

VI. Specific questions about converters

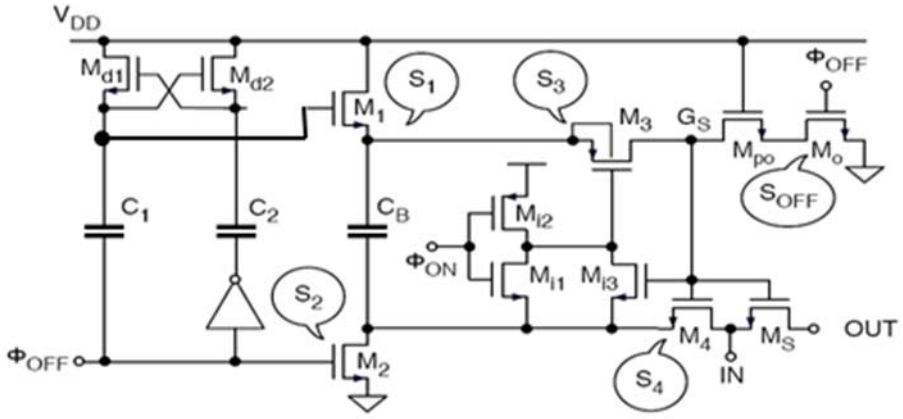
a) What kind of converter is the one below? Explain how it works, when it is employed, and what its main advantages and disadvantages are.



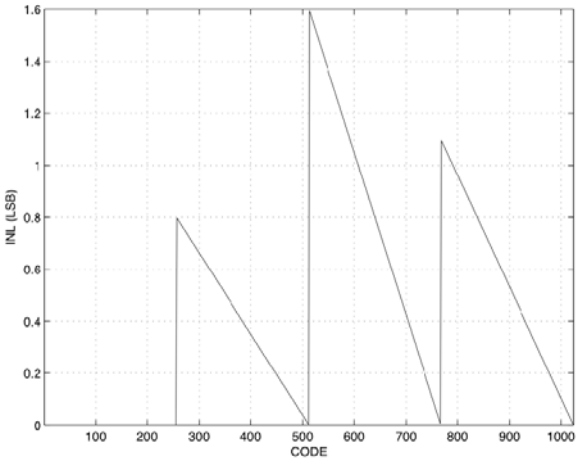

b) What kind of converter is the one shown below? Explain the function of the various blocks in it.




c) What is the circuit below? What are its main features? Explain in some details how it works.



d) The INL of a 10 bit ADC has a sawtooth-like behavior, with a jump of 1.6 LSB at half-scale, and 0.8 LSB and 1.1 LSB at one quarter and three quarters of the full scale (see below). Draw an approximate plot of the DNL and of the input-output transfer function around the three points.




e) What kind of converter is the one in fig. b) below? It is well known that RC delays have an adverse impact on the conversion speed. Assuming the total capacitive load constant, which are the two switch configurations giving rise to the highest delay, and why?