Examination in Integrated A/D and D/A Converters, ETI220

8.00-13.00, Saturday, Dec. 19, 2009

I. Basic questions about A/D converters

a) Explain why windowing is used when the fft of a signal is taken. When can we use a rectangular window?

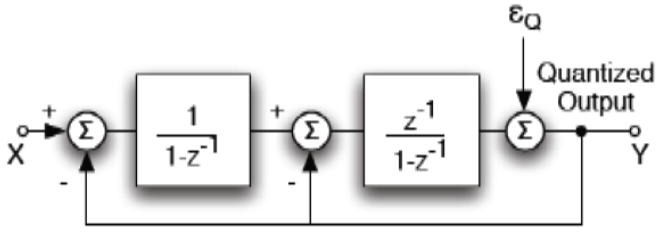
b) What causes the so-called signal feedthrough in a Sample & Hold circuit? Why is feedthrough a problem?

c) Assume a 10b Nyquist-rate ADC is operated at an oversampling ratio of 8. Ideally, what is the maximum SNR achievable?

d) Derive the SNR expression for an ADC converting a sinusoidal signal with angular frequency ω, if the clock has a jitter δ_j.

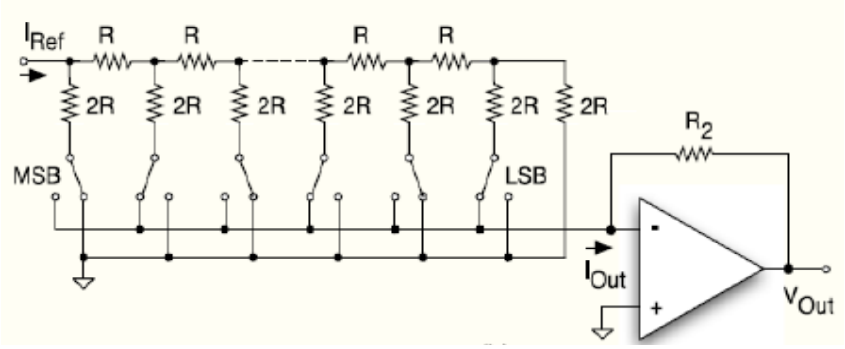
II. Specific questions about converters

a) Below you can se the linearized circuit of a Delta-Sigma converter. Find the signal transfer function and the noise transfer function. Explain why Delta-Sigma converters are so popular.



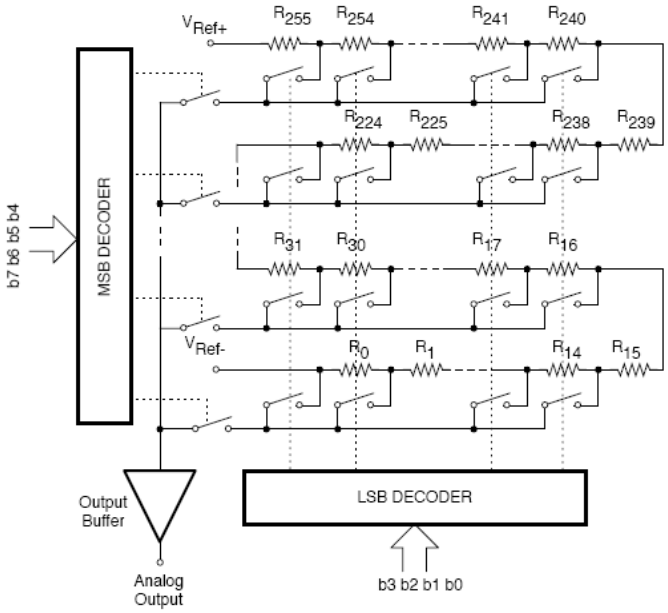
b) It is well-known that glitches are a problem in binary DACs.
   1. Explain why glitches may be generated in binary DACs.
   2. Assuming that a 500 MSample/s 10-bit D/A converter with an output range between 0V and 1V produces 50ps glitches with a (maximum) amplitude of 100mV, what is the worst-case ratio between glitch area and LSB? If this ratio is required to be 0.5, what is the maximum allowable glitch length?

c) Below you see an R-2R current-based DAC. Show that its output is indeed an analog version of the digital input.

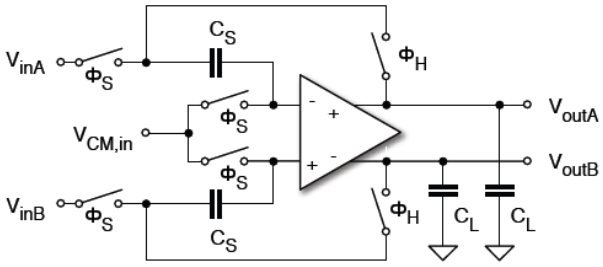


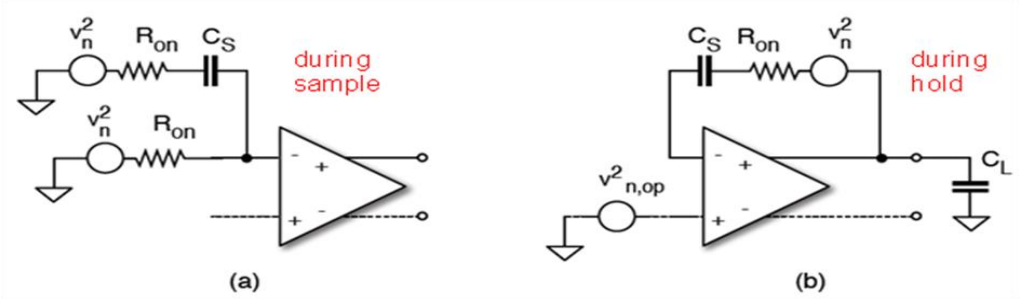
d) A very popular ADC architecture is the charge-redistribution successive-approximation ADC.
   1. Draw the schematic circuit of a charge-redistribution successive-approximation ADC, and explain how it works.
   2. Modify the ADC, in order to make it (ideally) insensitive to the comparator offset.
   3. Assume you want to implement a 12b conversion. What is the maximum mismatch allowed between the capacitors, if we allow for a conversion error of ½ LSB at most?
   4. Why is this kind of ADC not suited for a high conversion speed?

e) Explain what conversion is implemented by the circuit below, and how it works. Are there advantages and/or disadvantages, compared to other ways of implementing the same conversion?



f) Below you see a flip-around Sample & Hold circuit, with the (single-ended) circuits for noise analysis during Sample and during Hold. Assume that the amplifier noise is $v_{n,op}^2 = 4kT\gamma'/g_m$, the amplifier gain $A = \omega_T/s$, and $\omega_T = g_m/C_L$. Find the total noise at the output of the amplifier caused by both switches and amplifier, accounting for both Sample and Hold phases.





g) Below you see a sinusoid quantized with some resolution, together with its fft. The frequency of the sinusoid is (3/1024)·2MHz, the sampling frequency is 2MHz, and the simulation time is 512μs.
We notice that the quantization noise power is not distributed evenly in all bins – in fact, every other bin does not contain noise at all (notice that a level close to -300dB is practically zero). Explain why this is so (by the way, the same effect would be noticed if the signal frequency was (5/1024)·2MHz, or (7/1024)·2MHz, etc). Hint: the sinusoid has a DC level of exactly zero, and the reference voltages are V_{ref} and $-V_{ref}$, i.e. symmetrical around zero.
Try to answer this question only when you are ready with the other ones ☺