Integrated Radio Electronics

Laboratory 2: Voltage Controlled Oscillator

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1- Introduction

This lab introduces the simulation methods and software capabilities of Cadence SpectreRF commonly used for designing and verifying voltage controlled oscillators (VCOs). It is assumed that the students have already learned how to set up a simulation in Cadence, run it, and report the results, therefore it is strongly suggested that they do the first laboratory prior to this one.

VCOs play a key role in LO/clock generation units in almost all analog and digital embedded systems. Briefly speaking, they generate an oscillatory signal whose frequency is dependent on an input voltage level. There are various types of VCOs such as inverter-based ring oscillators, differential ring oscillators, and LC oscillators. LC oscillators generally outperforms ring oscillators in terms of phase noise and supply sensitivity, particularly as the frequency increases. Hence, in this lab we focus on an LC oscillator and investigate design techniques and simulation methods.

Essentially we can characterize a VCO by measuring the following metrics:

1- Power consumption
2- Oscillation frequency and tuning range
3- Phase noise
4- Power supply sensitivity
5- Harmonic generation

To evaluate the VCO performance, in this lab the following simulation are introduced:

1- PSS simulation for oscillation frequency, harmonics, tuning range, and supply sensitivity
2- Transient simulation for investigating current steering and power considerations
3- PSS+Pnoise simulation for phase noise

2- Schematic View

First a schematic view must be created:

- Create a schematic cellview in the RFIC_Labs library, call it ‘VCO’
- Draw the schematic according to Fig. 1.
- Use the *nlvtlp* transistors. Leave all values as default, except make the width a variable.

- Use ideal inductors ‘ind’ from analogLib. Set the inductance to 2 nH. To model the power dissipation in the inductor, put a resistor in parallel. Assume Q = 10. Also place *Cpar* = 100 fF in parallel with each inductor. Calculate *Cp* to make the tank resonate at 2.5 GHz.
  Question: What capacitances are modeled by *Cpar*?
- Place DC voltage and current sources to bias the circuit. Assume the power budget is 1.2 mW and VDD = 1.2V, thus I_{tail} = 1mA.

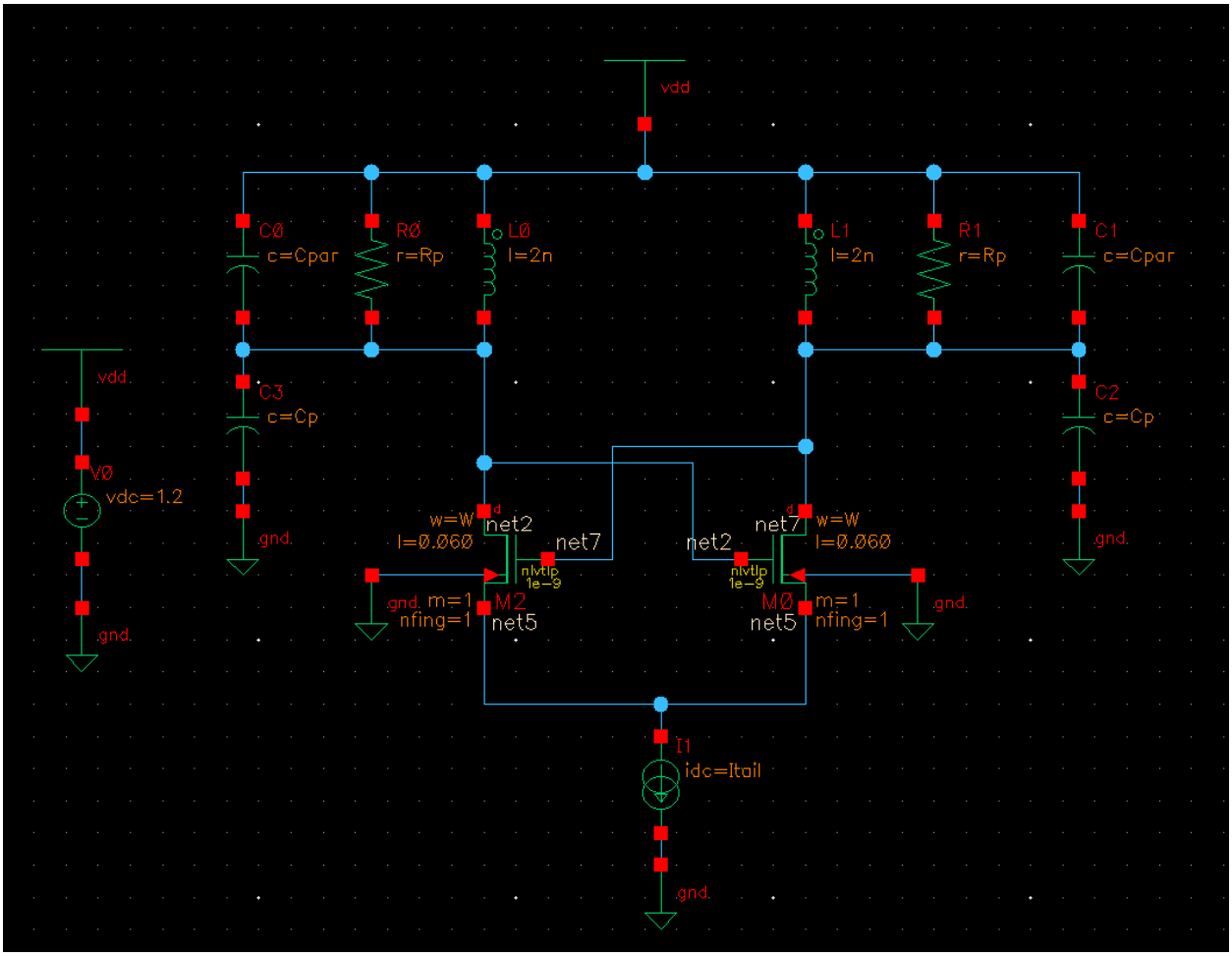

Figure 1: Cross-coupled LC oscillator.

3- Setting up Analog Environment Options

To reach satisfactorily reliable and precise results the default parameters of ADE should be changed. In this way the residual errors used by the equation solver to converge to the final result become smaller. Of course, nothing good comes for free, we pay it back by larger memory usage and longer simulation time. Therefore, the values shown in Fig. 3 are chosen for a moderate but satisfactory precision.

- Under Simulation>Options>Analog (Fig. 2), set the values in TOLERANCE OPTIONS according to Fig. 3.

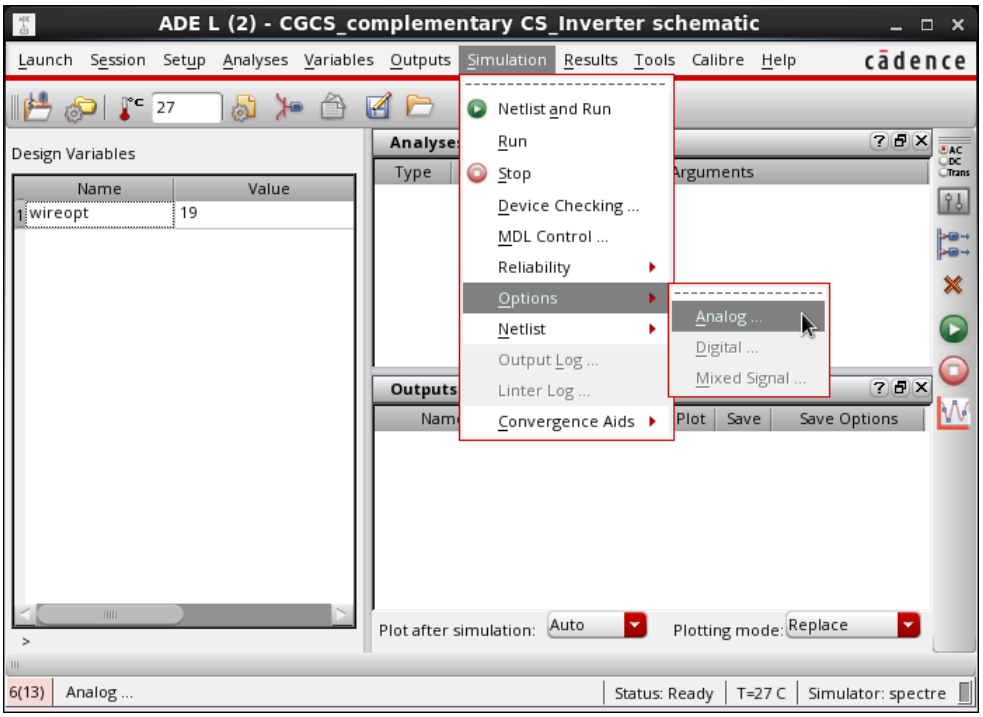
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Fig. 2

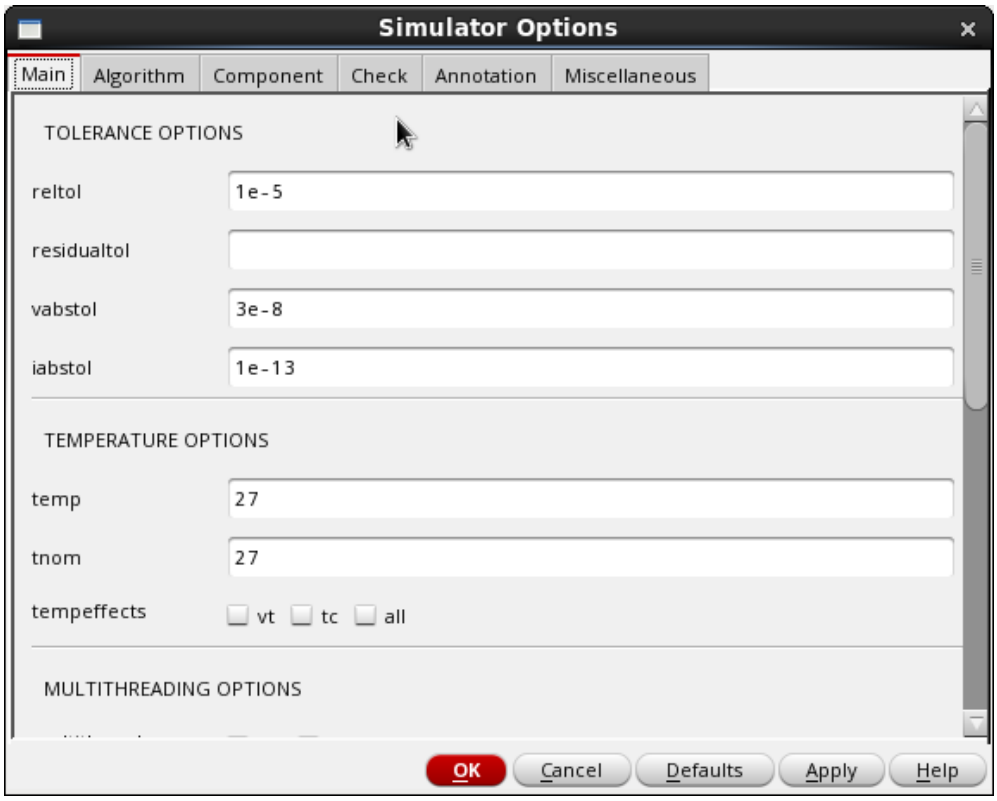
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Fig. 3

4- Transient Simulation

We perform transient simulation for two purposes. First, to ensure that the oscillation happens in the first place and to find the oscillation frequency for proceeding simulations. Second, we should make certain that the cross-coupled transistors are switched abruptly, i.e. the drain currents are close enough to square-wave. Otherwise, the tail current is not steered completely and the oscillation amplitude does not reach its maximum possible value. It exacerbates phase noise and degrades the figure of merit.

- In ADE, start by importing variables and set W = 10um, Itail = 1mA, and the passives according to your calculations.
- Select Outputs → To Be Saved → Select On Design and select the drain pins of the two transistors and press Esc. In the Outputs tab in the ADE window, it should now say M1/d and M0/d. This causes the drain currents to be saved and thus be plottable.
- Go to Analyses → tran → Options → Algorithm and configure it according to Fig. 4, then press OK.

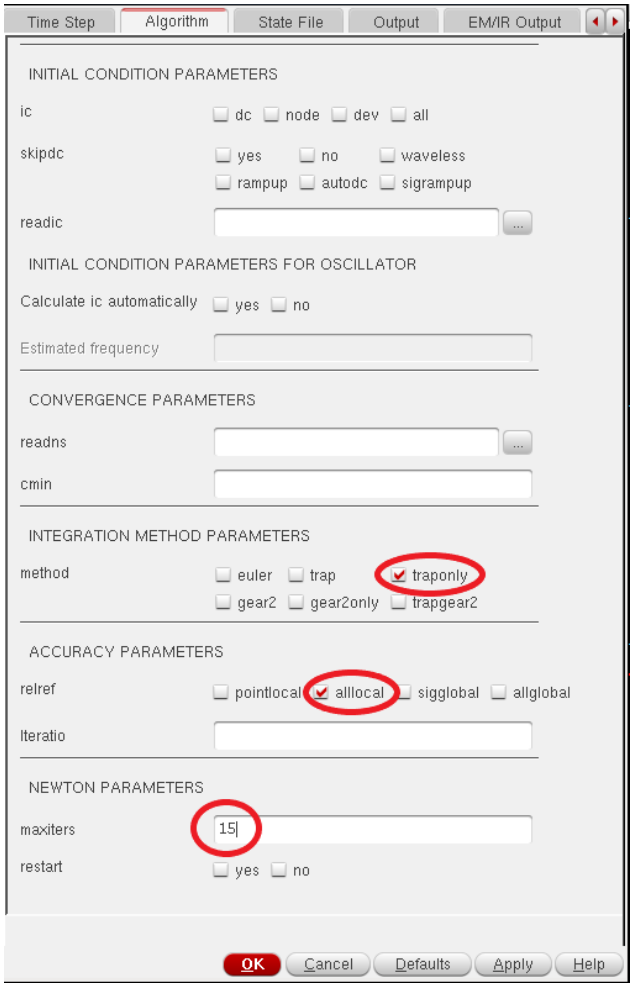


Fig. 4: Transient options

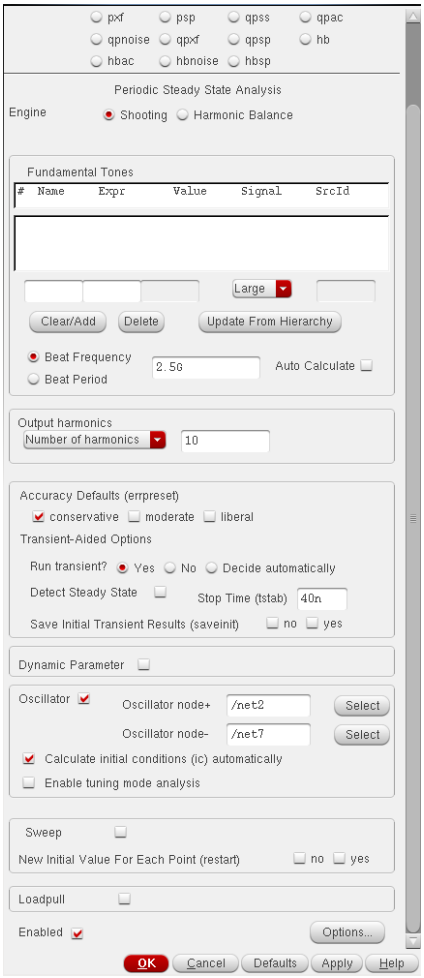
- Set “stop time” of tran to about 100 oscillation periods. Press OK.
- We need to create some asymmetry in the oscillator, otherwise the simulation will not start. In ADE, go to Simulation → Convergence Aids → Initial Condition. Type 1 in the field and (WITHOUT pressing OK) press on one of the outputs in the oscillator and then press OK.
- Run the simulation and plot the single-ended drain voltage. Does it reach a stable oscillation? Measure a rough value of start-up time (the time it takes to reach stable oscillation). If no oscillation occurs, try to make your transistors wider.
- Zoom in on a part where stable oscillation has occurred. Then open the calculator, tick “Clip” and select “Wave” and then click on the plot. This should generate a string starting with “clipX(…”. Go to the Function Panel, select “frequency”, and press the “Evaluate buffer” button
- Is your oscillation frequency 2.5 GHz? If not, adjust your *Cp*.
- Measure the peak-to-peak value of the stable oscillations. Are they in line with theoretical expectation?
- Now plot the drain currents. Are they square-wave?
- Double the transistors’ width and plot the drain currents and oscillatory voltage. Notice how the transitions have changed. How can you associate the oscillation amplitude with the current waveform?
- Size the transistors so that the peak-to-peak single-ended oscillation reaches about 380 mV. Do the cross-coupled transistors go into the triode region? Run a DC simulation to check what the threshold voltage is.
- Plot the tail voltage, above the current source. Is any oscillation going on? At what frequency?

5- PSS + Pnoise Analysis

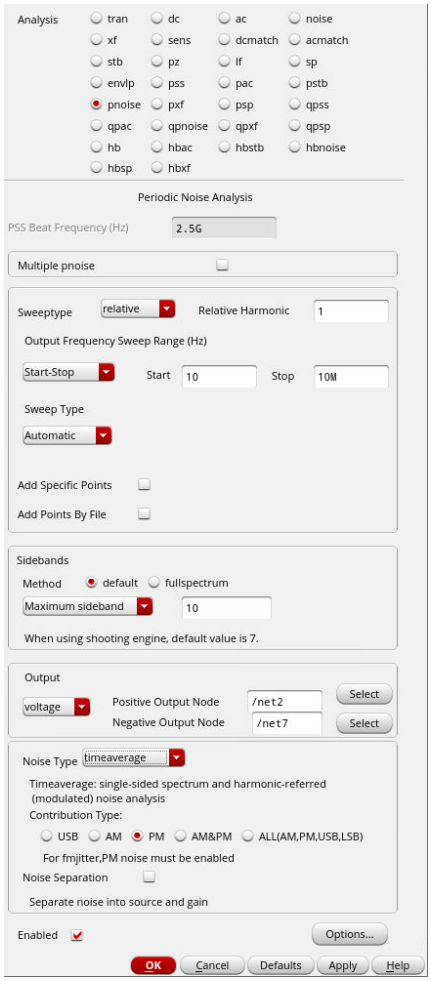
You will now simulate the phase noise, which is done with periodic steady-state analysis (pss) followed by a periodic noise analysis (pnoise). A number of parameters need to be specified prior to the analysis, see Fig. 5 and Fig. 6.

- Choose pss analysis.
- Set the ’Fundamental (Beat) Frequency’ to the oscillation frequency as found in the previous simulation (or slightly lower if you have problem with convergence).
- Set ’Number of harmonics’ to 10. The value of 10 means one can see 10 tones from the oscillation.
- Under ‘Accuracy Defaults (errpreset)’, select ‘conservative’.
- Set initial transient to a time that corresponds to about 100 oscillation periods.
- Click on ’Oscillator’ and choose ’oscillator node’ (click on the drain nets (not the pins!) in the schematic).
- Click on ’Options’ and specify integration method to ’traponly’. Press OK.
- The pss form should look like Fig. 5(a).
- Press ‘Apply’ and click on ‘pnoise’

- Change sweeptype to ‘relative’ and set ‘Relative Harmonic’ to 1 (we are interested in offset frequencies near the carrier frequency).
- Choose ’Start’ and ’Stop’ to 10Hz and 10MHz, respectively.
- Sideband, choose ’maximum sideband’ to the same number as ’Number of harmonics’ (10).
- Change ‘Output’ from ‘probe’ to ‘voltage’ and select the oscillator outputs (the drain nets).
- Change ‘Input Source’ to ‘none’.
- The pnoise form should look like Fig. 5(b). Press OK.
- Start the simulation. If the simulation does not converge, try to give a better estimation for the ’Fundamental (Beat) Frequency’ or/and increase the length of initial transient with tperiod/4.



(a)



(b)

Fig. 5

- From Results/Direct Plot/PSS, plot the spectrum in dB20 and the voltage in time domain (Fig. 6). Also report total harmonic distortion (THD). Other than the fundamental tone, which harmonic is the strongest? How much weaker than the fundamental tone is it?
- From Results/Direct Plot/pnoise, plot “Phase Noise” in dBc/Hz (Fig. 7). Give an estimate of the flicker corner frequency.

- Double the bias current and repeat above tasks. What differences have occurred and why? Look at the phase noise at both high and low offset frequencies.
- Revert the tail current to 1 mA.

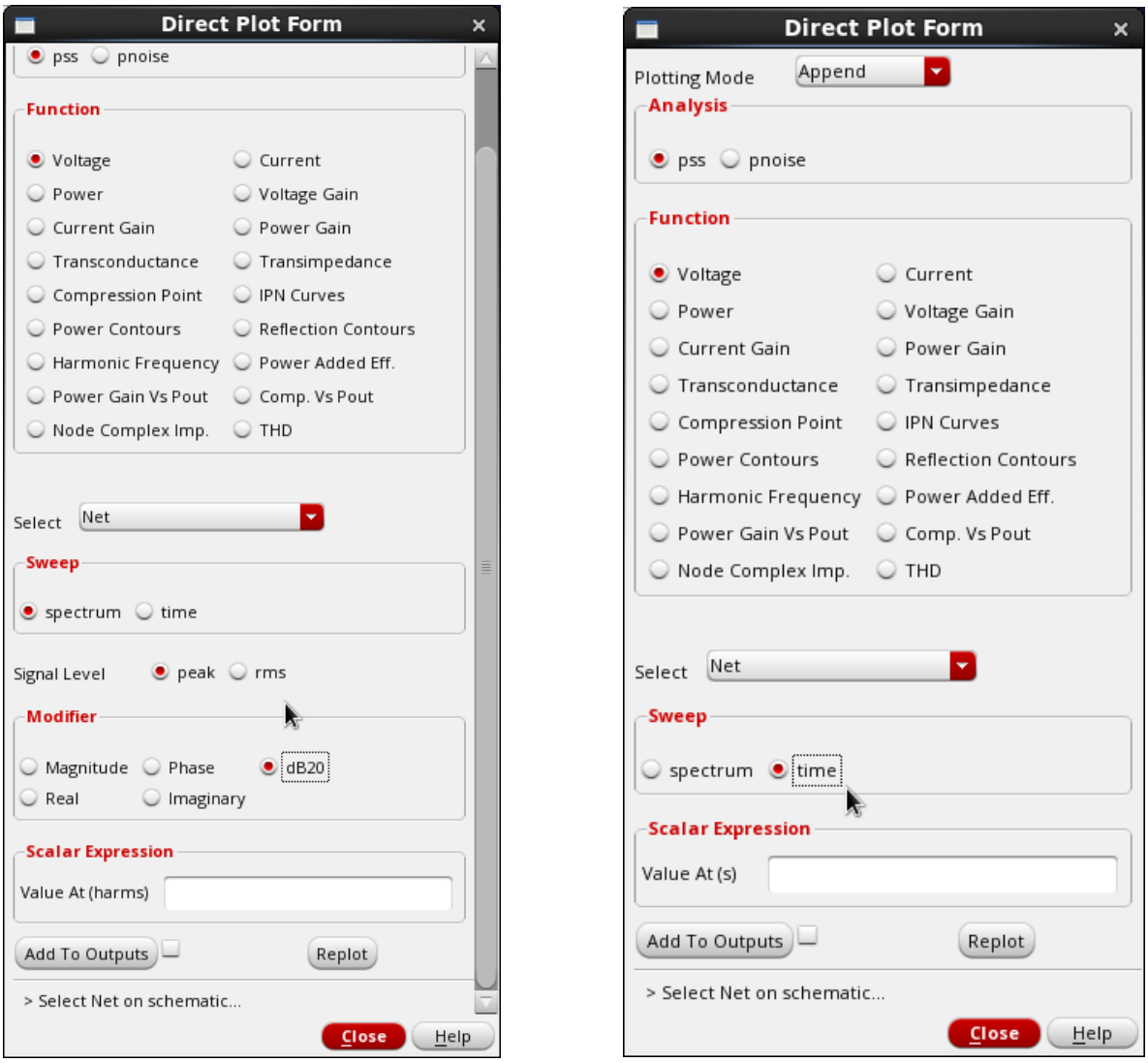


Fig. 6

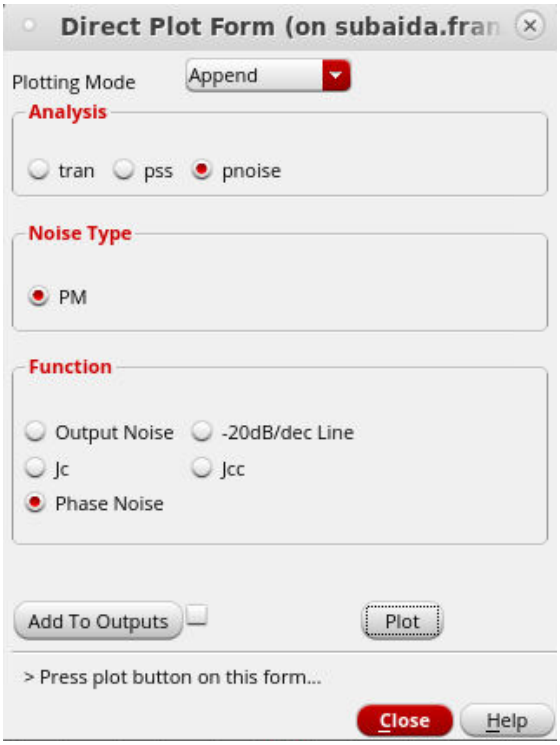


Fig. 7

6- Effect of Tail Capacitance

Now add a capacitor from the tail to the ground as depicted in Fig. 8. Call it Ctail and give it value 1pF.

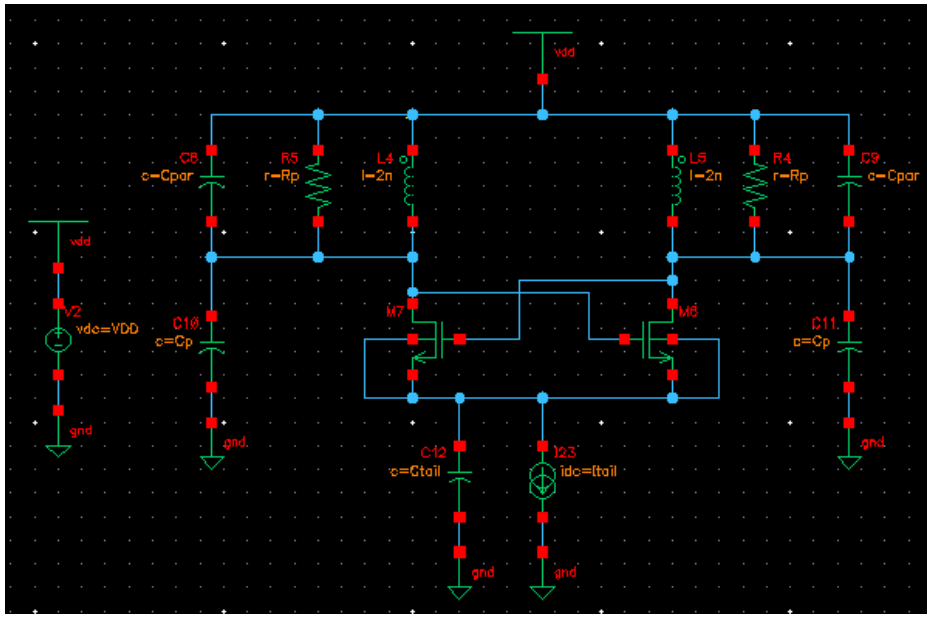


Fig. 8

- Run transient simulation and plot the drain currents again. Is there any change? What happens to the rise time and fall time of square wave?
- Run PSS+Pnoise simulation and plot the spectrum, THD, and phase noise. Compare the second harmonic, flicker corner frequency, and THD with the previous results.

7- Current Source Implementation

In this section we are going to replace the ideal current source with a transistor-level current mirror. Assume we have a reliable (ideal) bias current of 200 µA (1/5 of the tail current). As illustrated in Fig. 9, we can bias the oscillator with a diode-connected current mirror.

- Size the current mirror transistors so that: 1) the tail current is provided, and 2) the tail transistor always operates in saturation.
- Run PSS+Pnoise simulation and plot phase noise. How much the phase noise has degraded? Is this degradation different between flicker and thermal noise dominated regions?
- Open "Noise summary" from Results/Print. It gives you a list of the noise sources and their contribution in total noise. Set it up according to Fig. 10 and click OK. Note that the 'Frequency Spot' is relative to the fundamental frequency, i.e. the noise we are looking at is the noise at f_0 + 1 kHz. What is the major source of noise? Try some different frequencies and compare.
- Implement a low-pass RC filter as depicted in Fig. 11 to filter out the current mirror's flicker noise and examine how the phase noise and contributions change (R=2 kΩ, C=1 pF). Does it help with the flicker noise?
- How we can reduce the current mirror's flicker noise?

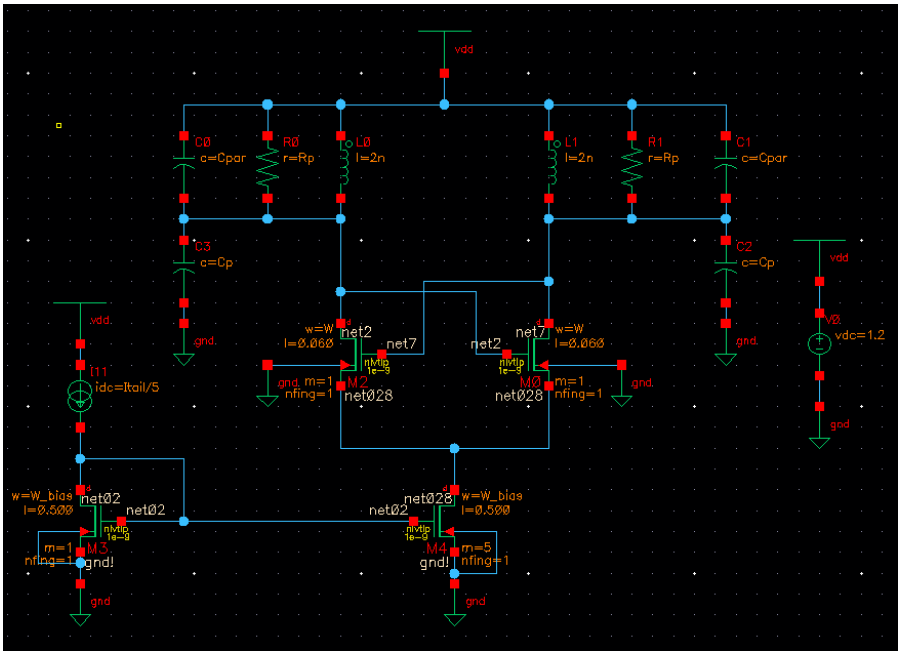
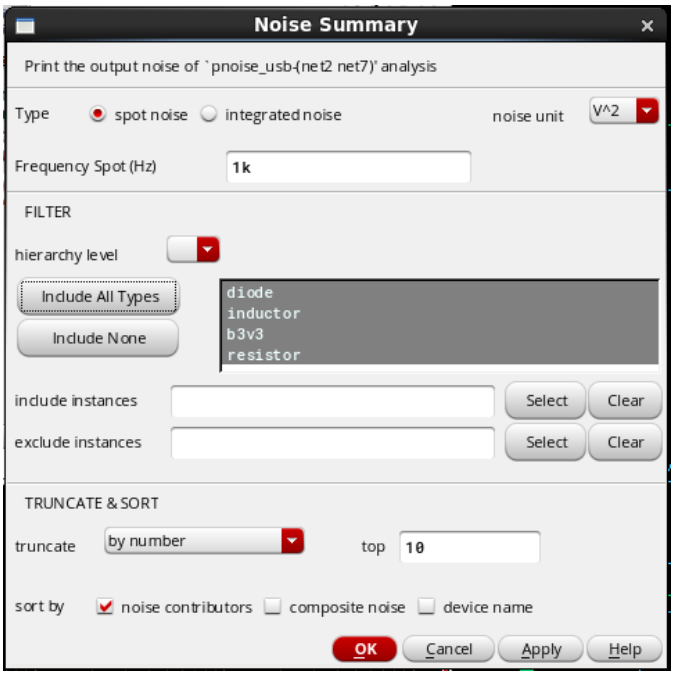


Fig. 9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resistor
include instances
exclude instances
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Clear
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by number
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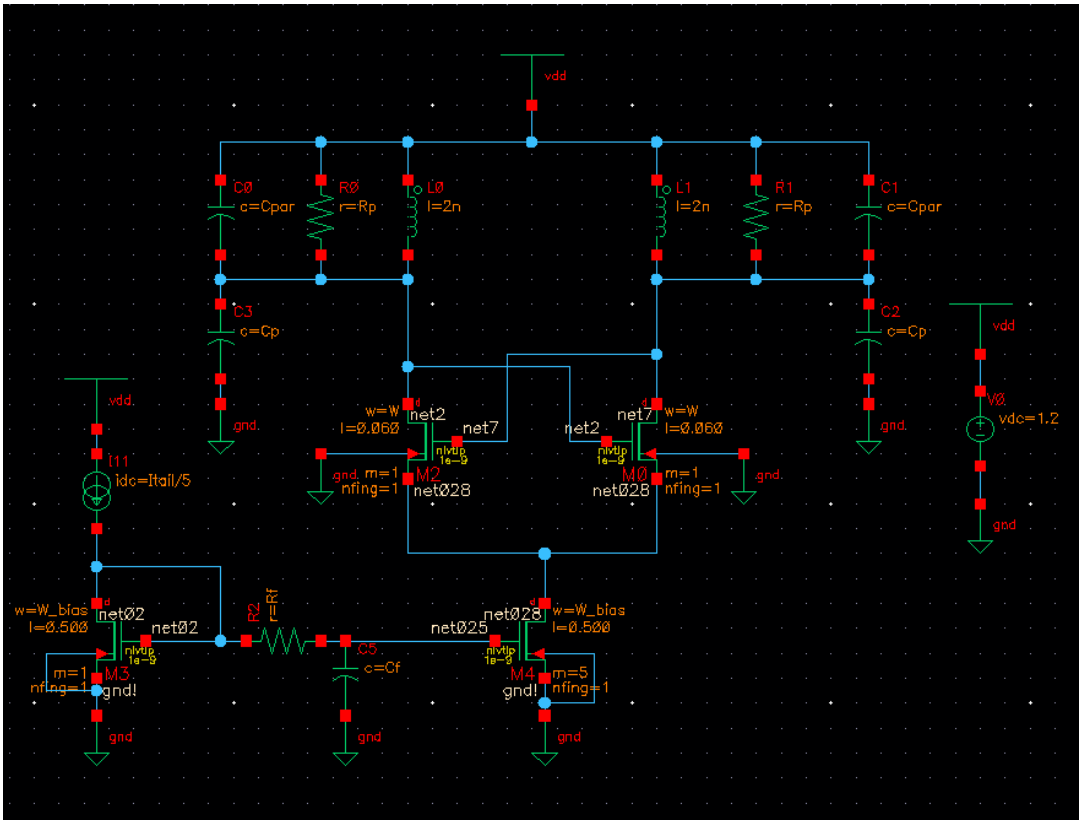
Fig. 10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C2
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M4
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R2
Rf
C5
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gnd
gnd!

Fig. 11

8- Voltage Controlled Oscillator (VCO)

Finally, in this section you will turn the designed oscillator into a VCO by adding varactors, which is a voltage-dependent capacitor. By tuning a control voltage, we can change the resonance frequency of the LC-tank and thereby the oscillation frequency. In most applications a combination of varactors and switched-capacitors are used to cover all the desired frequency range. 10 to 20 percent of the center oscillation frequency is a reasonable number for tuning range. In this example, the tunable range is assumed 10%, about 200 MHz. For simplicity in this lab, we leave out switched capacitors and try to cover all the range with a pair of varactors as shown in Fig. 12. Use *nlvtlp* and short the source and drain of each transistor and connect them to each other and a voltage source with a variable 'Vcont' as the DC voltage, see Fig. 12. Connect the bulks to ground. Use the minimum length and a width of 40µm. Set the 'Number of devices in //' to a variable, for instance 'xVarac'. Since the required width of the varactor to cover a 10% tuning range is very large, it is better to scale the number of devices in parallel compared to scaling the width, to ensure that we are operating within the modeled size range of the transistor.

- Set xVarac to 1 and run PSS+Pnoise simulation while sweeping V_{cont} from 0 to 1.2V, as shown in Fig. 13. Plot the oscillation frequency and phase noise versus V_{cont}. Select the fundamental harmonic from "Harmonic Frequency" form as illustrated in Fig. 15. Is your tuning range large enough? If not, increase xVarac. The varactors will add parasitic capacitance, which will lower your fundamental frequency. Decrease *Cp* to counteract this.
- Calculate K_{vco} which is the maximum slope of the oscillation frequency variations versus V_{cont}. Has the oscillation amplitude changed? Why?
- Change your VDD DC voltage from 1.2V to a variable called 'VDD'. Run PSS+Pnoise, but this time sweep VDD from 1.15V to 1.25V in steps of 0.02V. Calculate K_{vdd}. Is the oscillation frequency dependent on VDD? Explain this phenomenon which is called "frequency pushing".

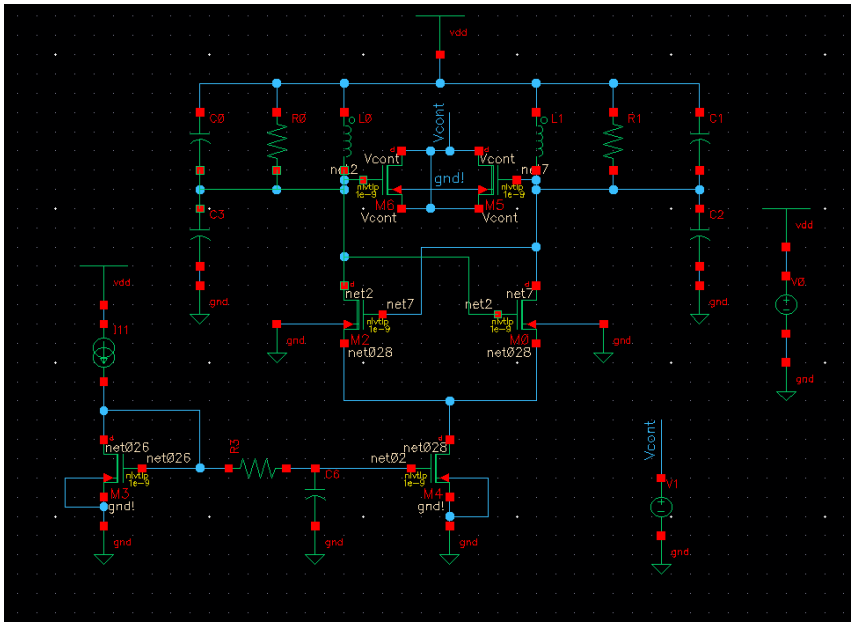
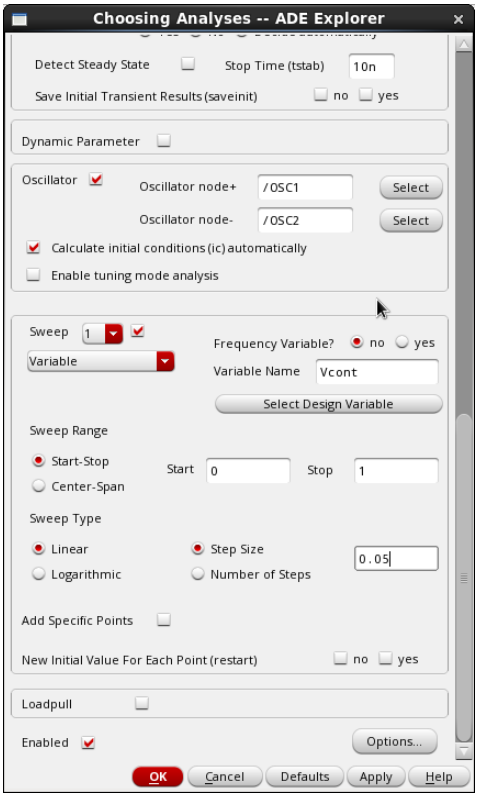


Fig. 12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Linear
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Step Size
Number of Steps
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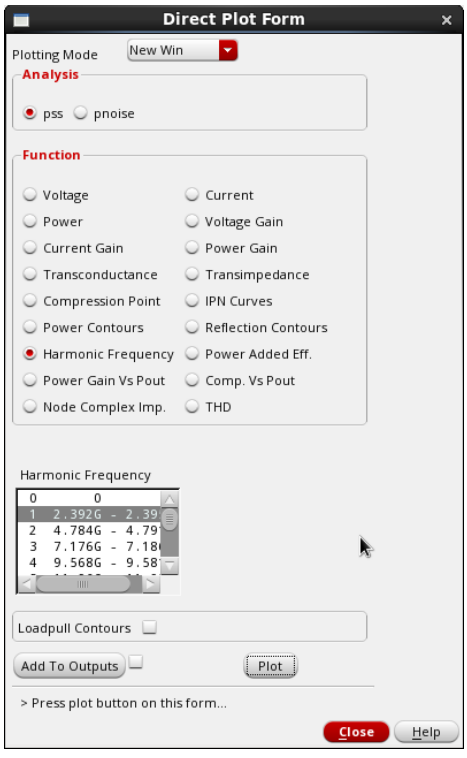
Fig. 13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3 7.176G - 7.18
4 9.568G - 9.58
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Fig. 14