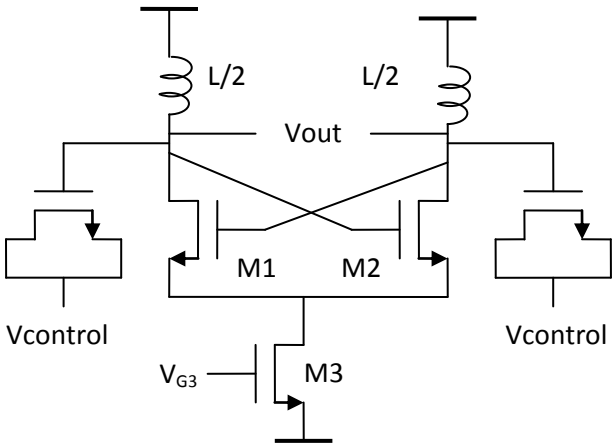
# Handin Exercise 2, Oscillators

This exercise deals with voltage controlled oscillators (VCOs) and is a preparation for lab 2. A differential oscillator shown in the figure below is to be designed. You will need to refer to the data sheet of the 130nm CMOS process. The following requirements and information is provided:

- Supply voltage = 1.2V
- Center frequency = 4.2GHz
- L=3nF, $Q_L$=15
- L=0.2um for all transistors, including the varactor




1. Calculate the effective parallel resistance of the load resonating at the center frequency.
2. Calculate the bias current needed to make the oscillation amplitude 0.7Vpk/side.
3. Calculate the efficiency of conversion from battery to resonator power.
4. Calculate the width and gate bias voltage of M3 for providing the bias current at 200mV gate overdrive.
5. Calculate the width of M1 and M2 so they have 0.15V gate overdrive in the zero crossing.
6. Calculate the startup loop gain.
7. Calculate the width of the varactors so that the center frequency becomes 4.2GHz. Take the drain capacitances of M1 and M2 into account, and assume the varactor has a capacitance range equal to 2, that is Cmax/Cmin=2.
8. Calculate the minimum and maximum frequency of oscillation.
9. Calculate the approximate finger length of the transistors (both switch devices and varactors) used to make the losses due to gate resistance much smaller than the losses of the inductors.
10. Calculate the phase noise at 3MHz offset from an oscillation frequency at 4.2GHz, assuming a noise factor F=6.
11. Does M3 contribute to the phase noise? Why/why not?