Implementation of Faster-than-Nyquist signaling transceivers

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Outline

- Motivation for Faster-than-Nyquist signaling (FTN).
- FTN Transceiver for multi-carrier systems.
- Decoding performance.
- Hardware considerations for FTN decoder implementation.
- Results
  - Performance of FTN decoder from RTL simulations.
  - Area usage.
  - Power and throughput.

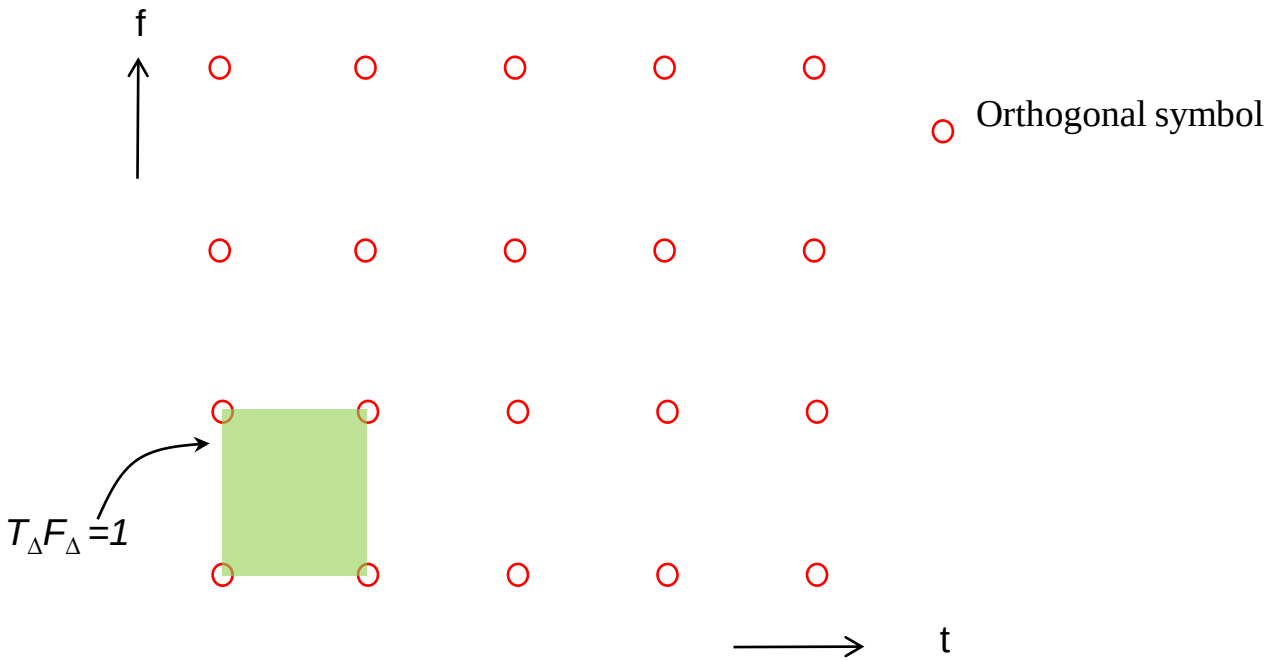
Introduction

- Original concept by J.E. Mazo in 1975 (Bell Syst. Tech. J).
- Main idea
  - to transmit information beyond that allowed by Nyquist's criterion for ISI free transmission.
  - more symbols stacked in time and/or freq – induce intentional interference.
- Bandwidth efficient systems.

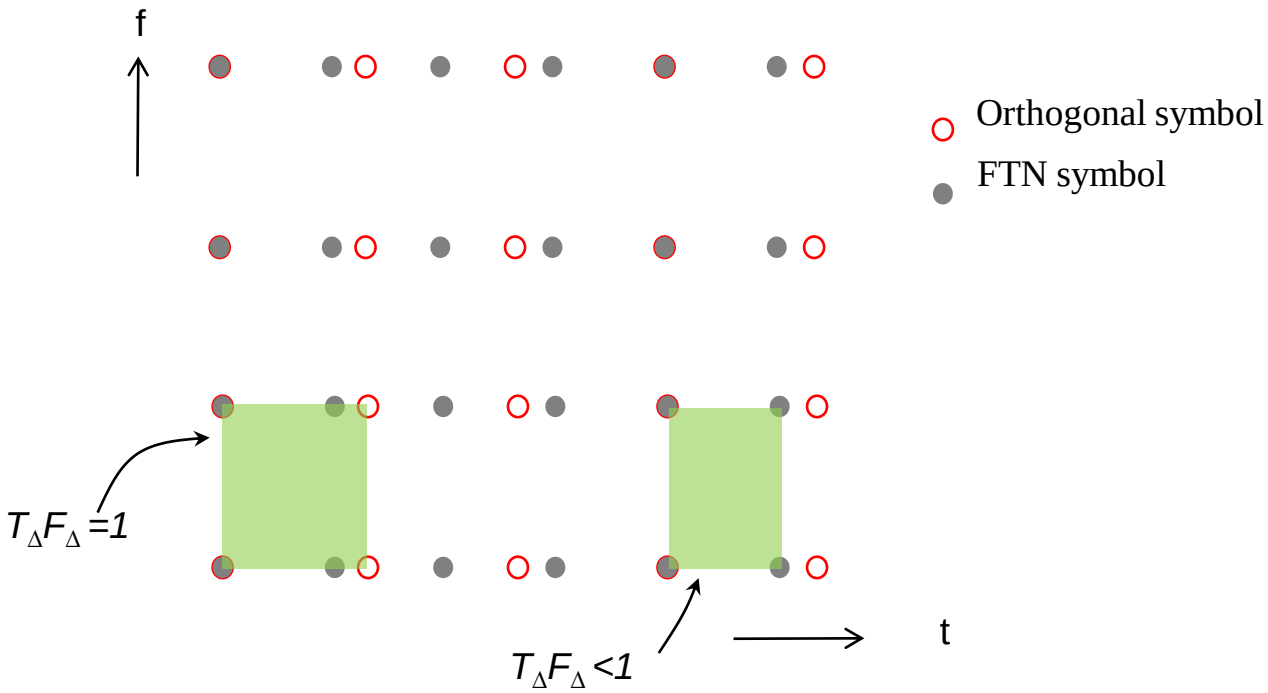
Motivation

- Bandwidth is a premium resource today.
- Improving logic density with advancing silicon technology.
  - more complex signal processing in transceivers and use bandwidth resources efficiently.
- Principal objective :
  - Feasibility evaluation and hardware implementation of decoders for FTN.
  - Multicarrier systems (OFDM based).
  - Tradeoff between complexity overhead vs. improvement in bandwidth efficiency

FTN vs. Orthogonal system



FTN vs. Orthogonal system



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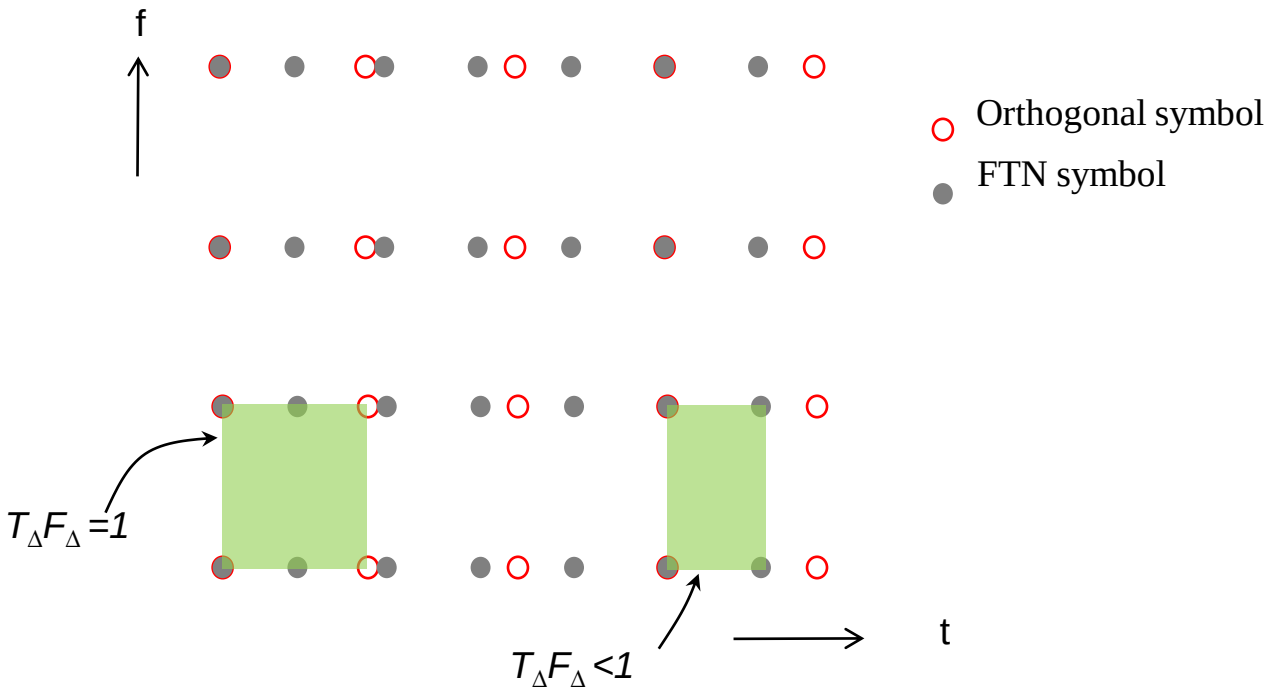
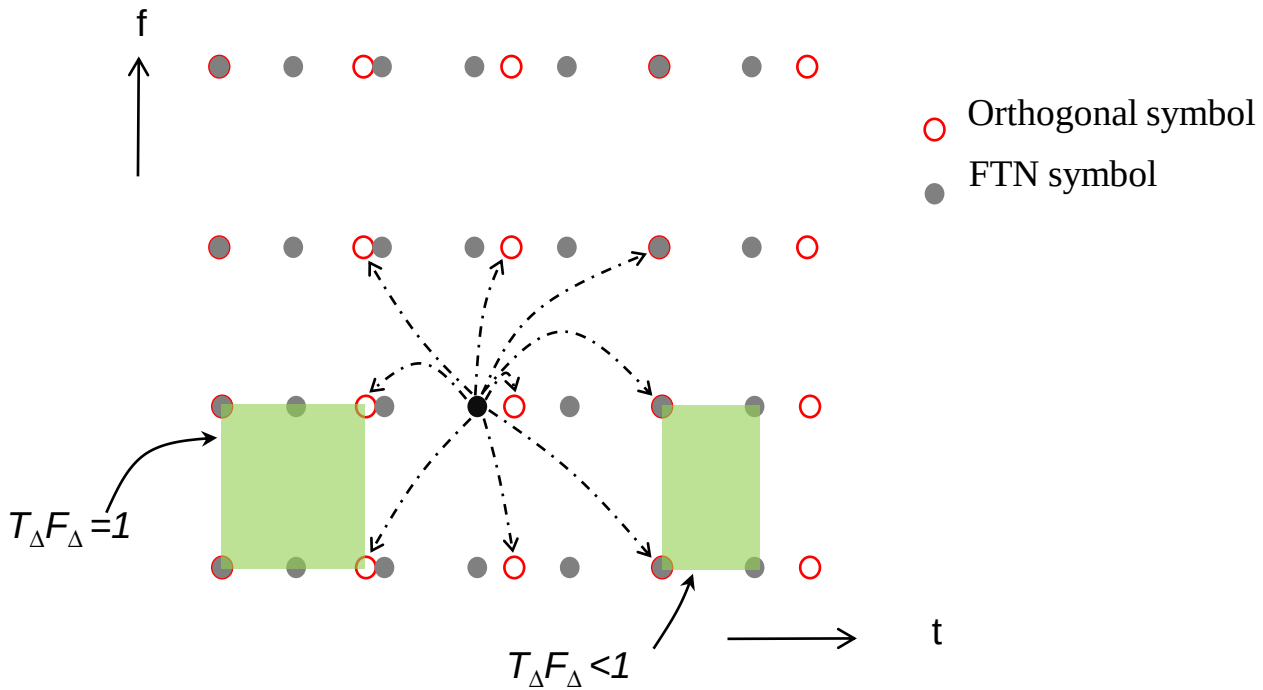
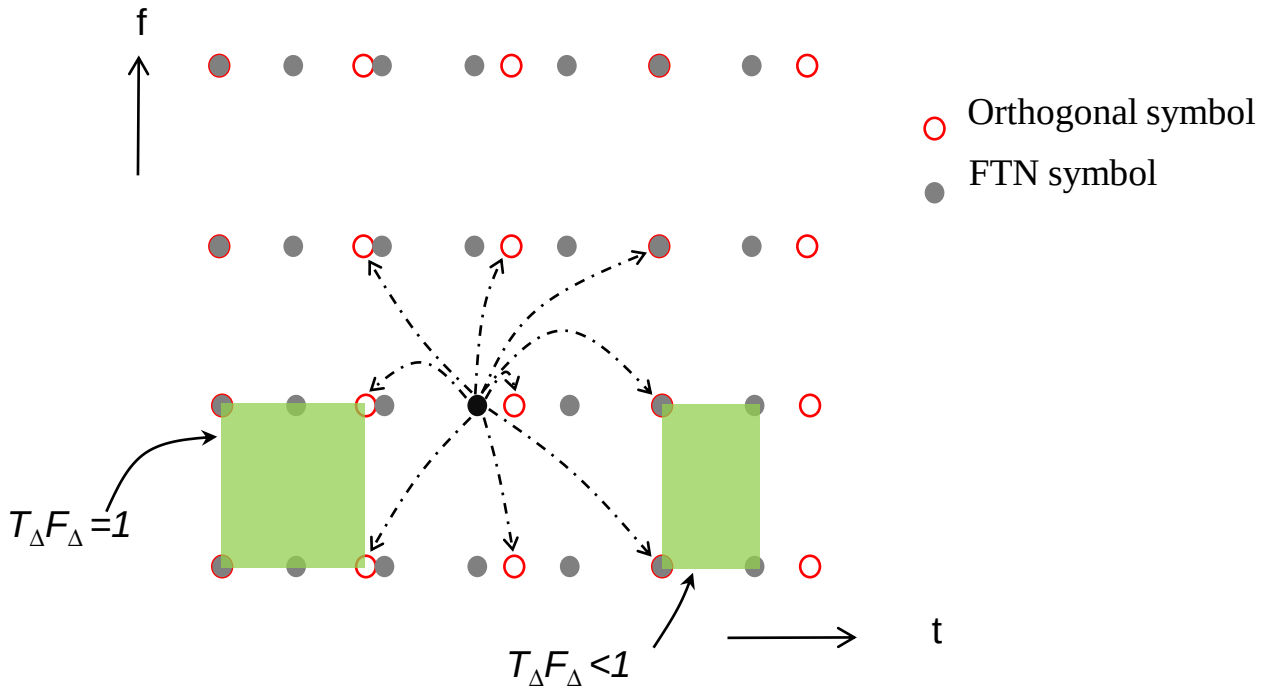


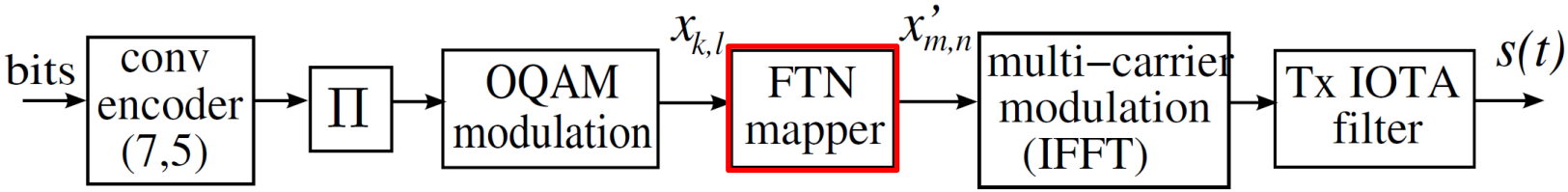
FTN vs. Orthogonal system



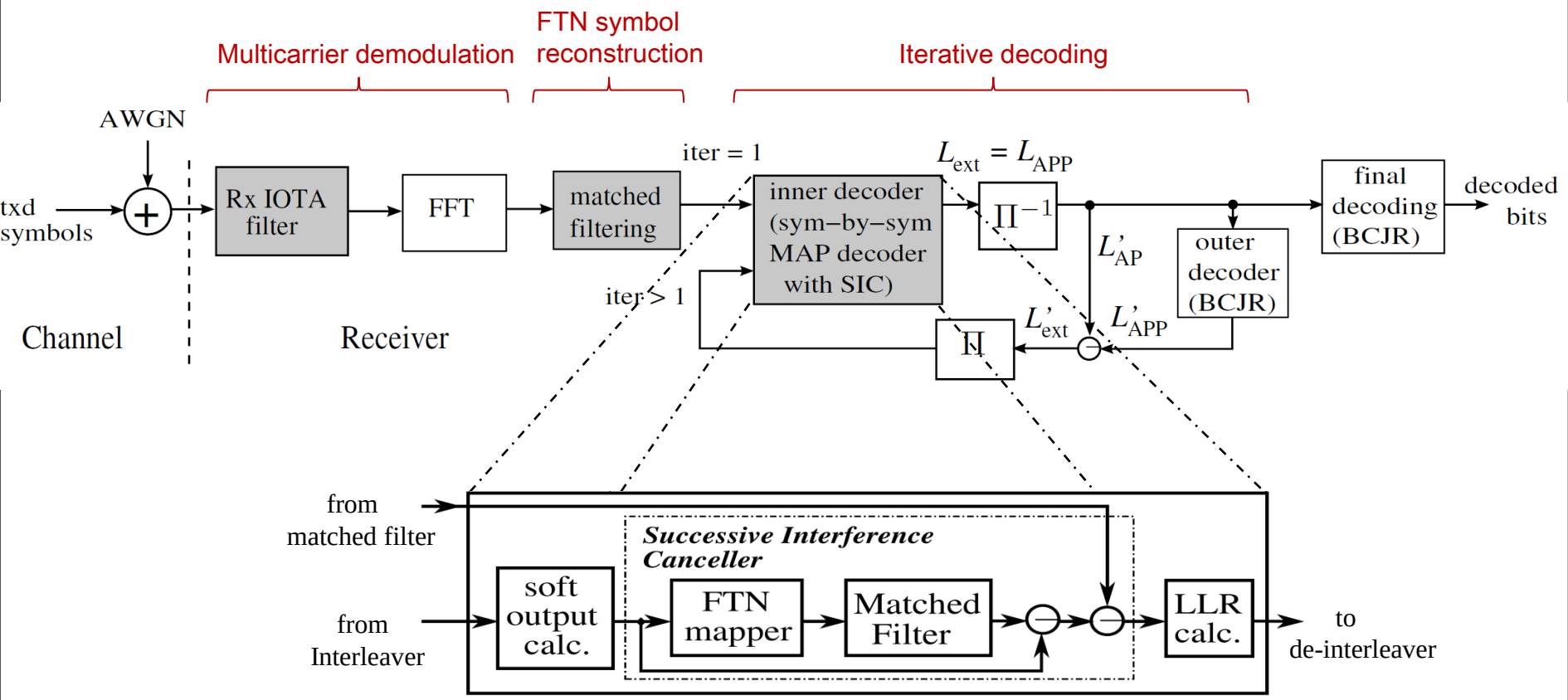
FTN vs. Orthogonal system



FTN transmitter: look-up table based

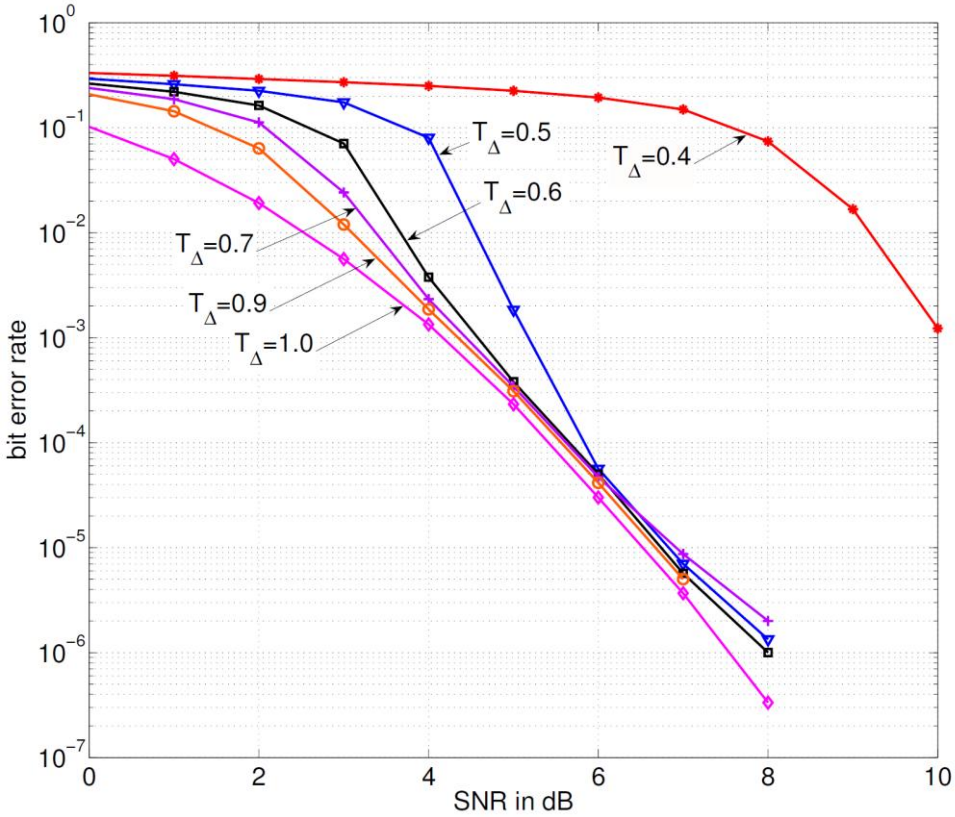


Receiver


Multicarrier demodulation
FTN symbol reconstruction
Iterative decoding
AWGN
txd symbols
Rx IOTA filter
FFT
matched filtering
iter = 1
iter > 1
inner decoder (sym–by–sym MAP decoder with SIC)
$L_{ext} = L_{APP}$
Π^{-1}
L'_{AP}
outer decoder (BCJR)
final decoding (BCJR)
decoded bits
Π
L'_{ext}
L'_{APP}
Channel
Receiver
from matched filter
from Interleaver
Successive Interference Canceller
soft output calc.
FTN mapper
Matched Filter
LLR calc.
to de-interleaver

Results: Receiver performance

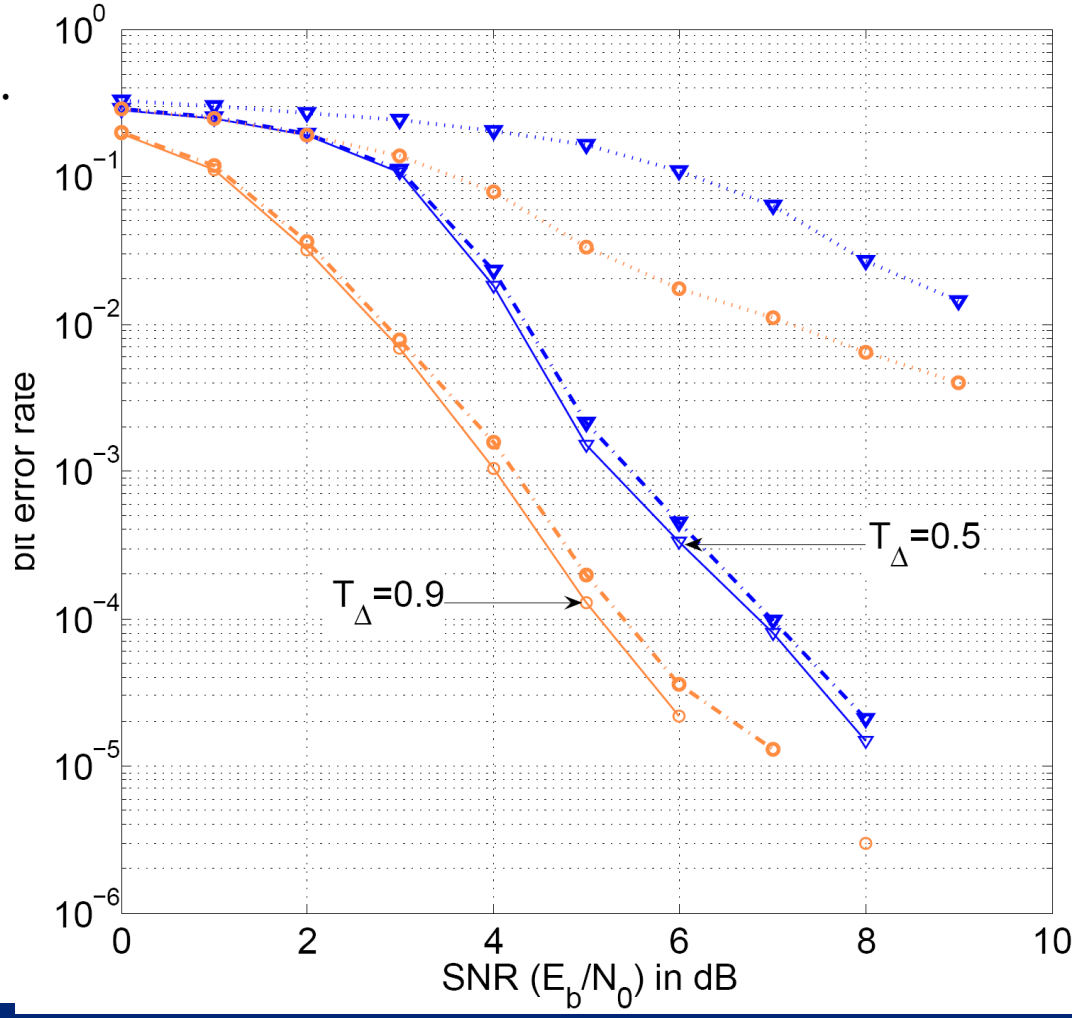
Receiver Performance at various time spacings.



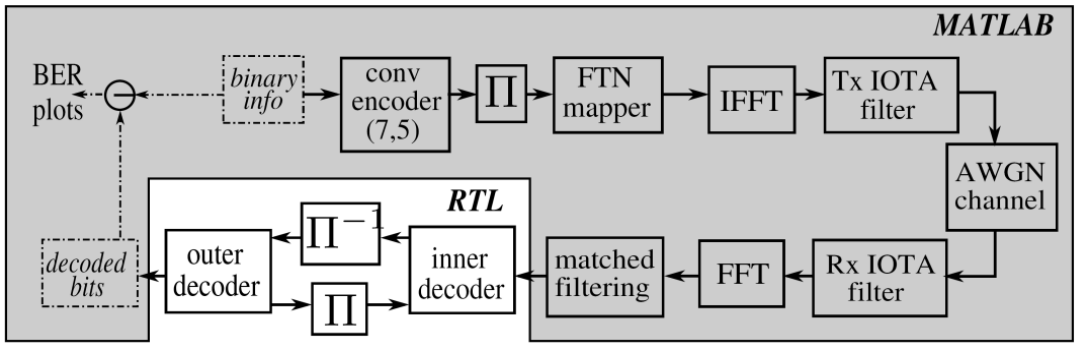
- ***2.5x improvement for the given system***

Fixed wordlength evaluation

- Transceiver model used to determine
  - wordlengths
    - 4, 6, 8 and 10 bits evaluated.
    - 8 bits minimum required.
  - no. of iterations : 8.
- Block size: 2016 symbols.
  - 3GPP interleaver.



Evaluating the implemented design

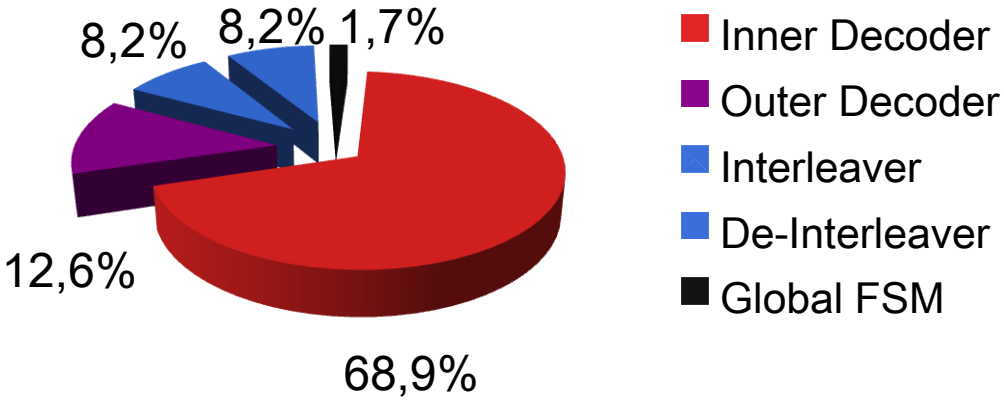


- Some degradation in RTL performance:
  - more averaging required.
  - 6 bit wordlength for outer decoder.
  - internal underflows.

- Consistent with simulation model.

Results: pre-optimization.

- Chip area : **0.519 mm^2** (~250k gate count ST 65nm standard cell CMOS)
  - 0.158mm^2 logic and 0.360 mm^2 memory (~17kB).
  - 64% of memory in Inner decoder.
- Estimated Power: **44mW** (80% in the memories)
- Speed and throughput: **3.2Mbps** at **300MHz**.



Conclusion

- A simulation model of the complete FTN transceiver realized.
  - to evaluate the performance.
  - explore design space for hardware implementation.
- Hardware architecture for the FTN system.
  - Implemented in 65nm CMOS (tapeout Nov!).
- Complexity overhead.
  - Memory : same order as a simple max-log-MAP implementation ((7,5) conv code).
  - Logic: ~5 times (time multiplexed resources: matched filter, FTN mapper)
- Higher bandwidth efficiency through FTN in practice.

Thank you!