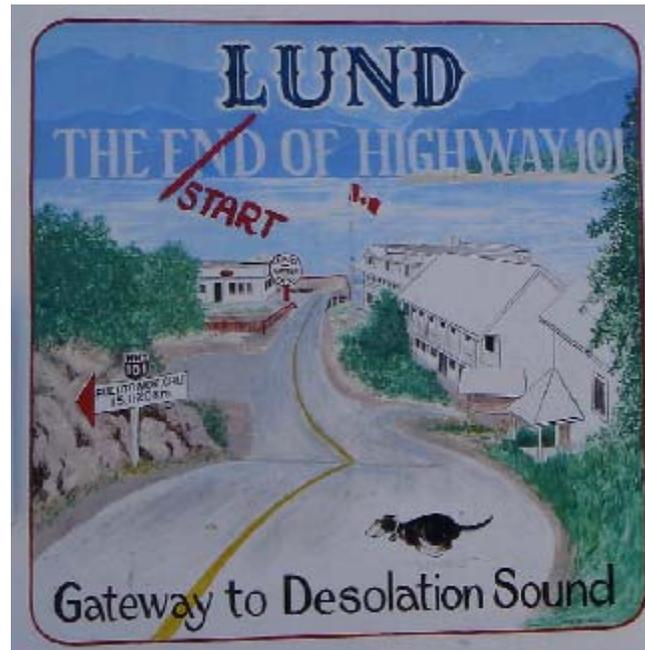


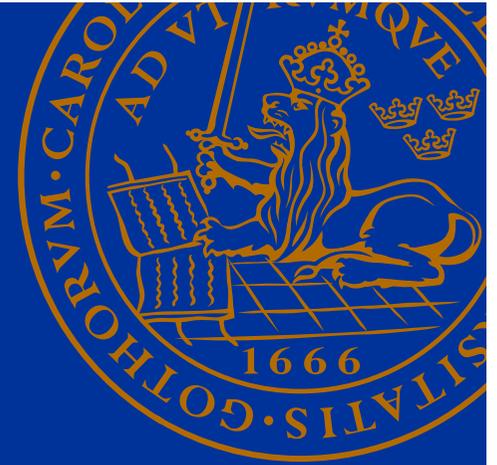


LUND
UNIVERSITY

Welcome to the



Lund Circuit Design Workshop
2010



Welcome and Introduction

Viktor Öwall

Dept. of Electrical and Information Technology

Lund University, Sweden

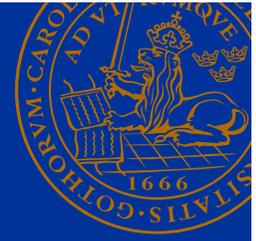
viktor.owall@eit.lth.se

Welcome to two exiting days



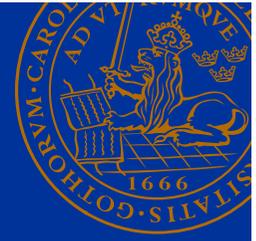
- A Lund University perspective by senior researchers and PhD students
- Invited speakers from academia:
 - Kofi A.A. Makinwa, TU Delft
 - Heiner Linke, Solid State Physics, Lund University
 - Andreas Jansson, ESS Scandinavia
- An industrial perspective:
 - Dag T. Wisland, Novelda AS
 - Lars Risbo, TI Denmark
 - Sami Vilhonen, ST Ericsson Finland
- Social activities including: The Dinner

Some Logistics!



- Today's program is at Grand Hotel including Lunch.
- Dinner in the Main Building of Lund University.
- Tomorrow's programs is at the Faculty of Engineering, Lund University.

Some Logistics!

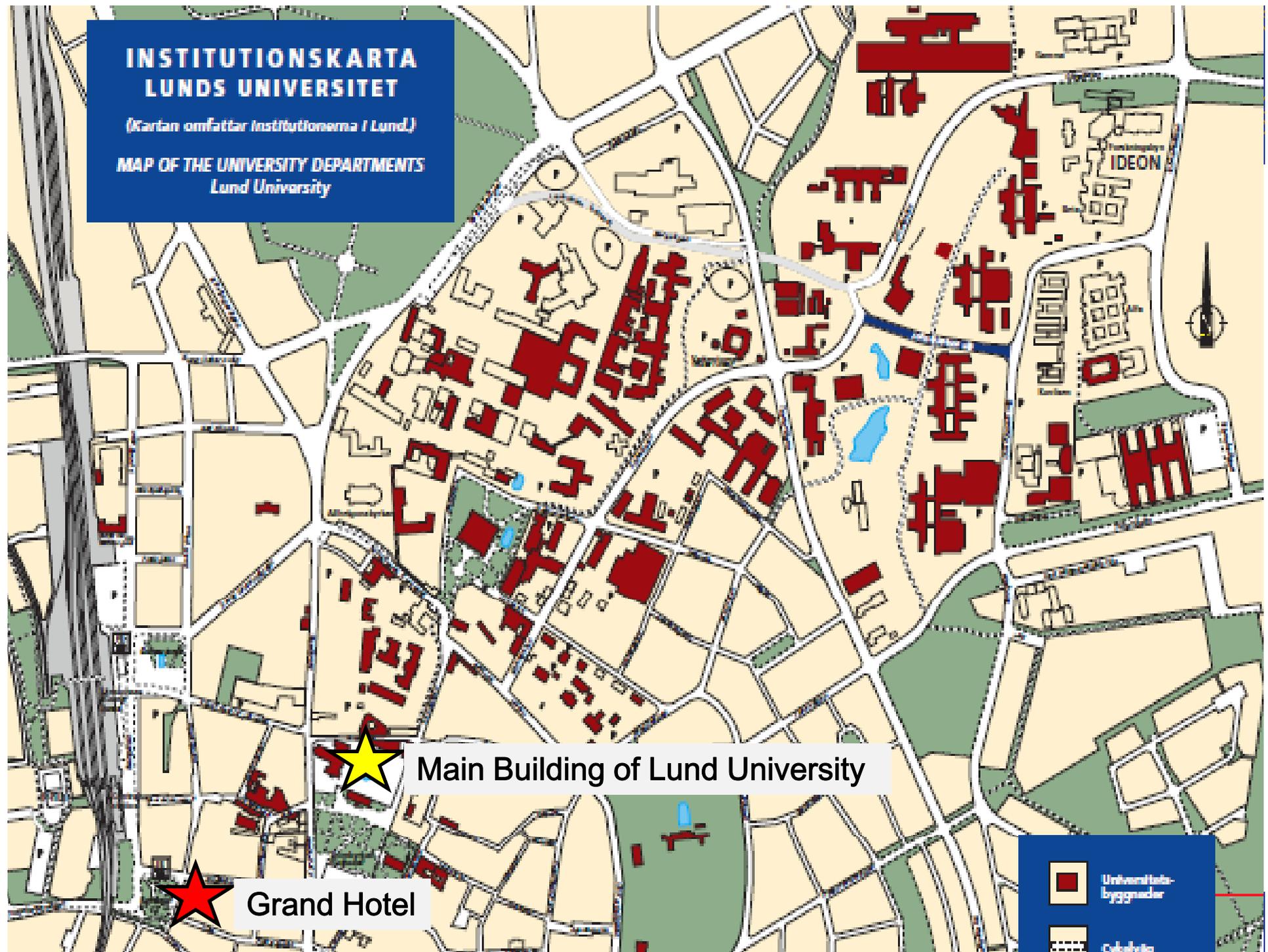


- Today's program is at Grand Hotel including Lunch.
- Dinner in the Main Building of Lund University.
- Tomorrow's programs is at the Faculty of Engineering, Lund University.

INSTITUTIONSKARTA LUNDS UNIVERSITET

(Kartan omfattar institutionerna i Lund.)

MAP OF THE UNIVERSITY DEPARTMENTS
Lund University



Grand Hotel

Main Building of Lund University

- Universitetsbyggnader
- Cykelväg

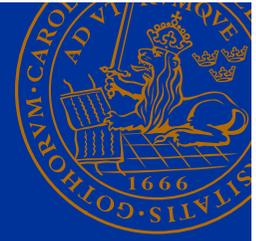
Dinner : Main Building of Lund University



2010-09-22

Lund Circuit Design Workshop 2010

Some Logistics!



- Today's program is at Grand Hotel including Lunch.
- Dinner in the Main Building of Lund University.
- Tomorrow's programs is at the Faculty of Engineering, Lund University.

INSTITUTIONSKARTA LUNDS UNIVERSITET

(Kartan omfattar institutionerna i Lund.)

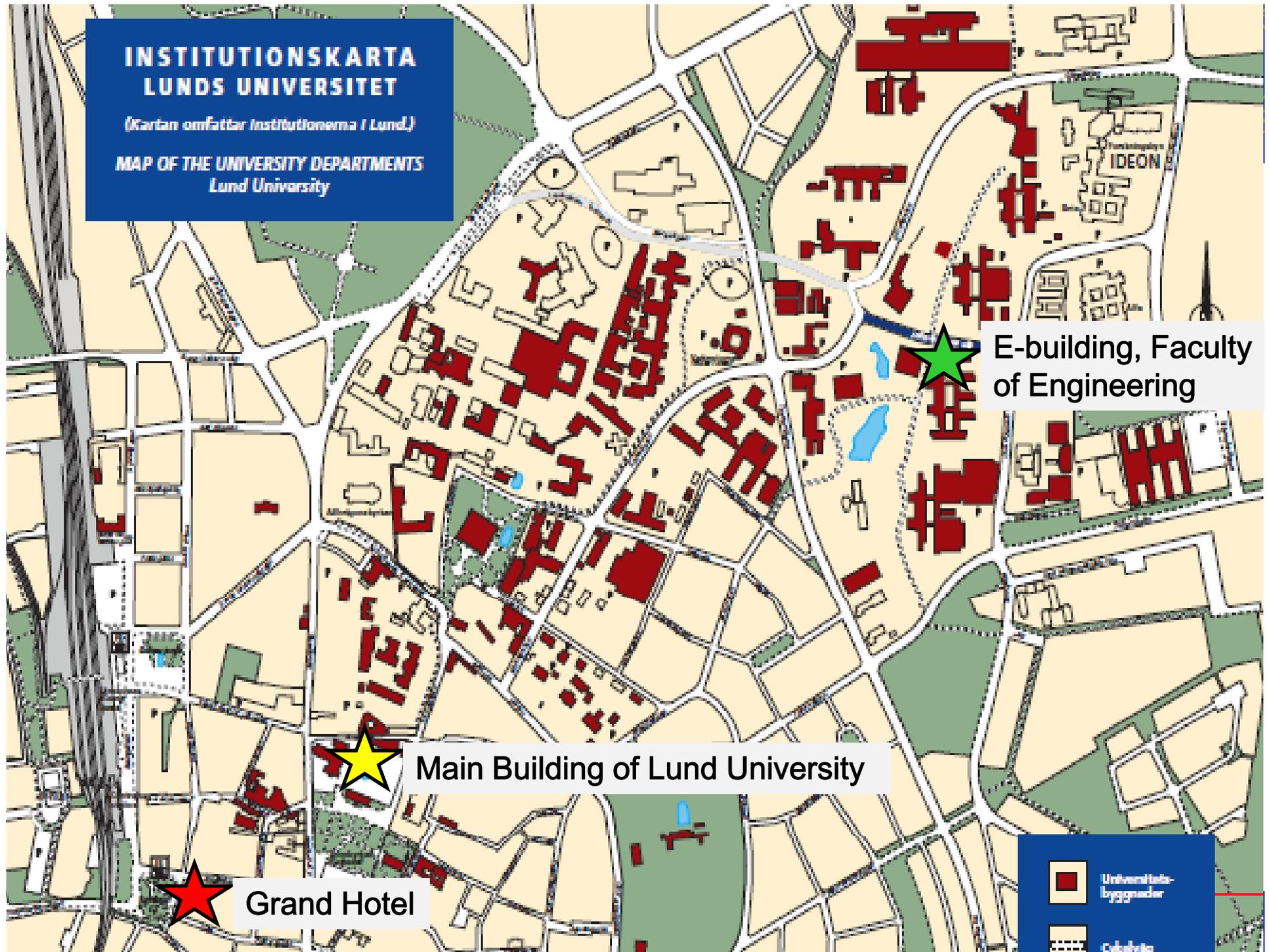
MAP OF THE UNIVERSITY DEPARTMENTS
Lund University

★ E-building, Faculty of Engineering

★ Main Building of Lund University

★ Grand Hotel

■ Universitetsbyggnader
--- Cykelväg



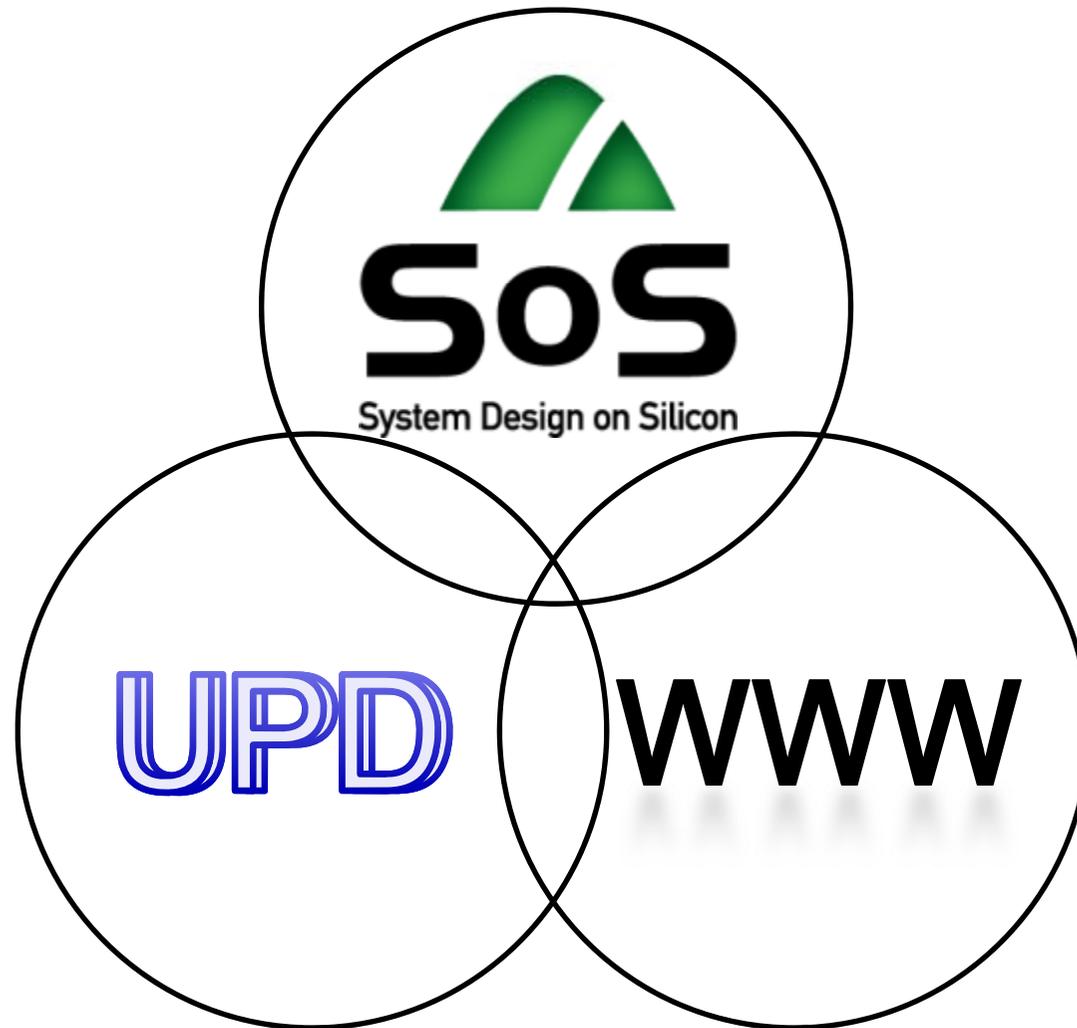
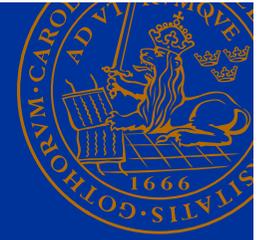
E-building: faculty of Engineering



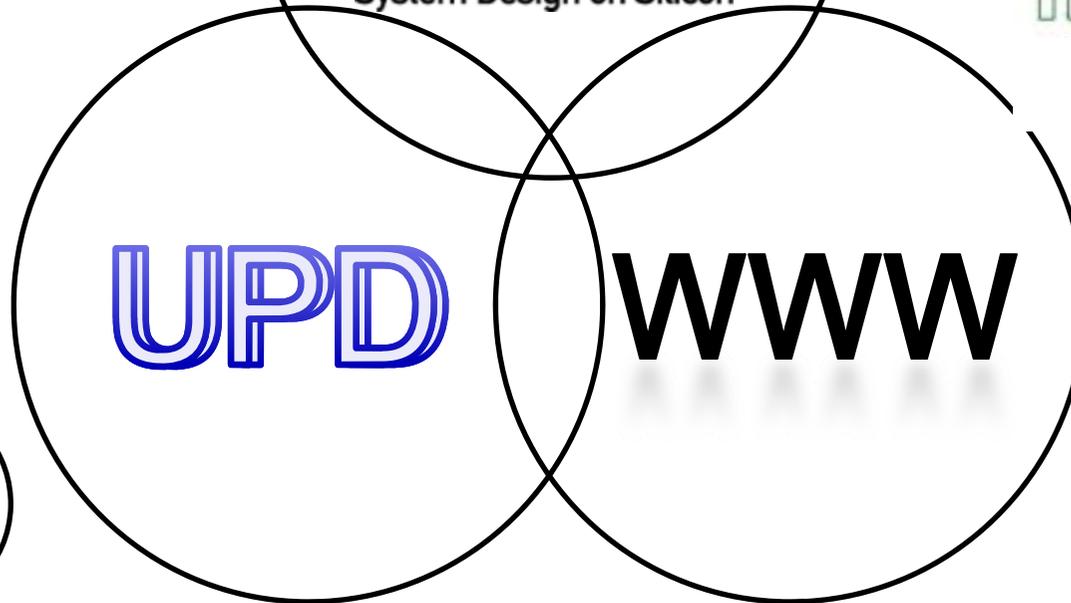
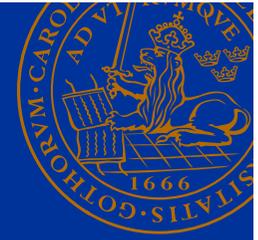
2010-09-22

Lund Circuit Design Workshop 2010

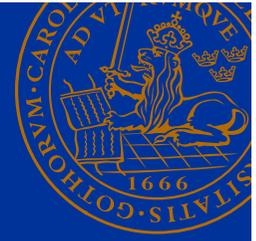
The hosts



Funding and Initiatives

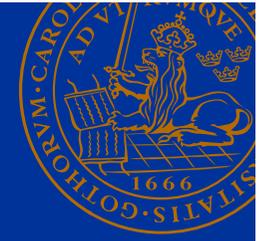


Strategic Research Funds: ELLIIT

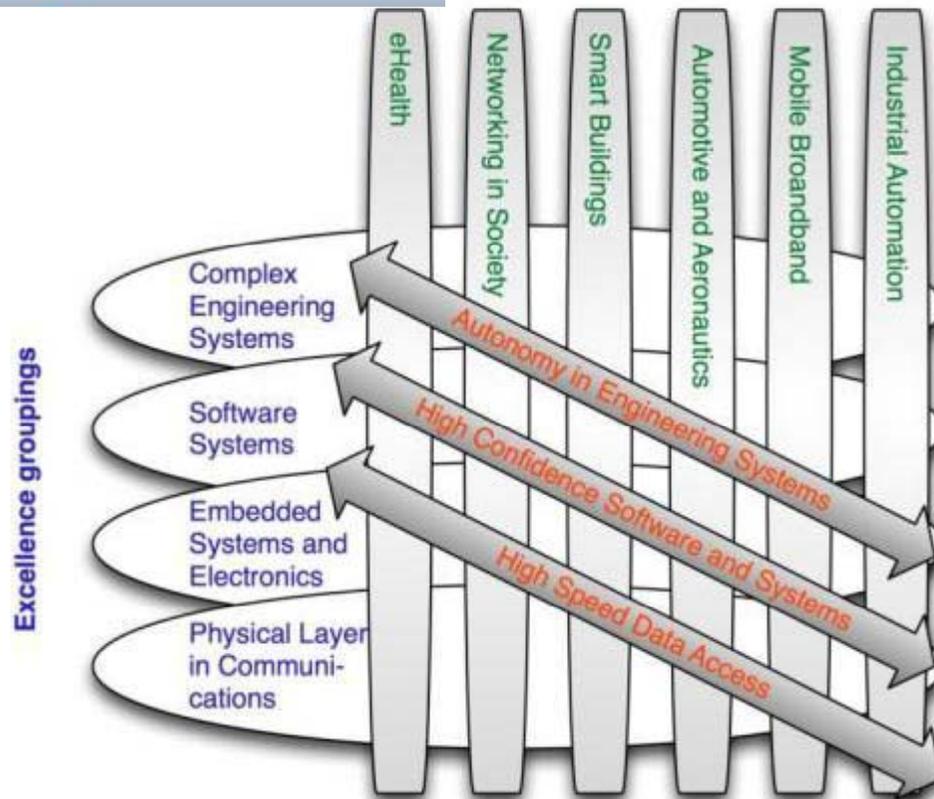


ELLIIT is a network organization for Information and Communication Technology (ICT) which has been created to support and enhance an internationally acknowledged research environment in these areas. It is organized within the Swedish government's strategic research support initiative.

Strategic Research Funds: ELLIIT

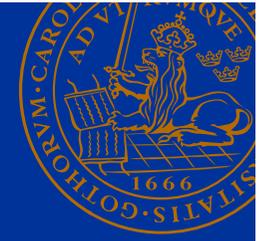


Application areas



ELLIIT:

1. is headed by Lennart Ljung from Linköping University. Co-director John B. Anderson Lund University.
2. partners are at Linköping, Lund, Halmstad and Blekinge,.
3. covers "all" aspects of ICT.
4. embedded systems and Circuit Design is an important part of the initiative.

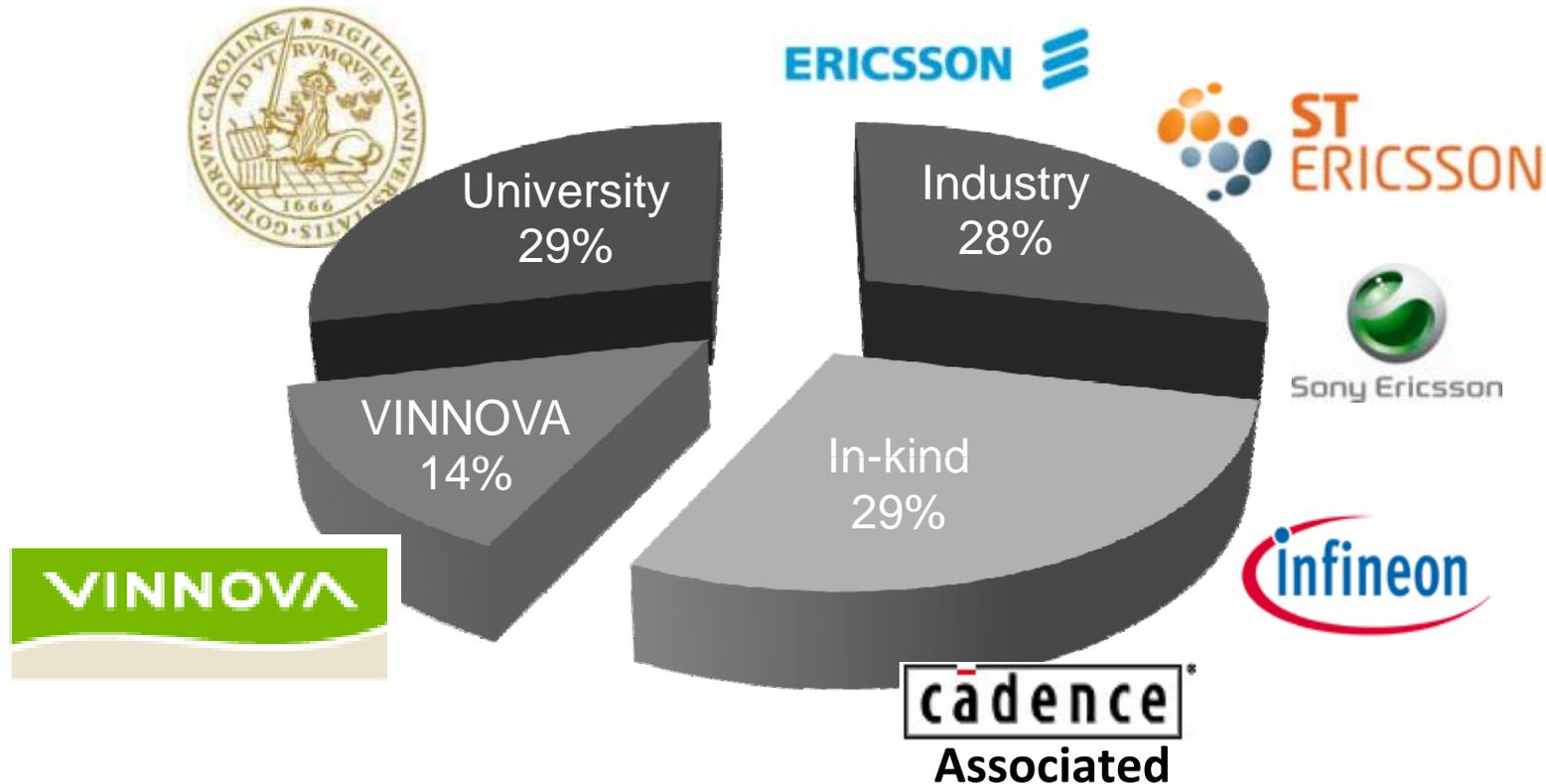


VINNOVA Industrial Excellence Center in



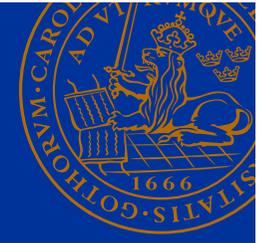
has the vision to be a **world class research facility** for the development of **system solutions on silicon for wireless communication devices** that ensure the competitiveness of the participating companies.

VINNOVA Industrial Excellence Center in System Design on Silicon



**Budget approximately 14.5MSEK/year including in-kind.
Ongoing discussions with several other companies.**

Some Results



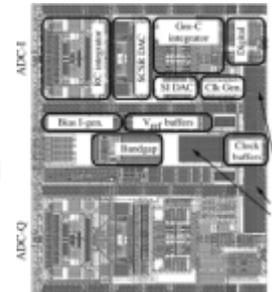
Academic output:

- Six PhD degrees.
- 16 journal papers (primarily in IEEE journals).
- 28 papers at international peer reviewed conferences.

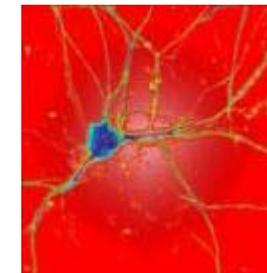


Some Technology transfers:

- A novel A/D-converter is currently used by SoS industrial partners. The work was performed by Martin Anderson as a CCCD/SoS PhD student. Martin is now employed at Ericsson Research in Lund.



- During our previous center, CCCD, a digital holographic microscope was developed which is now a start-up company.



People in SoS



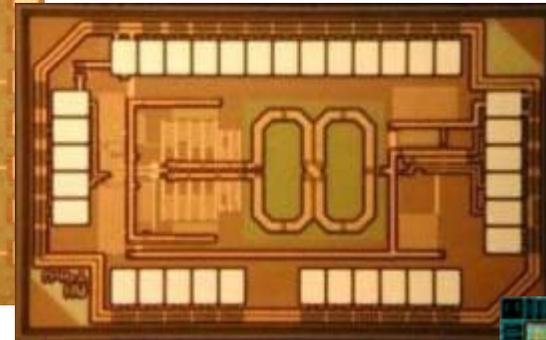
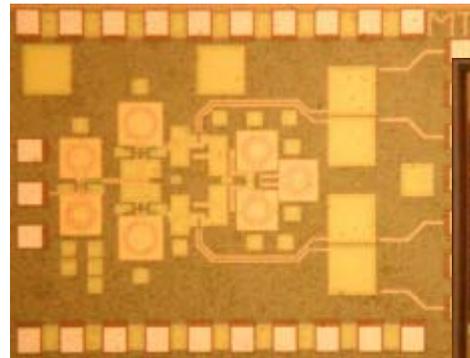
Director: Viktor Öwall, Co-director: Pietro Andreani
Chairman of the Board: Sven Mattisson, Ericsson AB



International Advisory Board

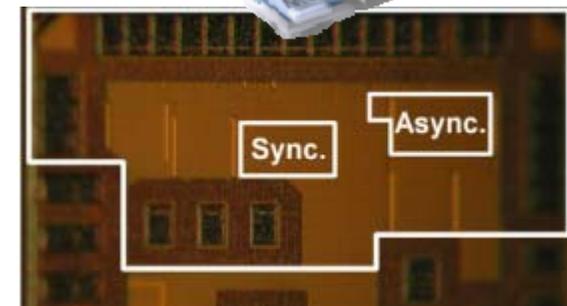
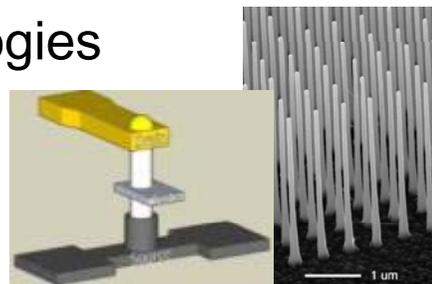
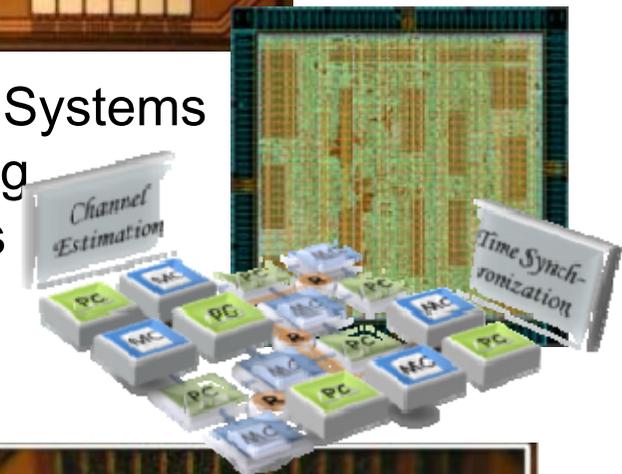
- Professor Jan Rabaey, BWRC, UC Berkeley, USA
- Professor Mike Faulkner, Victoria University, Australia
- Professor Qiuting Huang, ETH, Zürich, Switzerland

Research projects in SoS



Ongoing projects:

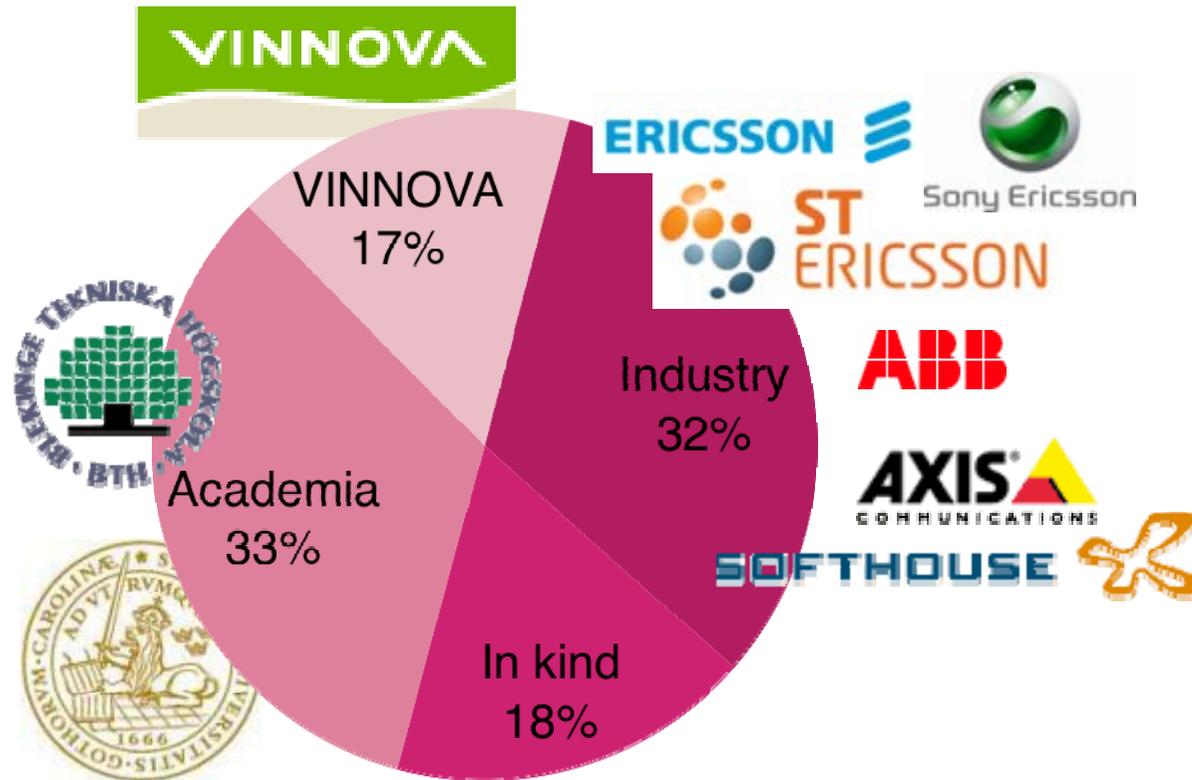
- Switched Mode RF Transmitters
- Microwave and mm-Wave CMOS Circuits and Systems
- Transmitters with adaptive impedance matching
- High-Performance CT Delta-Sigma Modulators
- VCOs and Very-Low-Power Radio Front-ends
- Reconfigurable Computing
- Low Leakage Arithmetic and Architectures
- Future/emerging technologies



EASE – the sister center



EASE - Embedded Applications Software Engineering



**Budget approximately 10.5MSEK/year including in-kind.
Director: Per Runeson, Dept. of Computer Science**

Research within EASE



Collaboration with SoS regarding mapping to reconfigurable architectures.

Themes

A: Flexible Software Architectures

B: Parallel Embedded Systems

C: Efficient Software Methods
(OSS, Agile)

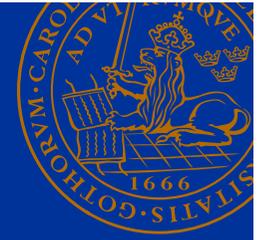
D: Aligning Requirements and
Verification

Technology/Tools



Engineering/People

Mobile Heights



Mobile Heights is an industry-driven cluster initiative that gather top companies and universities, as well as regional and national agencies, to finance applied research and innovation in mobile communications business.



LUNDS UNIVERSITET



MALMÖ HÖGSKOLA



Mobile Heights – The environment

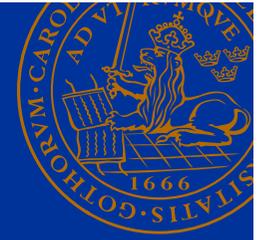


Mobile Heights is located in Southern Sweden, one of Europe's most dense and specialized geography on mobile communications and ICT.

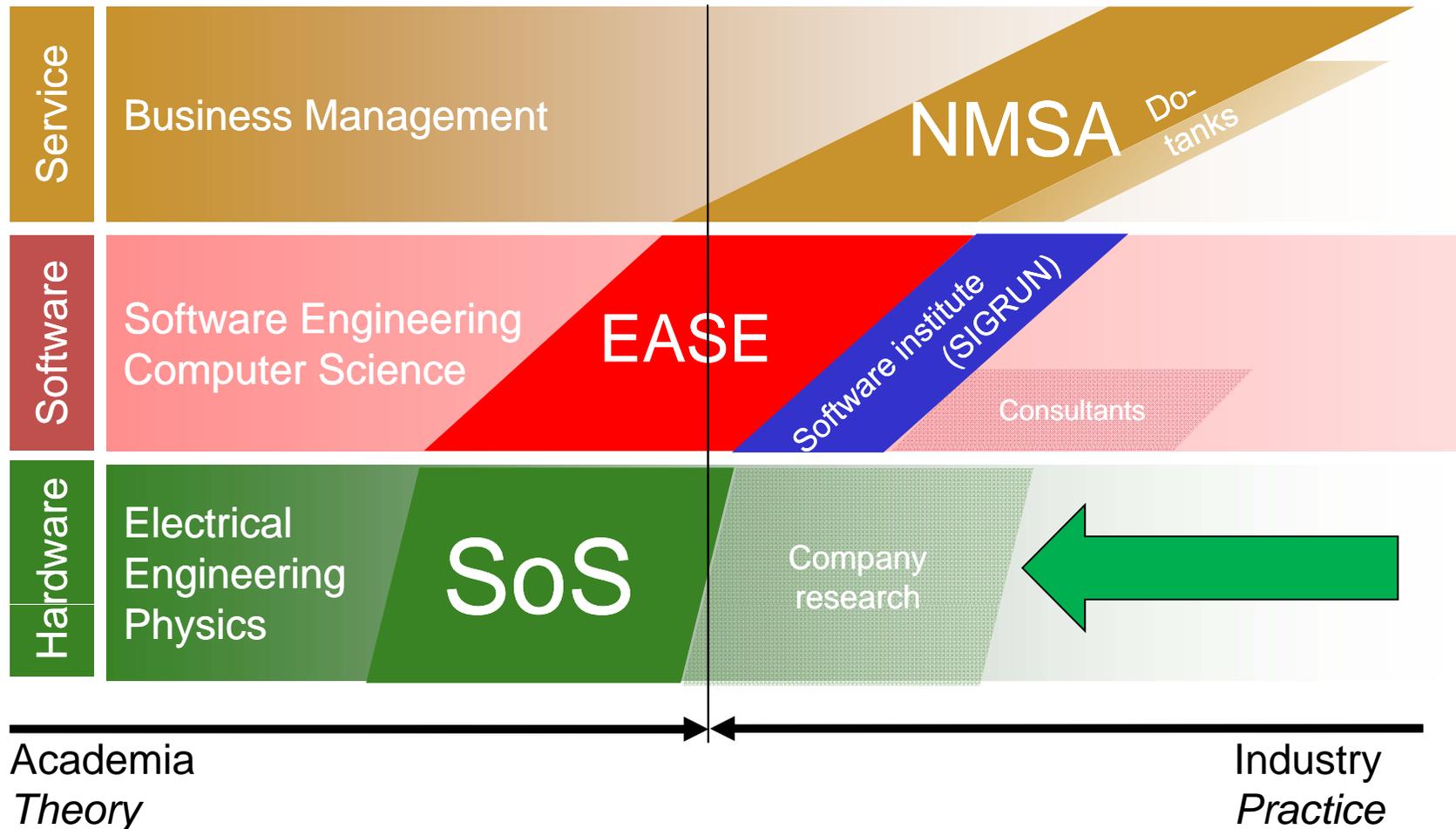
A European mobile handset hotspot!

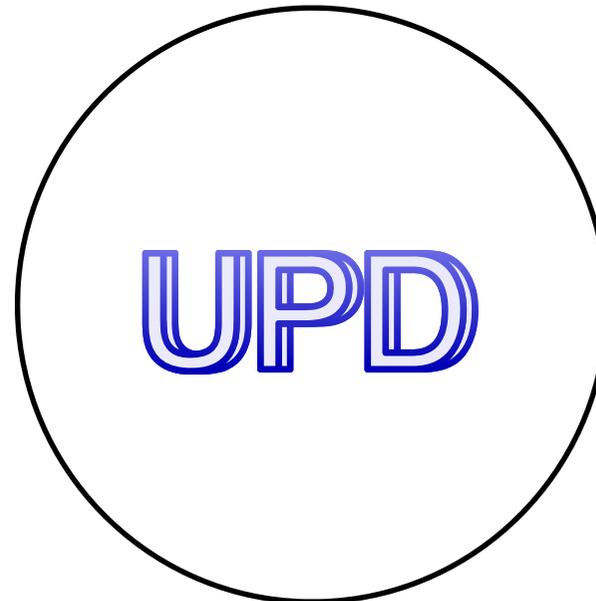
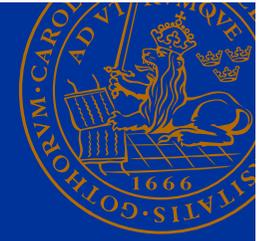
- 100 000 employees in ICT, 7 000 working in mobile
- 12 000 companies, 2 000 companies in mobile
- 500 public researchers within ICT
- 8 000 students within ICT

Research and innovation



And a business arena to pilot Open Innovation principles:
MHBC – Mobile Heights Business Center





SSF strategic grant in



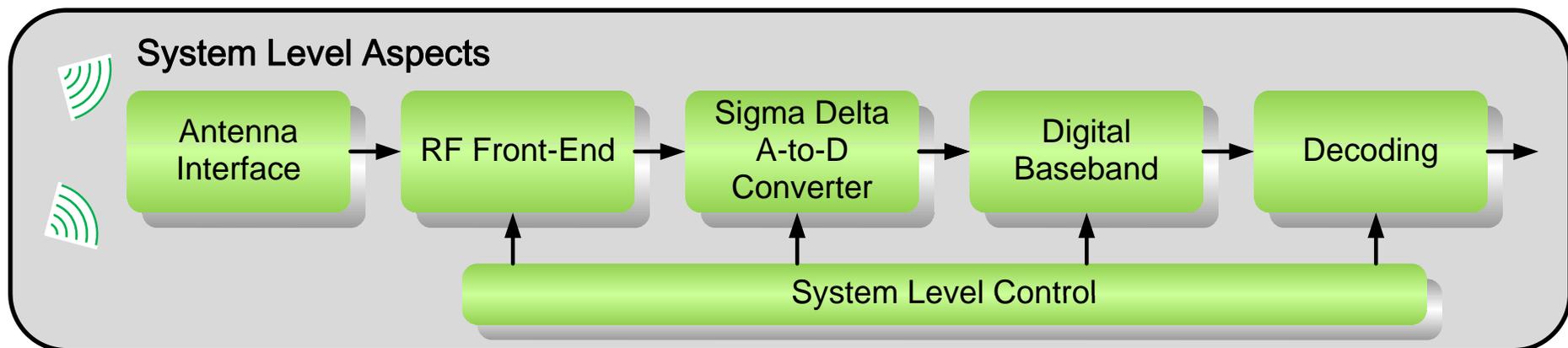
Wireless Communication for Ultra Portable Devices

UPD: Wireless Communication for Ultra Portable Devices



SSF Project granted in summer of 2008.
Main applicant: Henrik Sjöland
Financing: 22.4MSEK over 5 years

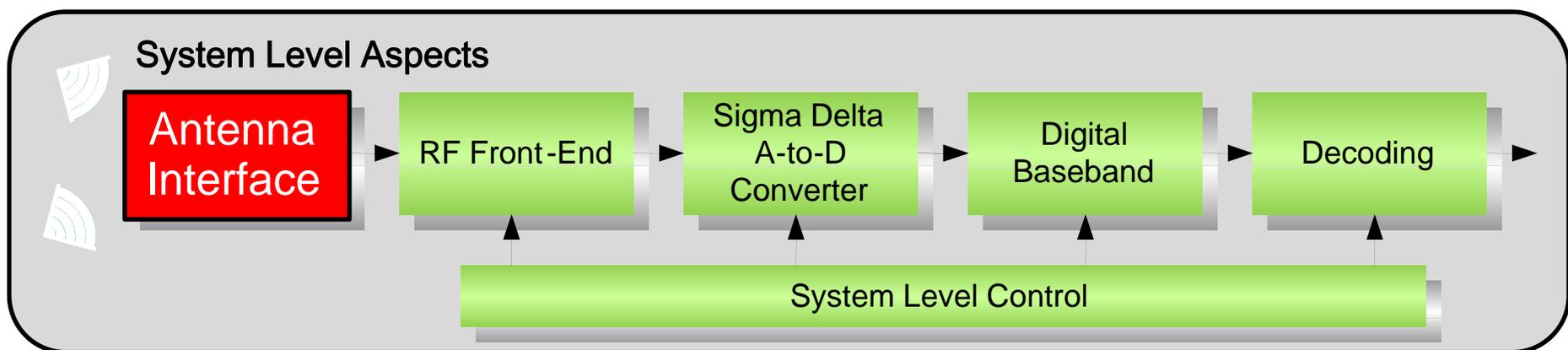
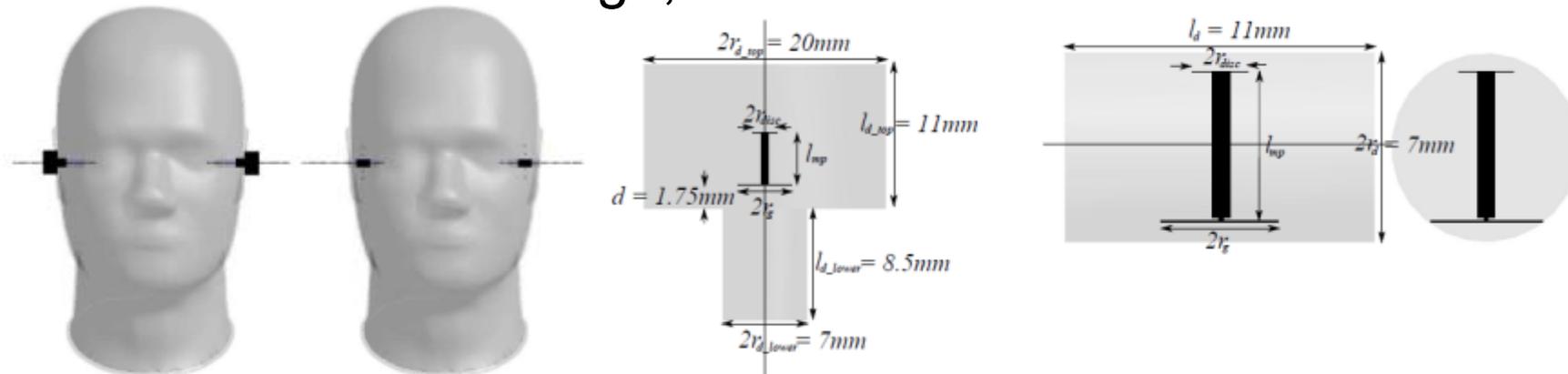
The main goal of this project is to design an ultra compact and low power radio that can be used in devices like hearing aids, medical implants, and remote sensors.



UPD: some results



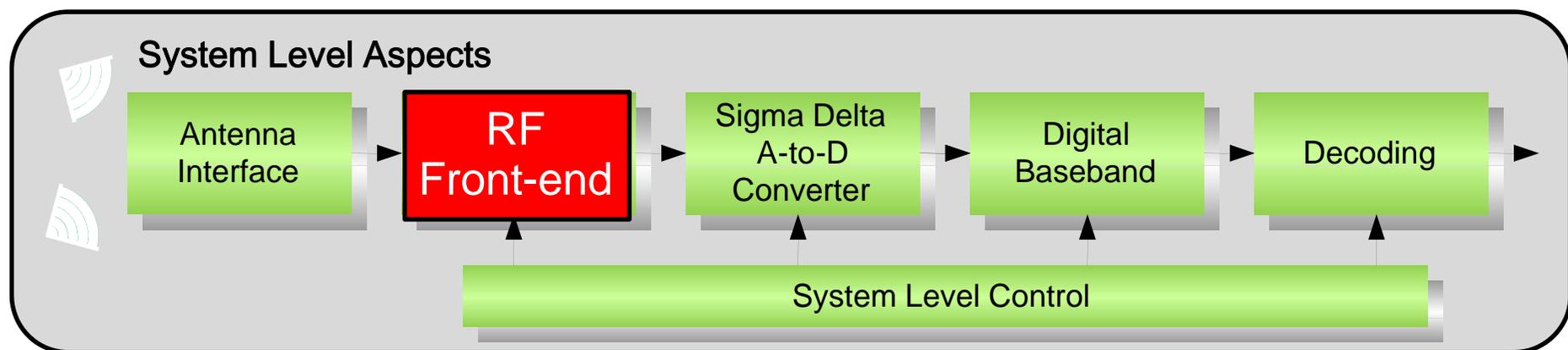
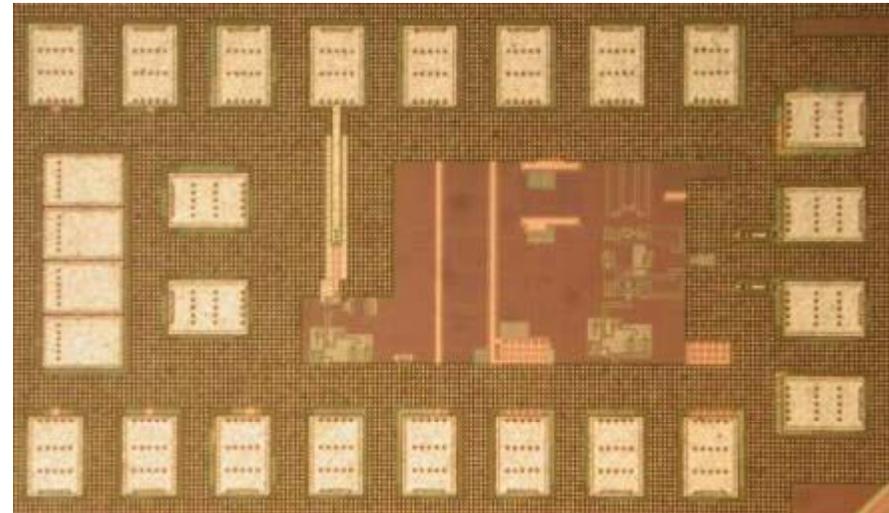
Antenna Design; In-the-ear and in-the-canal



UPD: some results



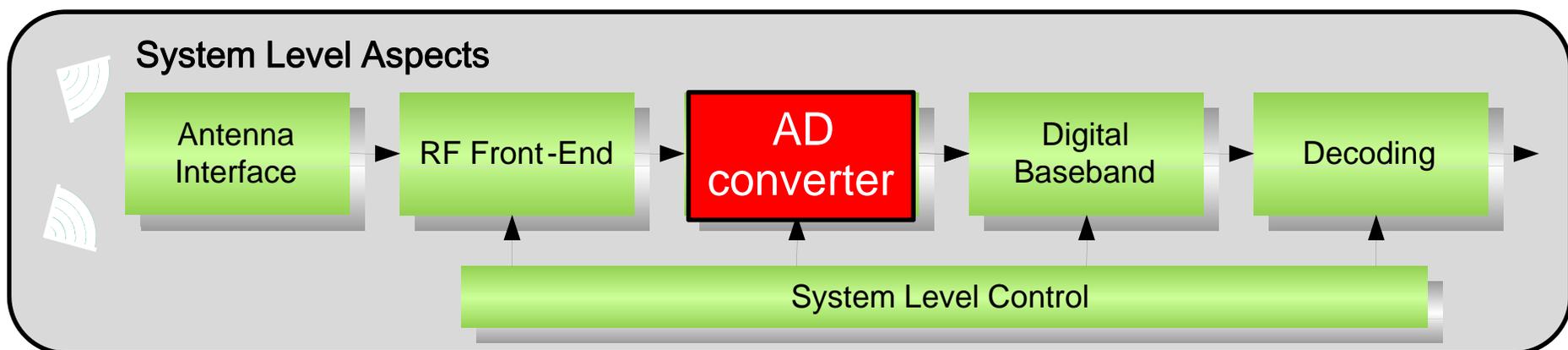
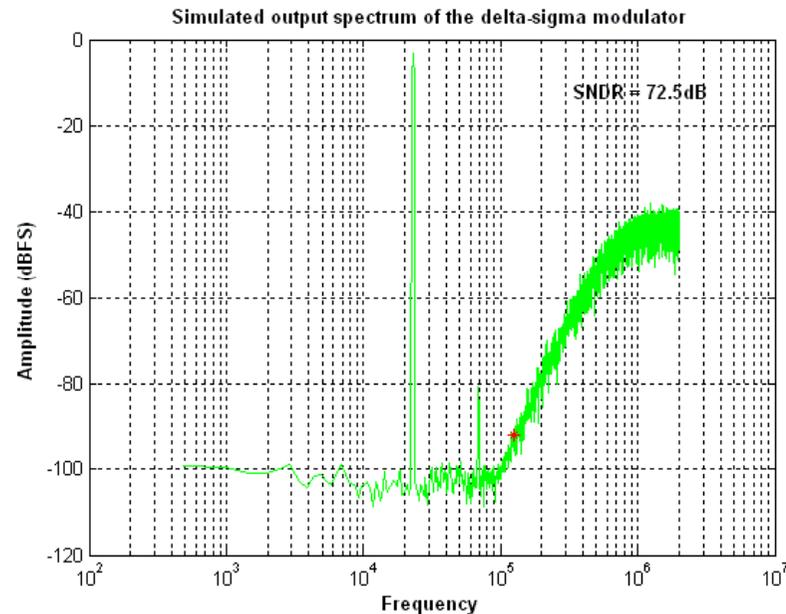
- LNA + frequency divider + mixer
- ST 65nm CMOS
- expected power cons. <math>< 300\mu\text{W}</math>



UPD: some results

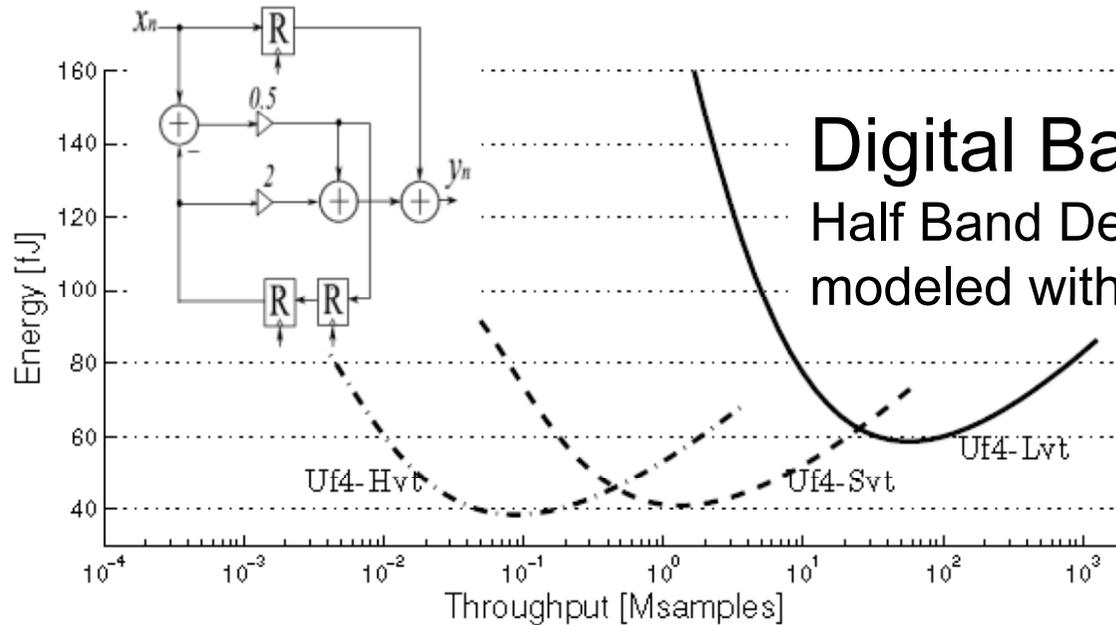


Simulated spectrum for the output signal from the delta-sigma modulator with SNDR calculated.

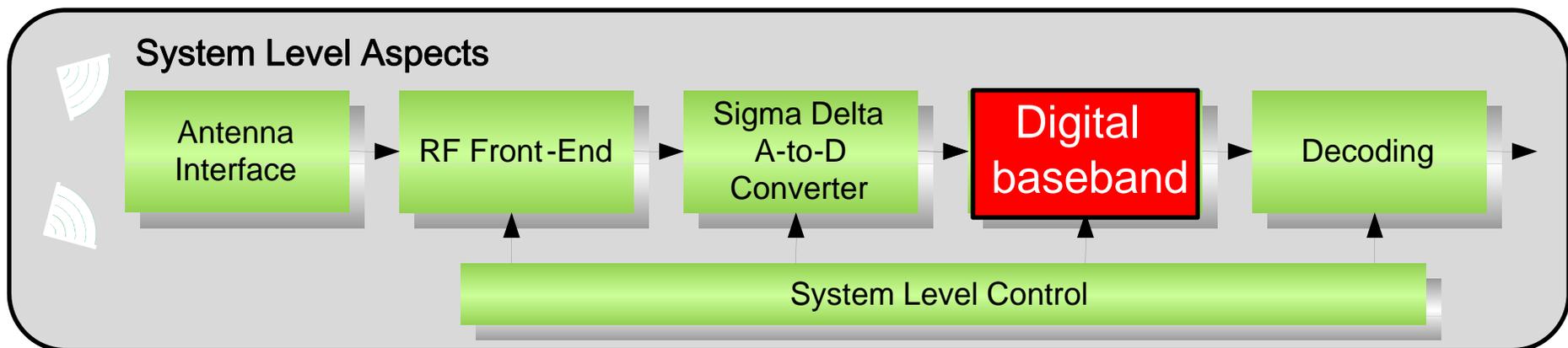




UPD: some results



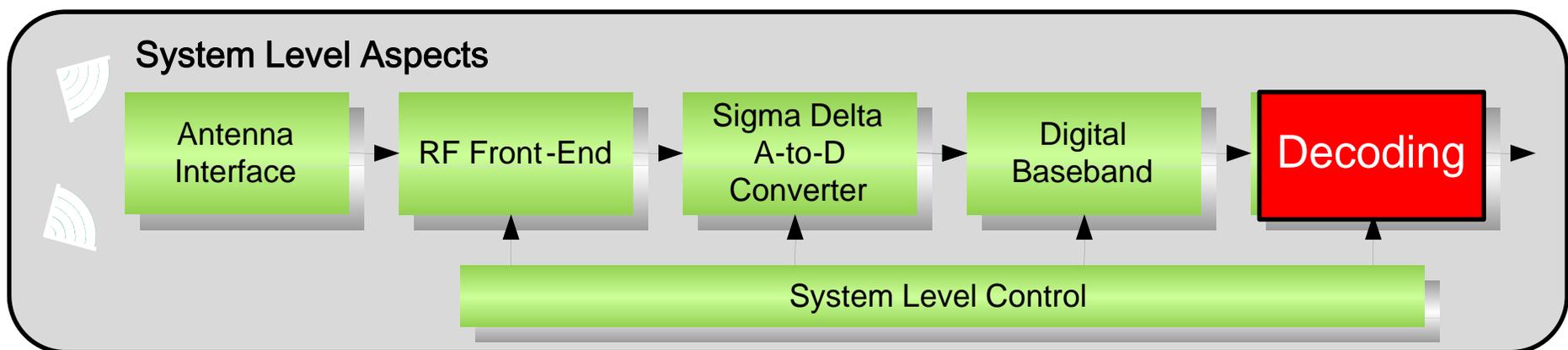
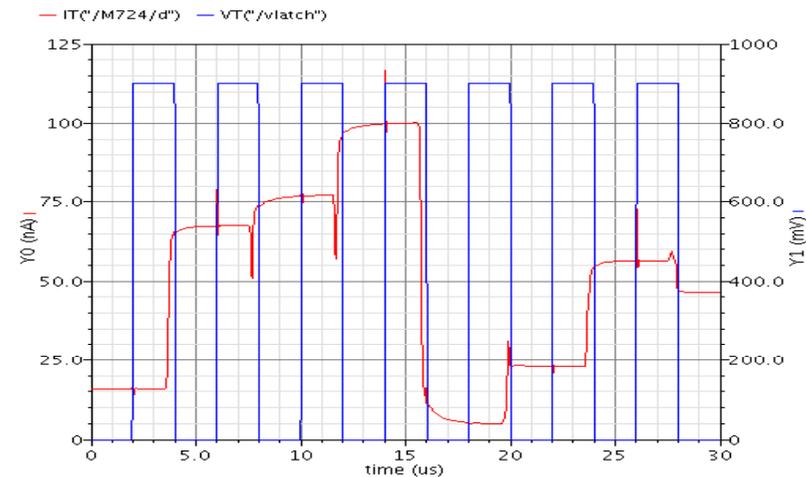
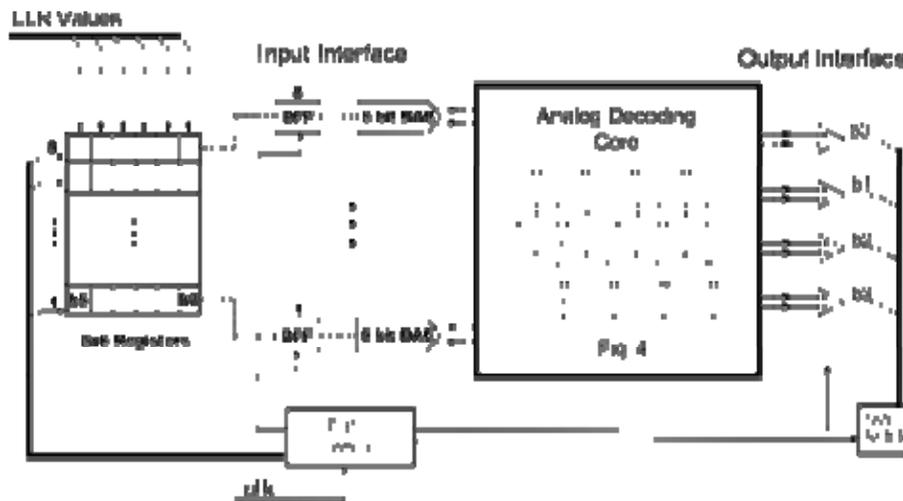
Digital Baseband in Sub-Vt:
Half Band Decimation Filter Chain,
modeled with various architectures.



UPD: some results



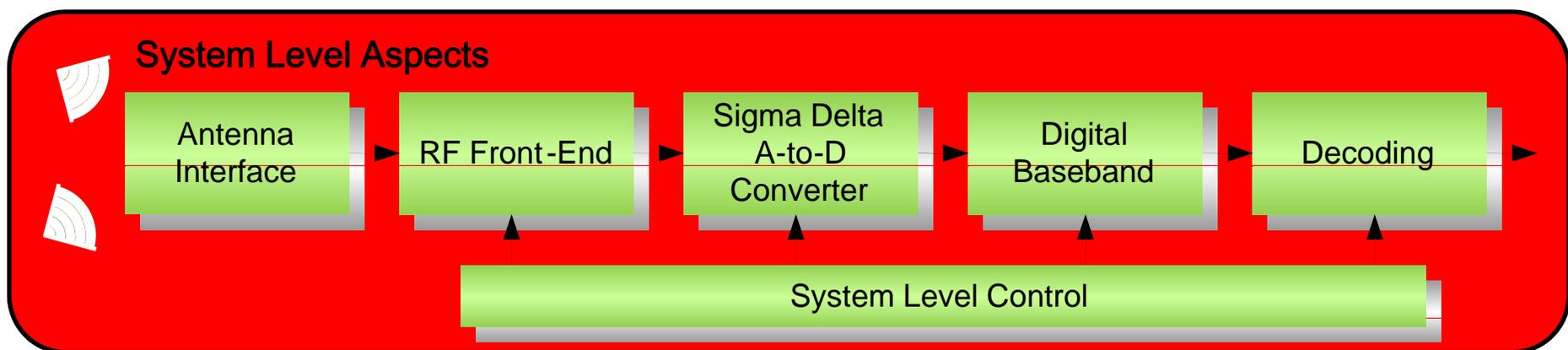
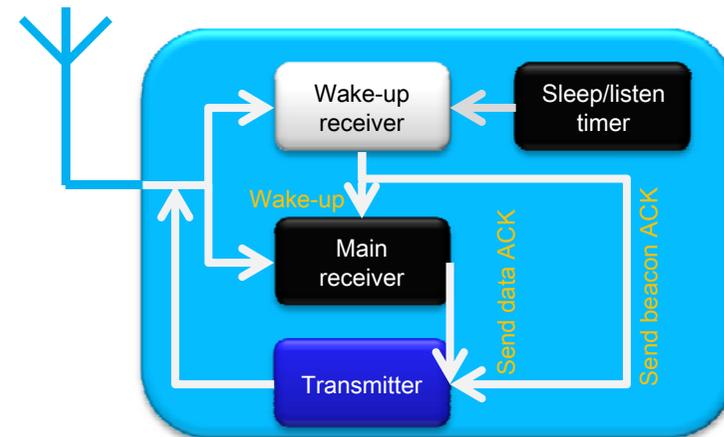
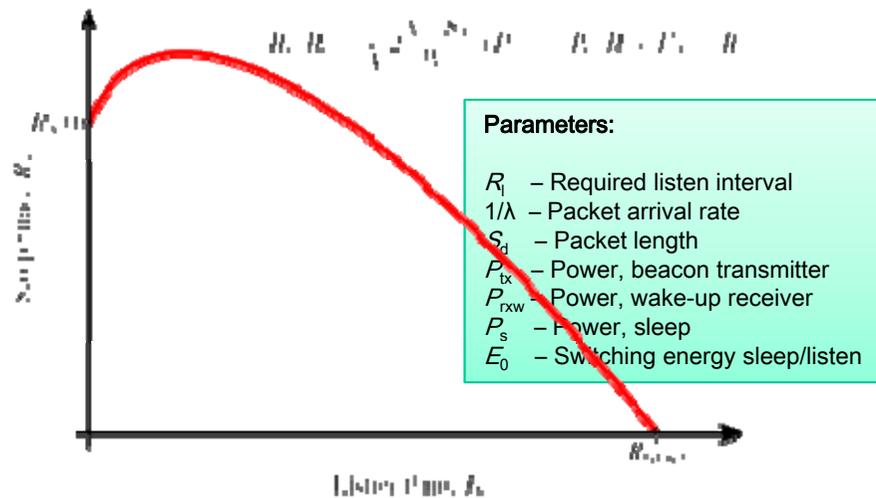
Analog decoder in a digital environment.

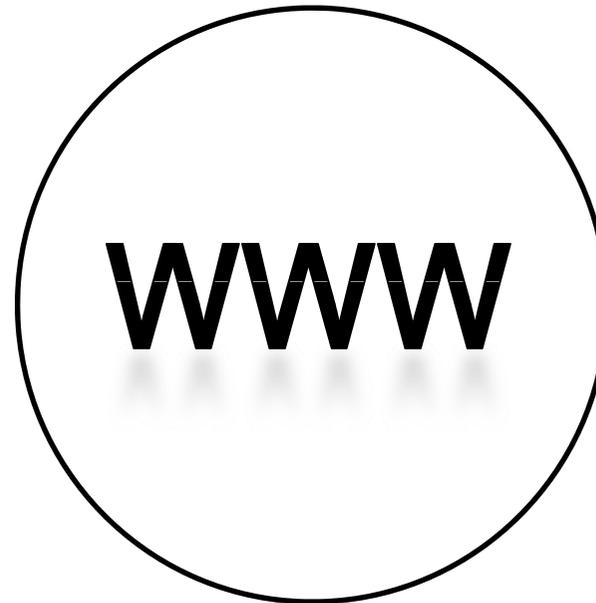
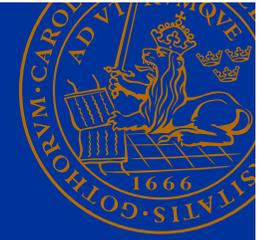


UPD: some results



Finding the minimal total energy/packet





SSF strategic grant in



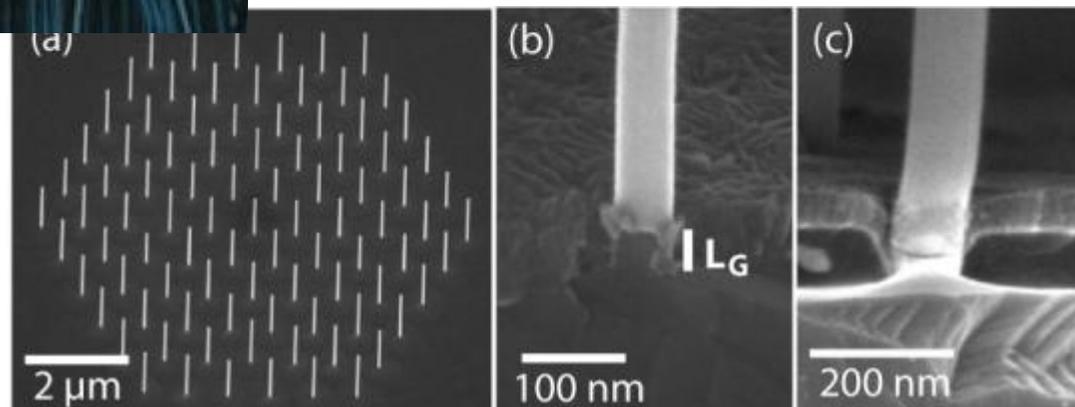
Wireless with Wires

WWW: Wireless with Wires

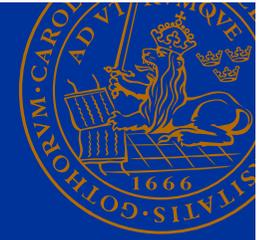


SSF Project granted in summer of 2008.
Main applicant: Lars-Erik Wernersson
Financing: 24MSEK over 5 years

Interdisciplinary research between device physics and circuit design. Transistor and circuits at the end of the ITRS roadmap are considered using nanowire transistors.

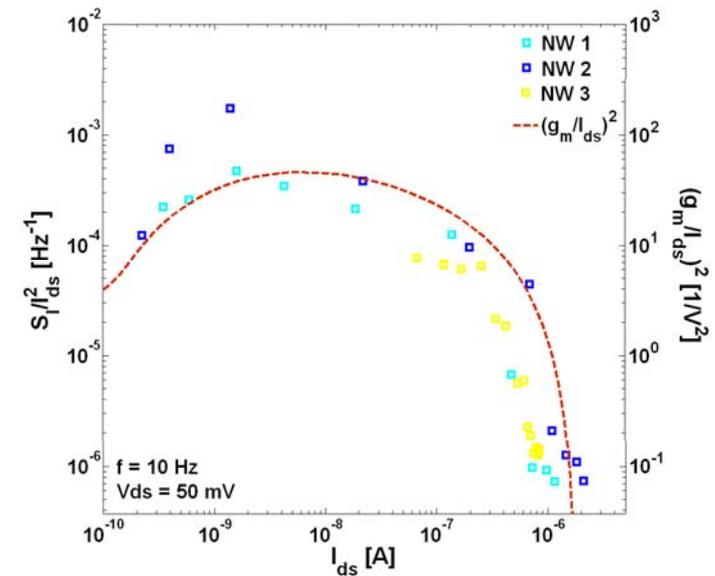
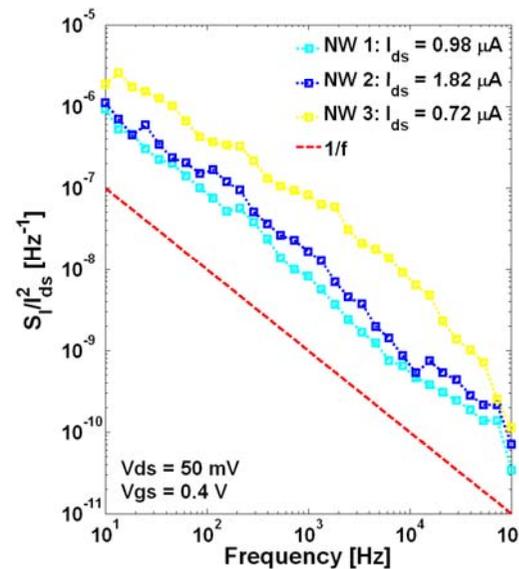
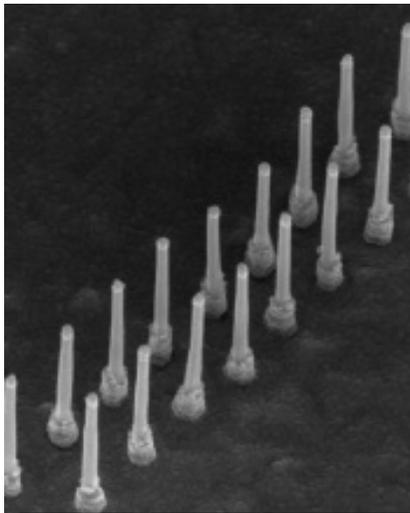


Results: WWW

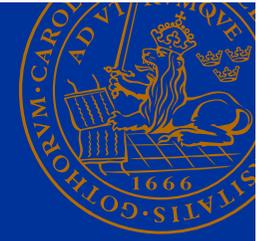


DC and 1/f-noise performance of 35 nm L_g individual InAs nanowire transistors

First result of noise characteristics for III-V MOSFETs
Correlated number-mobility fluctuation

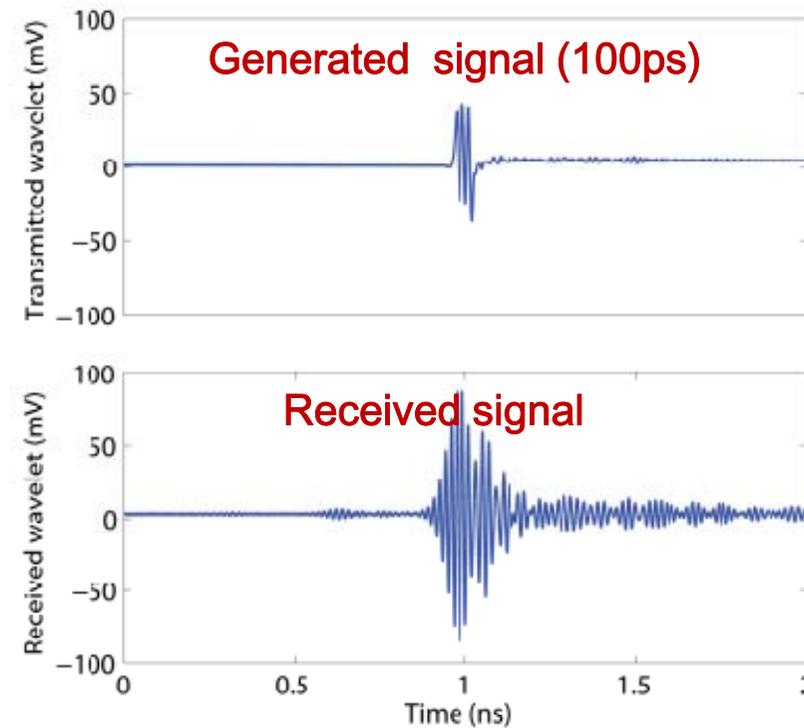
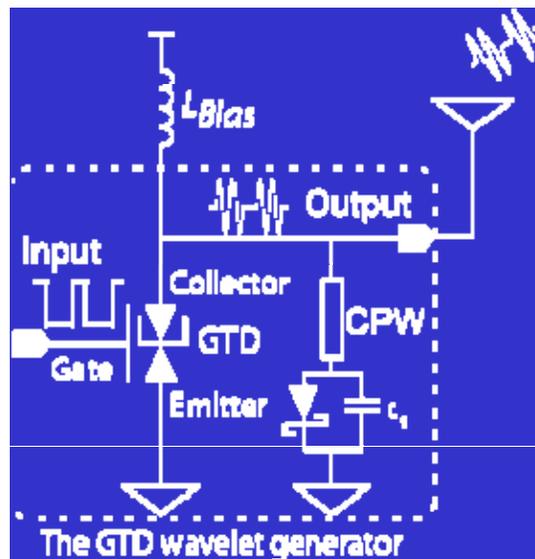


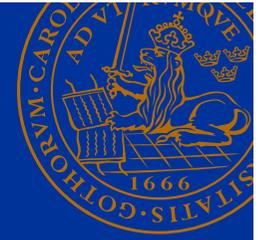
Results: WWW



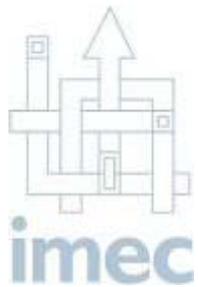
60 GHz pulse generators in TX-RX configuration over air interface.

12.5 Gbps demonstration!





Multibase: January 2008 – April 2011



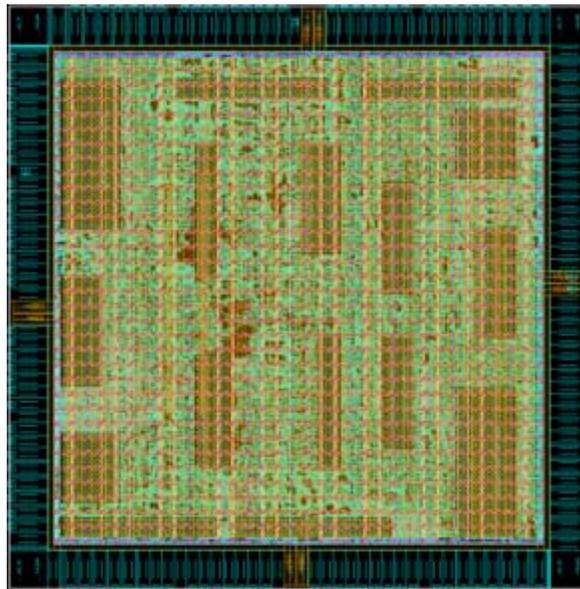
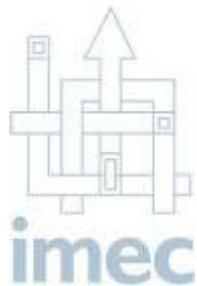
Scalable Multi-tasking Baseband for Mobile Communications

1. Multi-streaming radio (concurrent execution of multiple standards)
2. Scalable programmable/reconfigurable multi-processor technology
3. Algorithm/architecture co-design for maximum energy efficiency

LU Focus: Synch and Channel Estimation, algorithms and architectures.

Multibase: January 2008 – April 2011

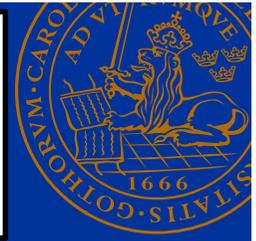
ERICSSON 



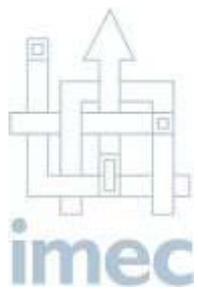
Status:

- Complete DFE Rx taped out in June.
- Samples are expected soon.
- Infineon 65nm CMOS
- Chip area 5mm²
- Core area 3.5mm²

FP7 STREP DRAGON



Project started in January 2010 for 3 years.



ERICSSON



TU
Graz



Disruptive Radio Architectures Going Nanoscale

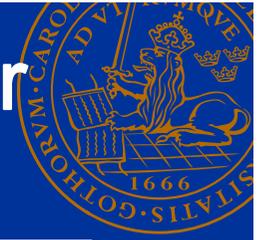
1. Innovative receiver architectures.
2. CMOS power amplifiers that double TX efficiency.
3. Reconfigurable radios with no overhead.
4. Ultimately, new concepts/methodologies pushing the A/D converter closer to the antenna -
The holy grail of fully digital radio receivers.



Sven Mattisson
Ericsson



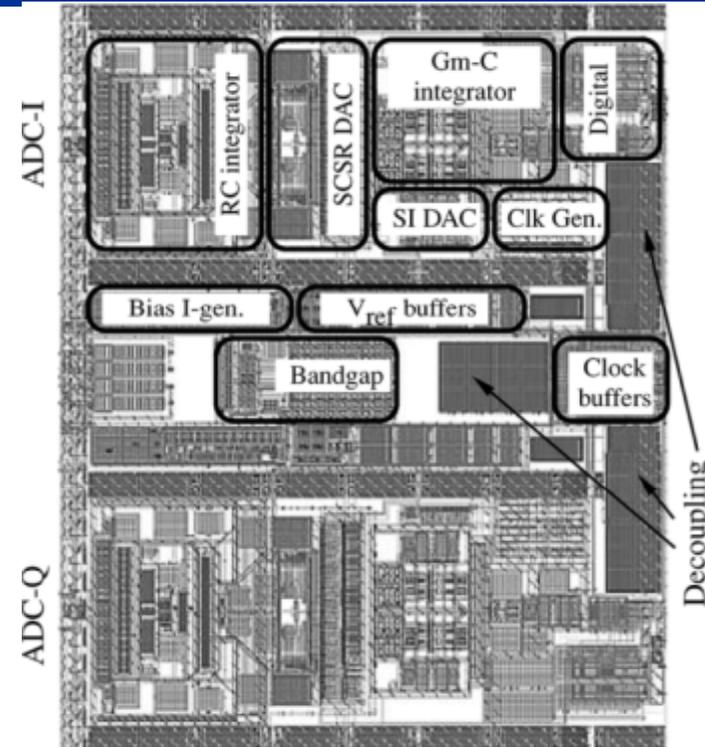
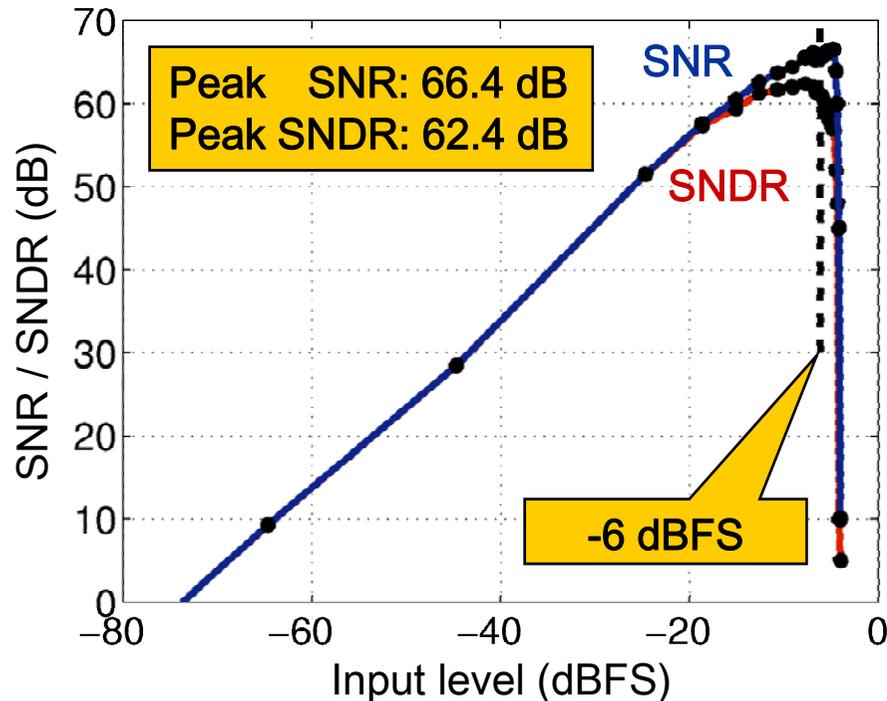
And now to some
more achievements!



New Switched-Capacitor Switched-Resistor CT $\Delta\Sigma$ modulator with low jitter sensitivity

Currently being used by SoS industrial partners!

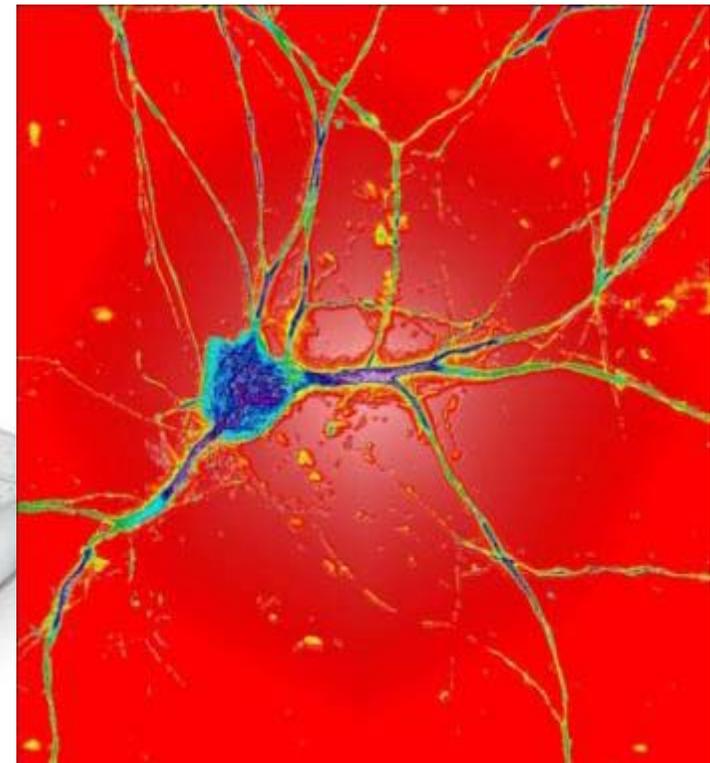
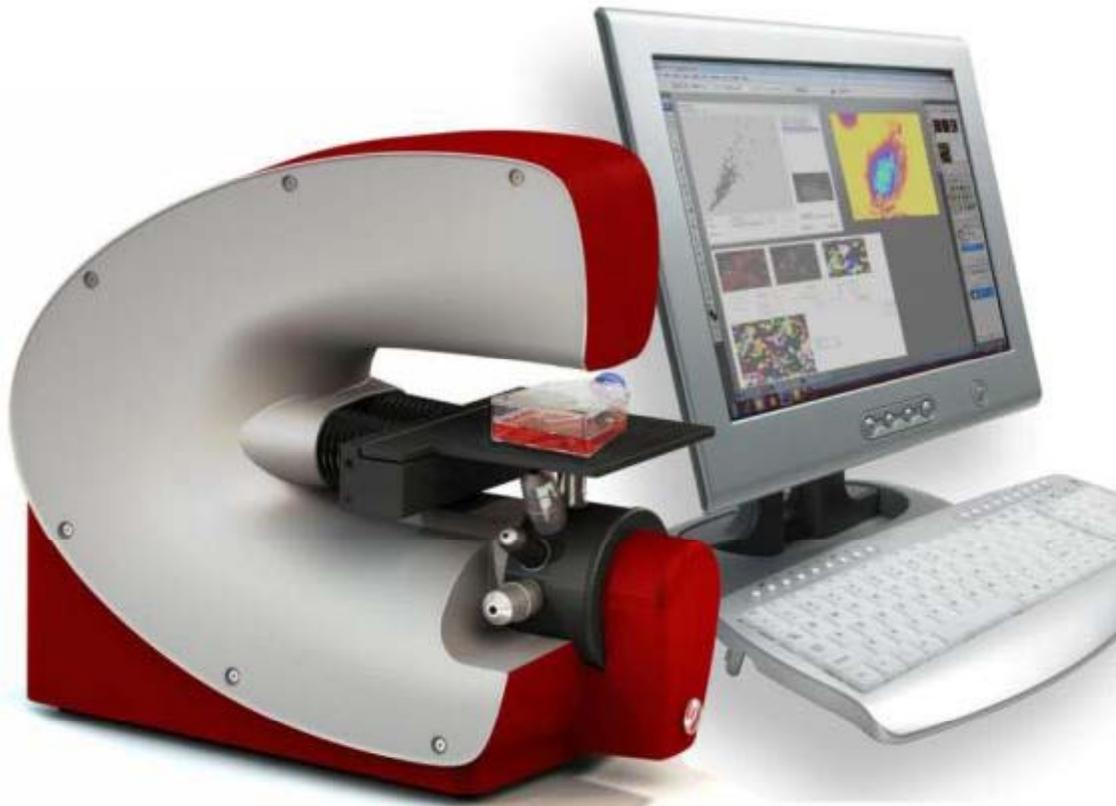
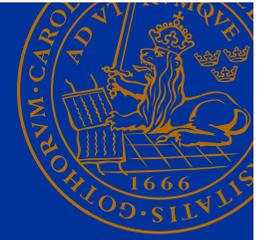
Measured input amplitude sweep



- 1.2 / 1.8V supply
- 90 nm RF-CMOS
- I & Q $\Delta\Sigma$ Modulators
- 0.48 x 0.62 = 0.3 mm²

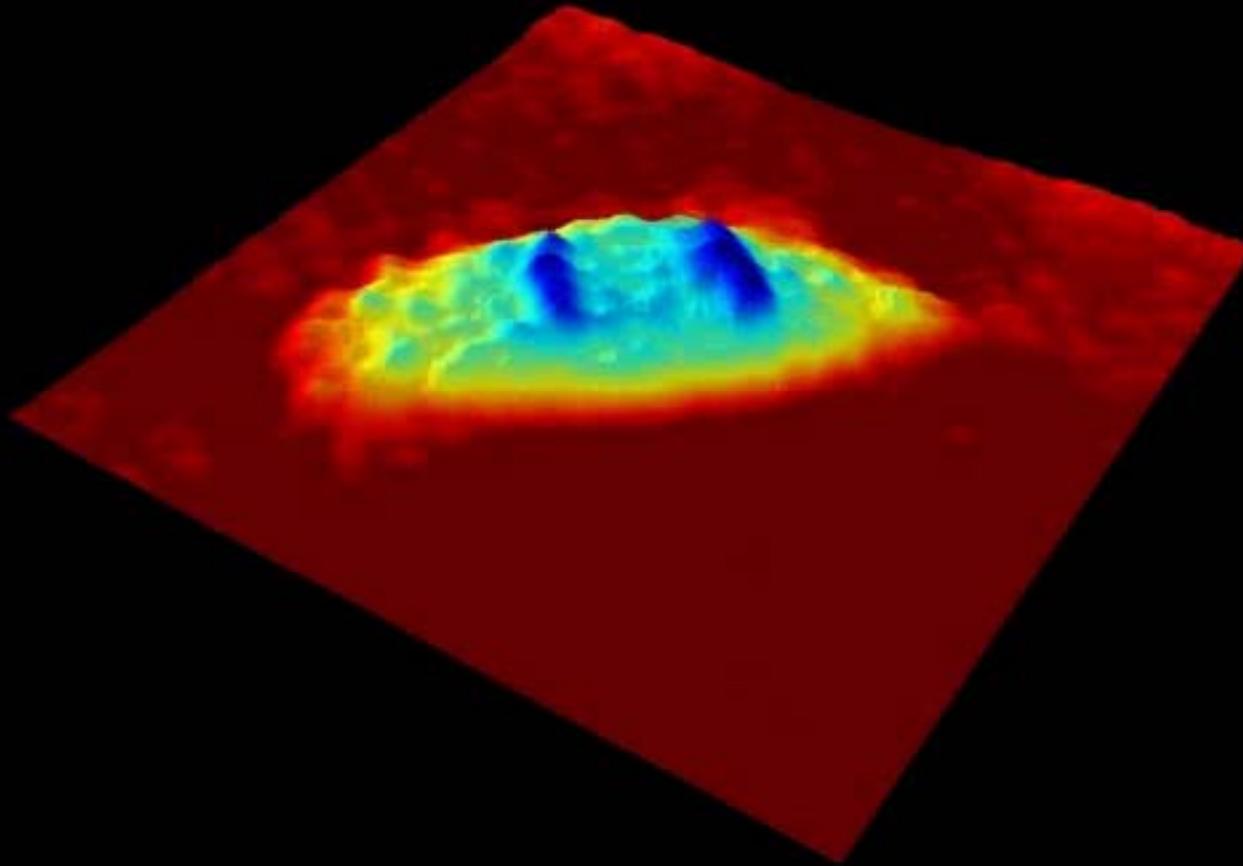
M. Anderson and L. Sundström, "CT $\Delta\Sigma$ Modulators With Reduced Sensitivity to Clock Jitter through SCSR Feedback", IEEE Journal of Solid-State Circuits, Feb. 2009.

Now a product



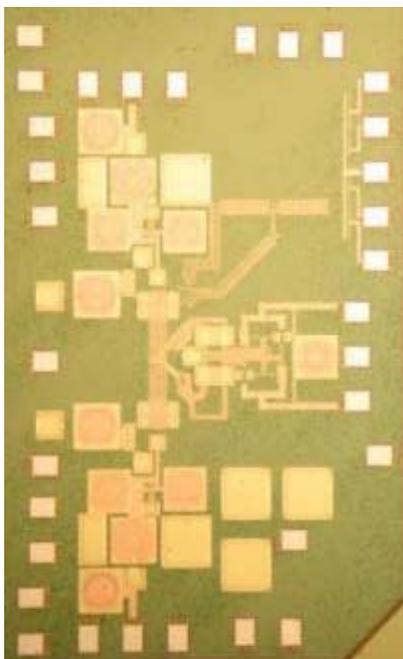
www.phiab.org

Phase image of a neuron

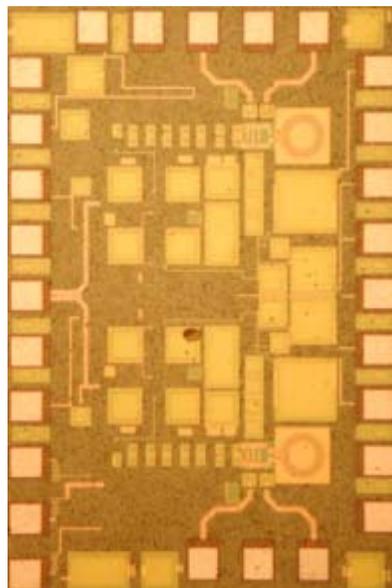


Created by Holomonitor M3: Cell division of Wilm's tumor, cell line WiT-49

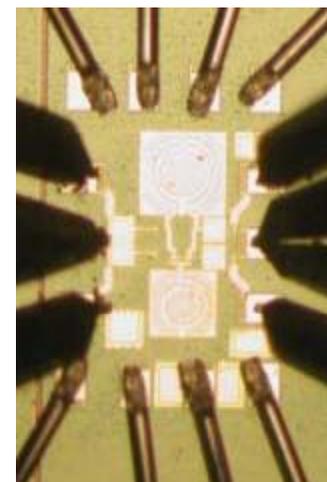
Beamforming: Receiver & Building Blocks



24 GHz receiver
2 channels
Analog baseband
phase rotation
ESSCIRC 2010



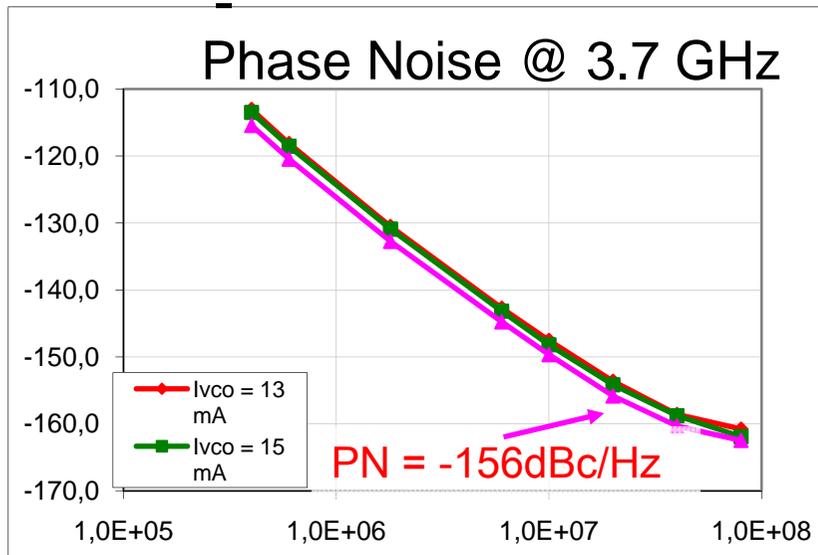
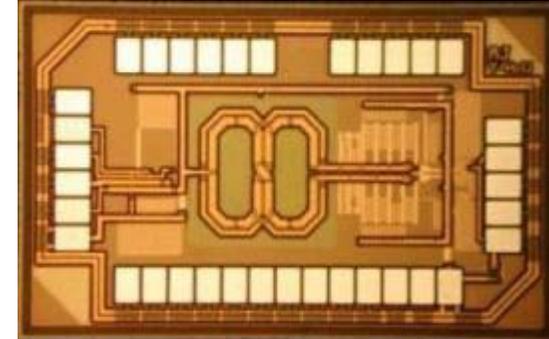
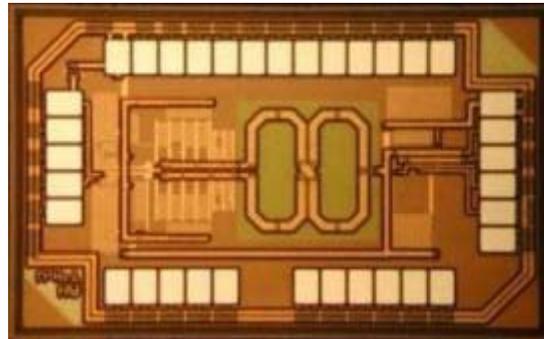
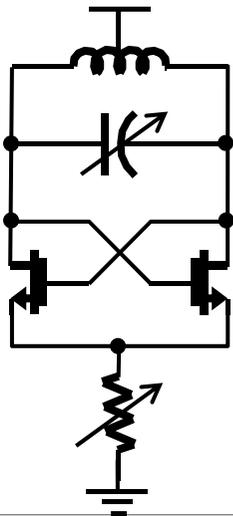
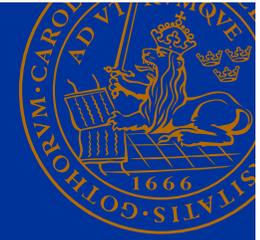
2 PLLs with
digital phase control
APMC Prize 2009



Injection locked
phase shifter
IMS 2010



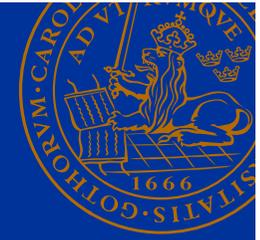
A Tx CMOS VCO for WCDMA/EDGE



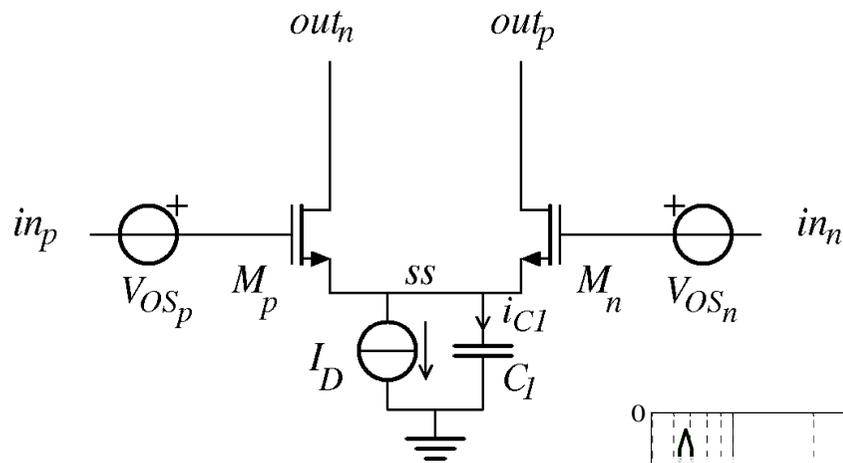
- 2.55GHz < TR < 4.08GHz
- Complies with GSM specs as well as SAW-less WCDMA TX specs

P. Andreani et al "A transmitter CMOS VCO for WCDMA/EDGE", ESSCIRC 2010

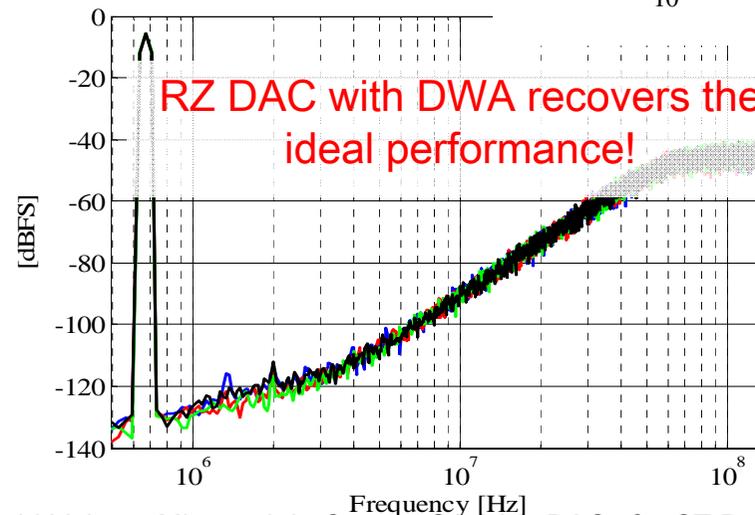
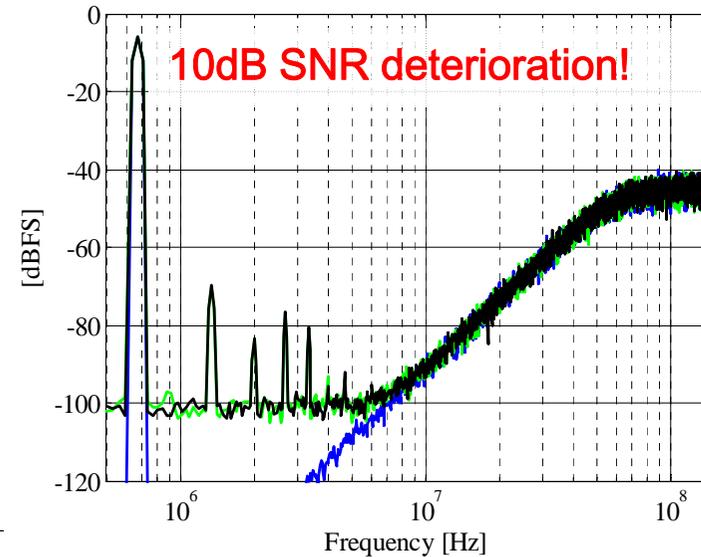
$\Delta\Sigma$ ADC with current-steering DAC



Mismatch between transistors causes nonlinearity!

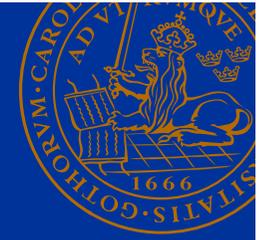


DAC unit-current cell

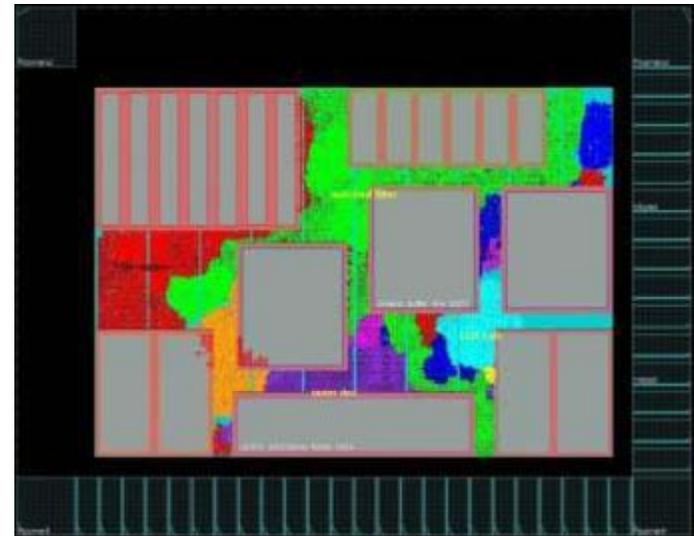
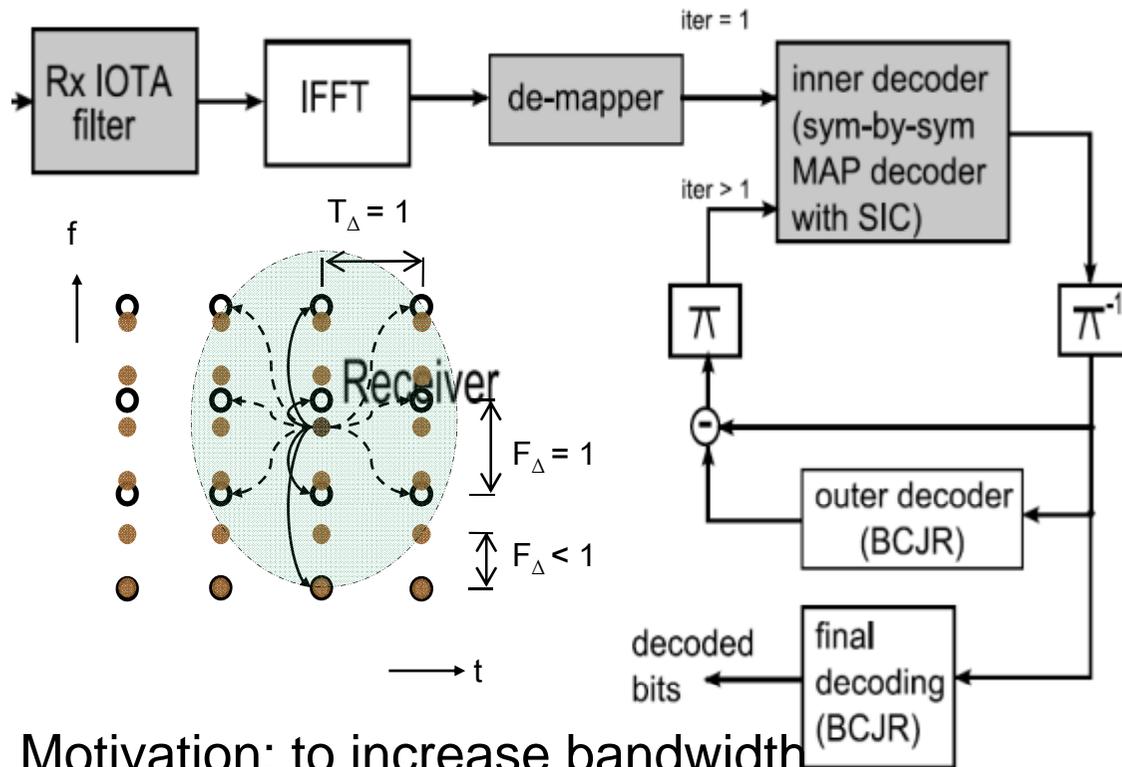


M. Andersson et al "Impact of MOS Threshold-Voltage Mismatch in Current-Steering DACs for CT Delta-Sigma Modulators", ISCAS 2010

Faster-than-Nyquist (FTN) receiver



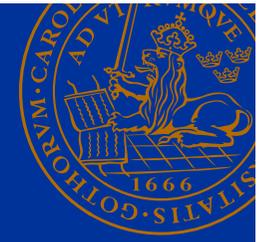
FTN iterative receiver



Designed for ST 65nm CMOS
Tape-out in November



Motivation: to increase bandwidth efficiency by compressing in time and/or frequency



**Thank You
and
Enjoy!**