Novel Architectures for Baseband Processing

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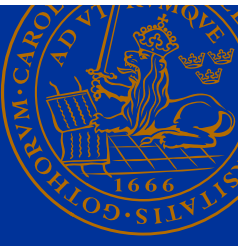
Outline



- Multibase project and DFE Rx
- Reconfigurable computations
- Sign bit synchronization
- Analog decoding
- SVD-based channel estimation

FP7 STREP Multi-Base

Multibase: January 2008 – April 2011

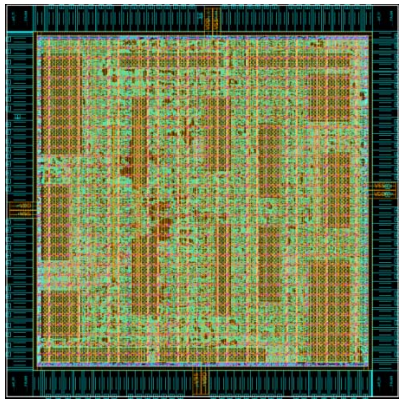
Scalable Multi-tasking Baseband for Mobile Communications

1. Multi-streaming radio (concurrent execution of multiple standards)
2. Scalable programmable/reconfigurable multi-processor technology
3. Algorithm/architecture co-design for maximum energy efficiency

LU Focus: Synch and Channel Estimation, algorithms and architectures.

FP7 STREP Multi-Base

Lund focus in circuits: DFE Rx



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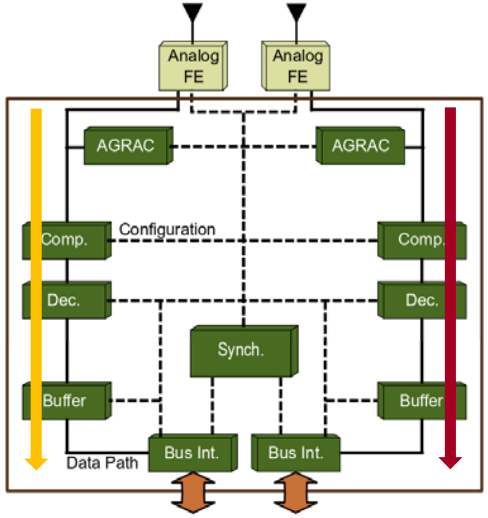
Motivation

- Design a multi-standard digital front-end receiver including:
  - Automatic Gain and Resource Activity Controller
  - Compensation
  - Filtering and resampling
  - Synchronization

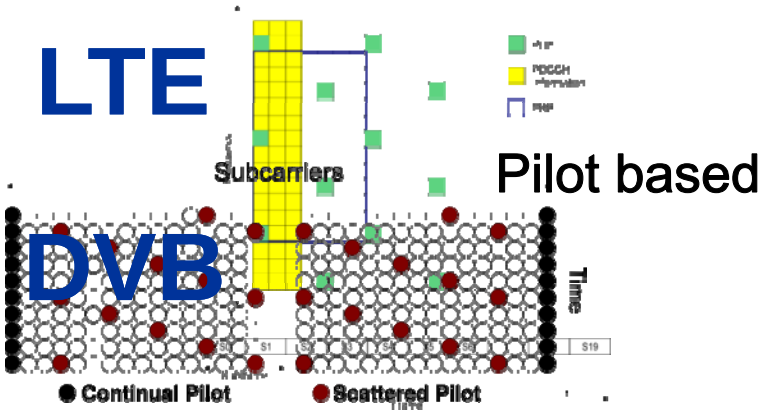


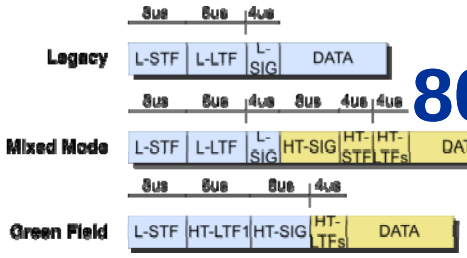
- Support for concurrent data streams
- Supported standards: LTE, DVB-H and IEEE 802.11n

The standards

- All three standards are OFDM based, however with different FFT-size:
  - LTE: 128-2048
  - DVB-H: 2048, 4092 (and 8192)
  - IEEE 802.11n: 64-128

- …and different sample rates:
  - LTE: 30.72 Msps
  - DVB-H: 9.143 Msps
  - IEEE 802.11n: 20 or 40 Msps





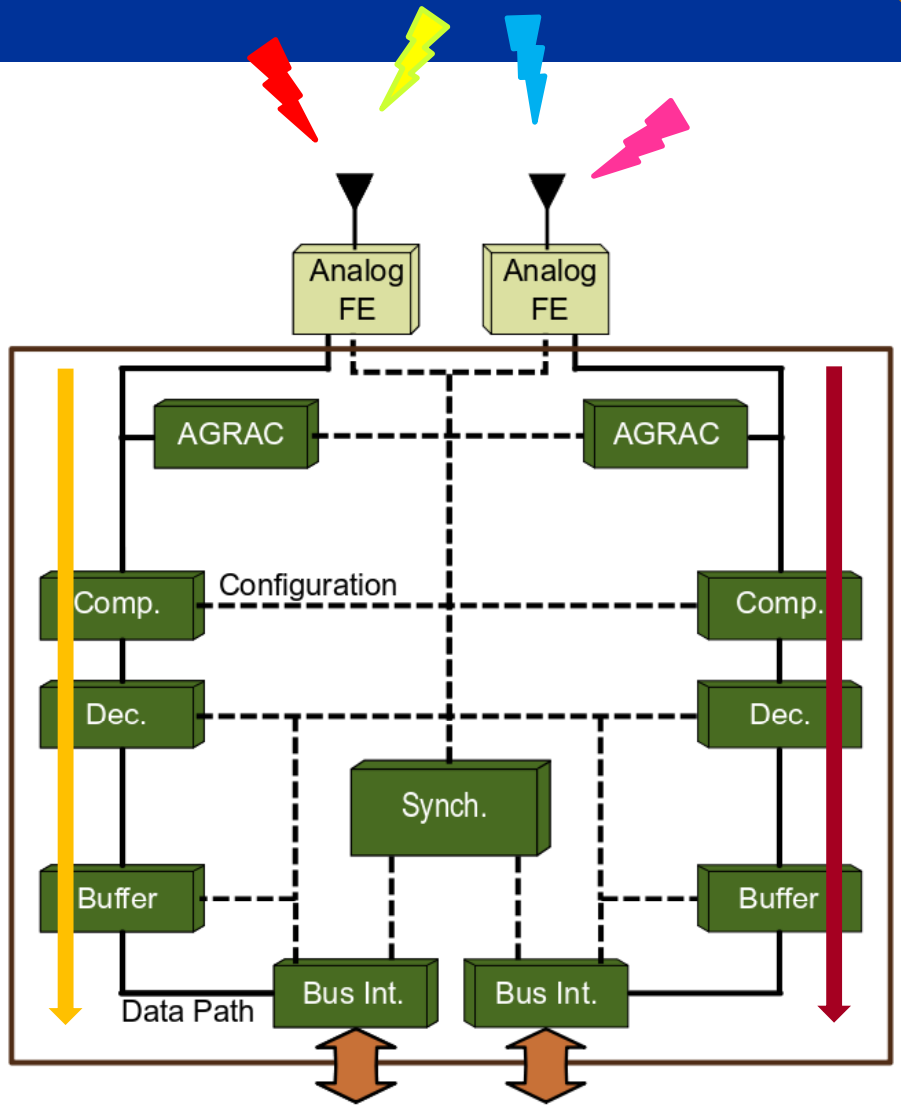
802.11n

Preamble based

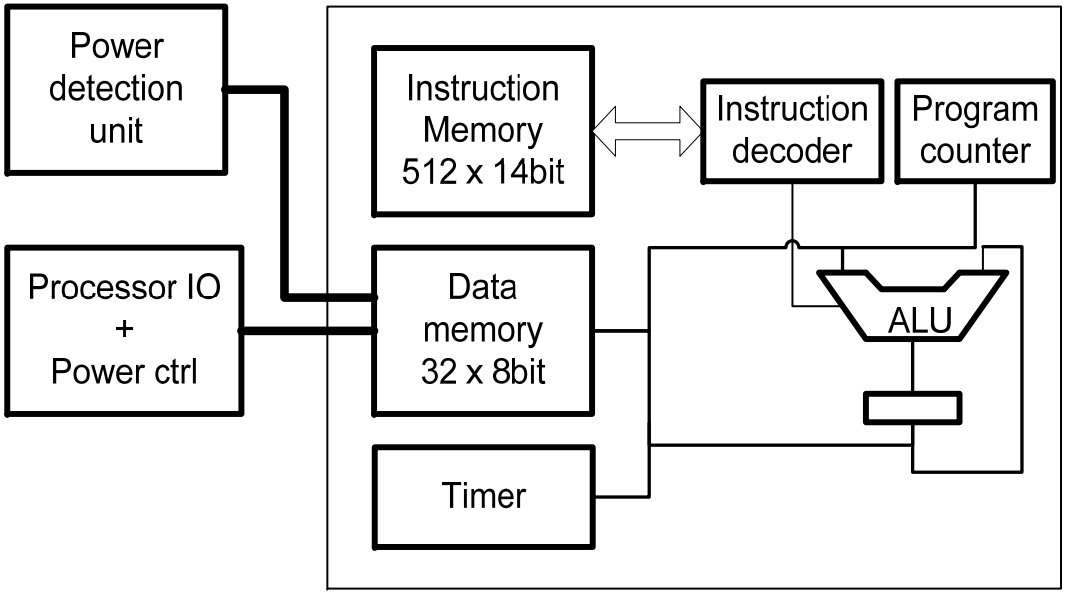
The multi stream DFE-Rx

Two concurrent data streams in hardware.

More data streams possible since they do not transmit all the time.



AGRAC - Automatic Gain and Resource Activity Controller

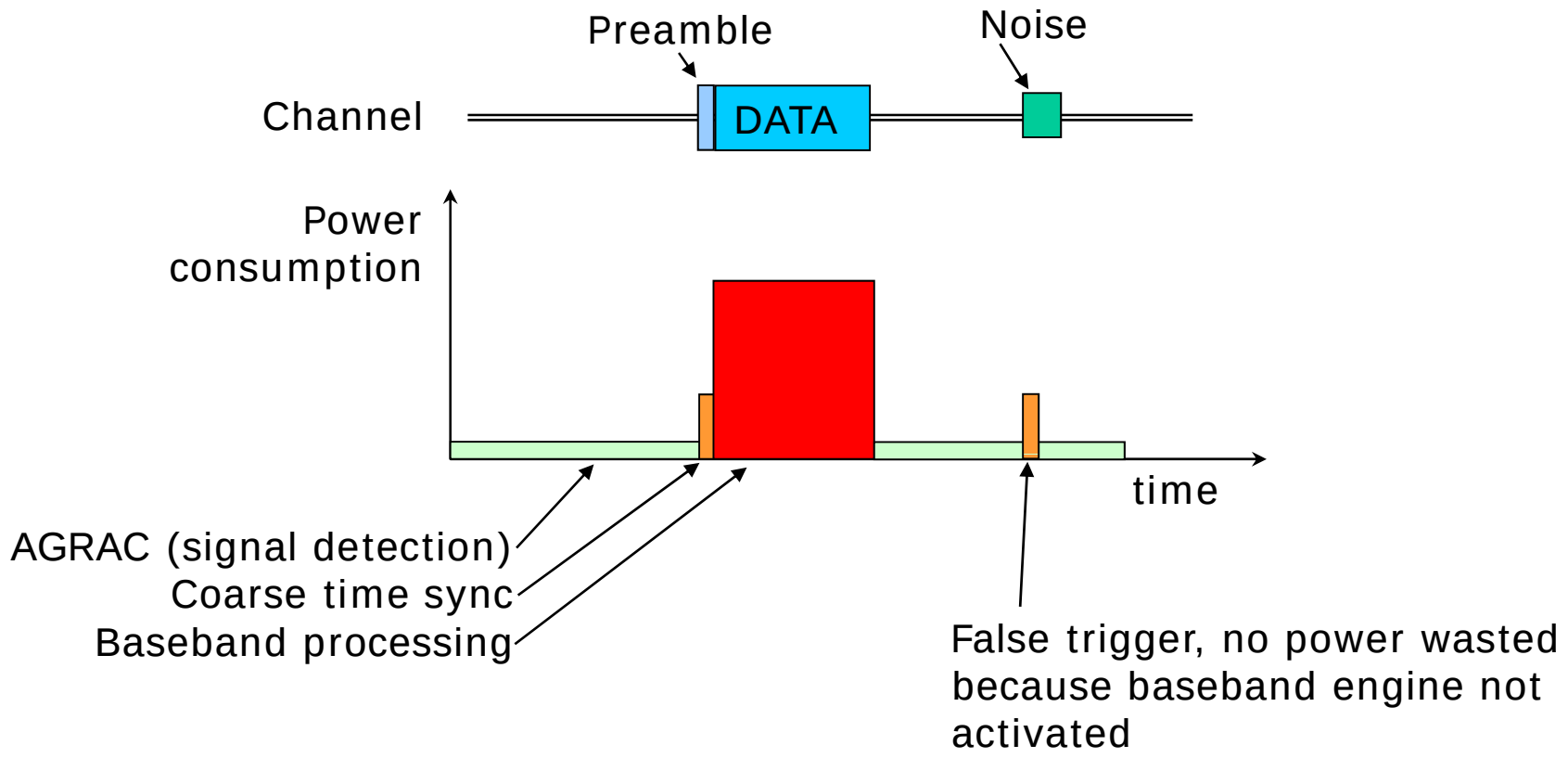


- Performs AGC of the analog frontend
- Enables/disables other subblocks of the DFE Rx and baseband processing as required.
- Hierarchical wakeup to conserve power.

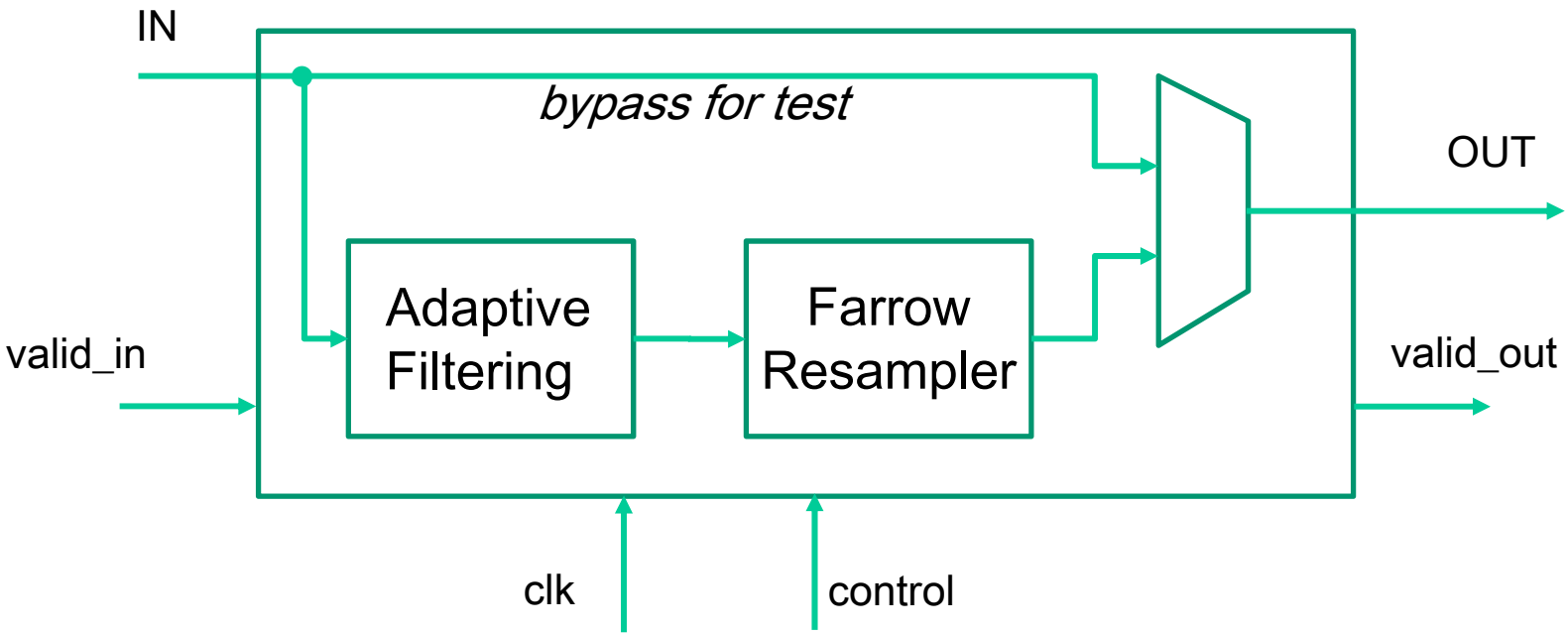
Hierarchical wakeup: principle

Component	Activation probability	Power consumption
Baseband	Low	High
Sync		
AGRAC	High	Low

Example: reception of WLAN

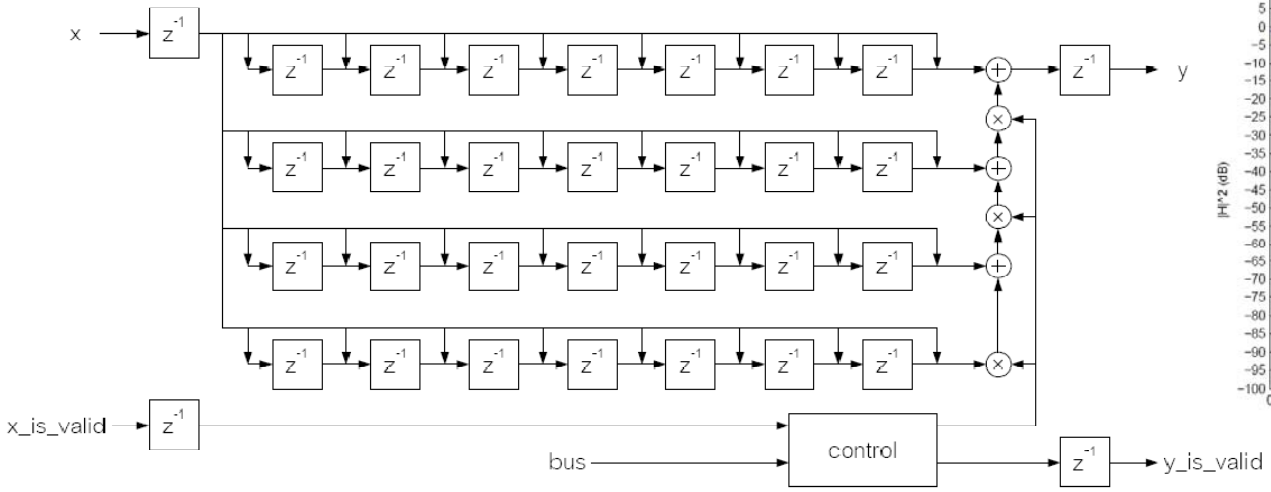


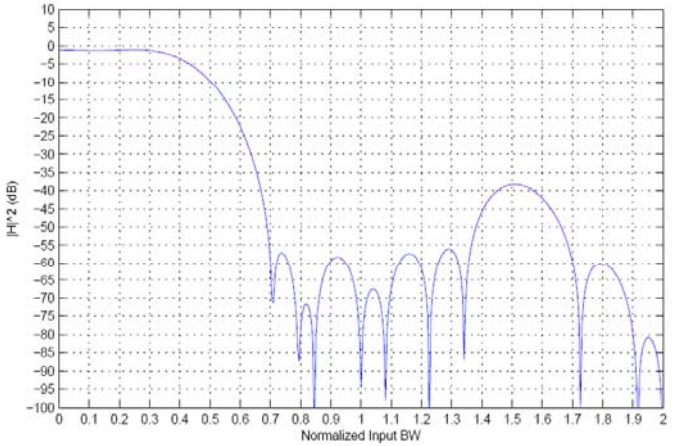
DFE Decimation Chain



- Reconfigurable for LTE, 802.11n, and DVB-H
- One decimation chain for each DFE stream

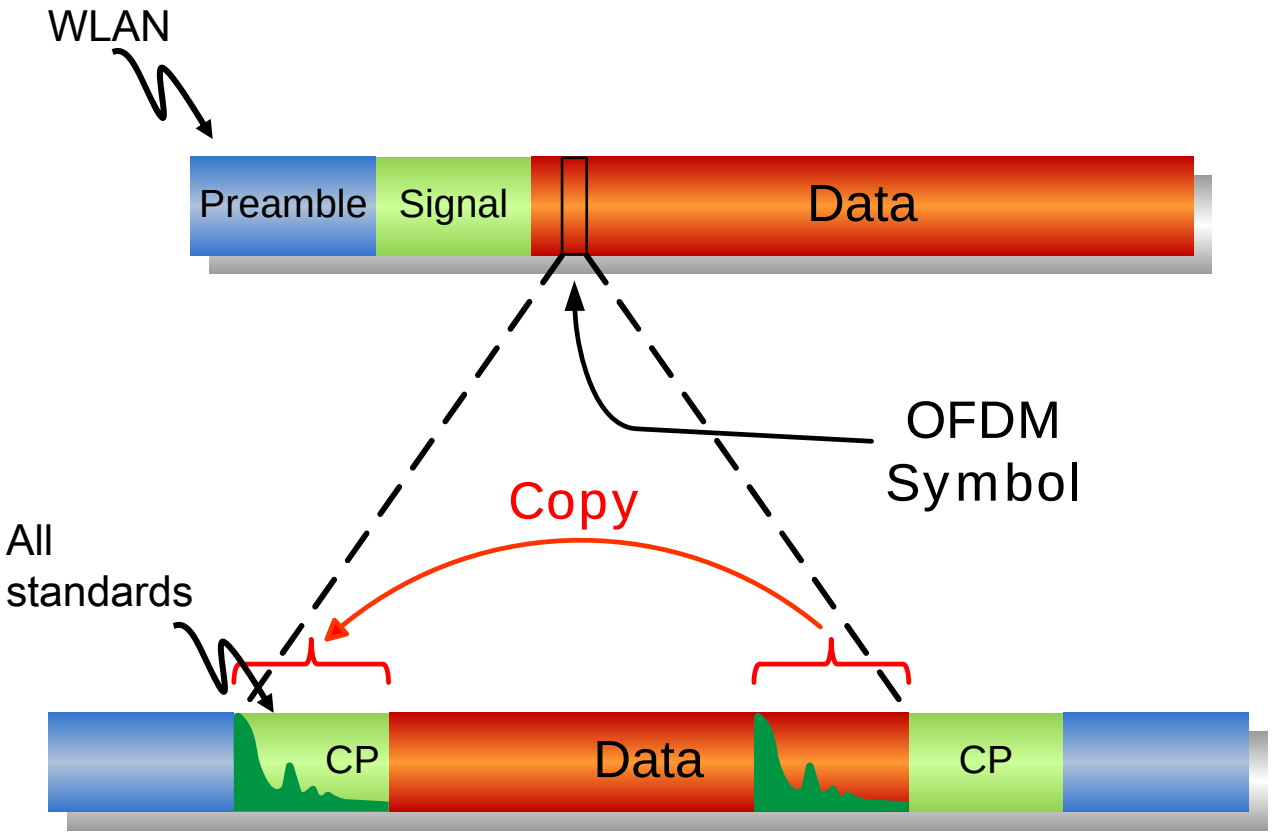
Farrow Resampler



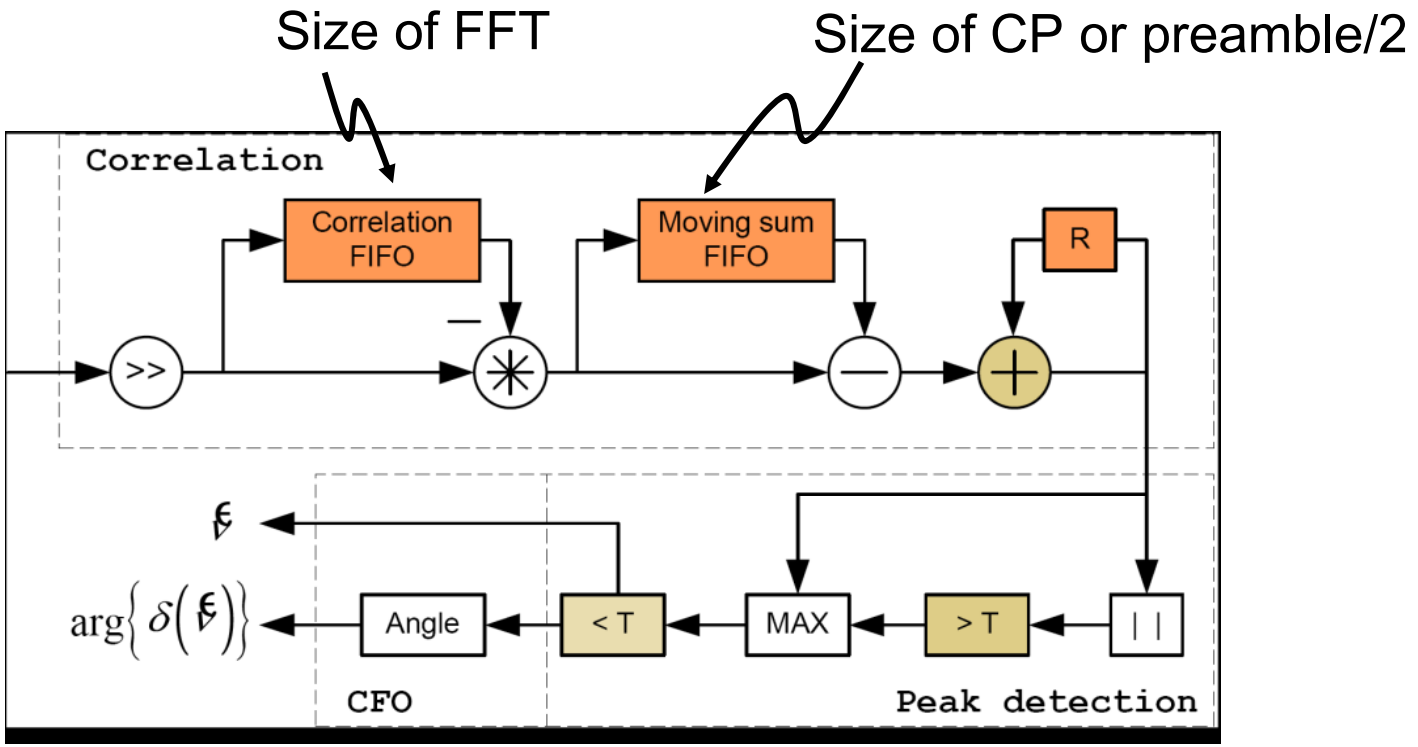


- Polynomial order = 3, Length = 8
- Transposed FIRs for reduced delay
- Optimized fixed point coefficients and maximal coefficient sharing
  - Realized through integer linear programming

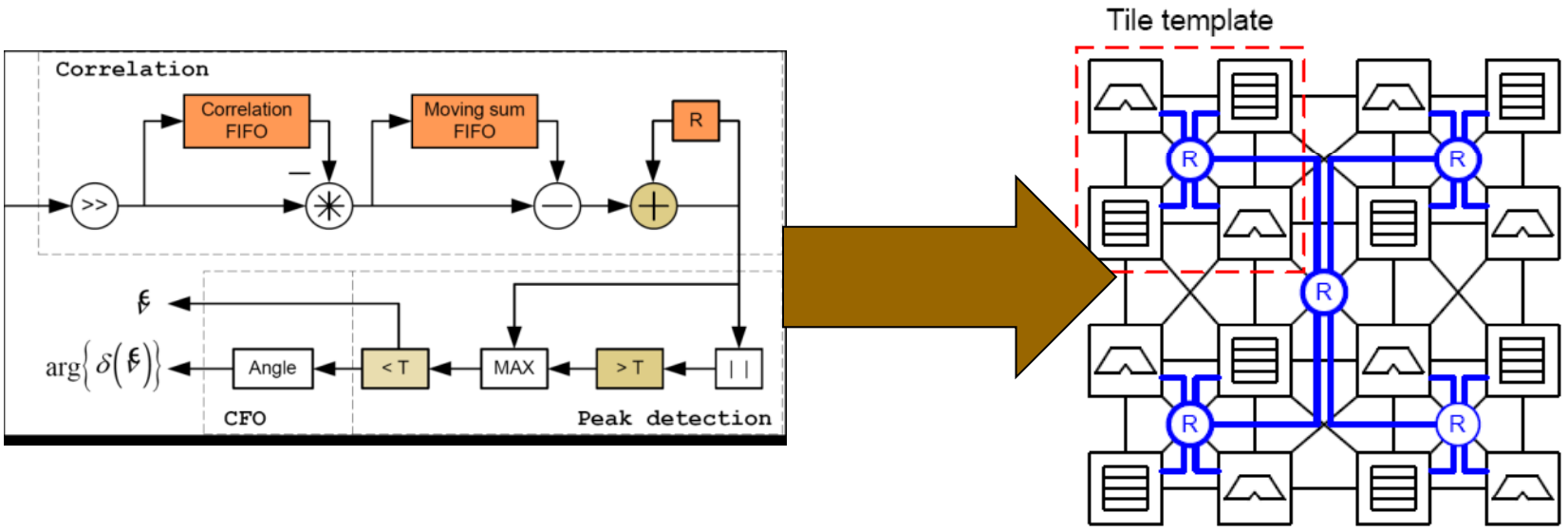
Synchronization



Synchronization Architecture



Synchronization Hardware

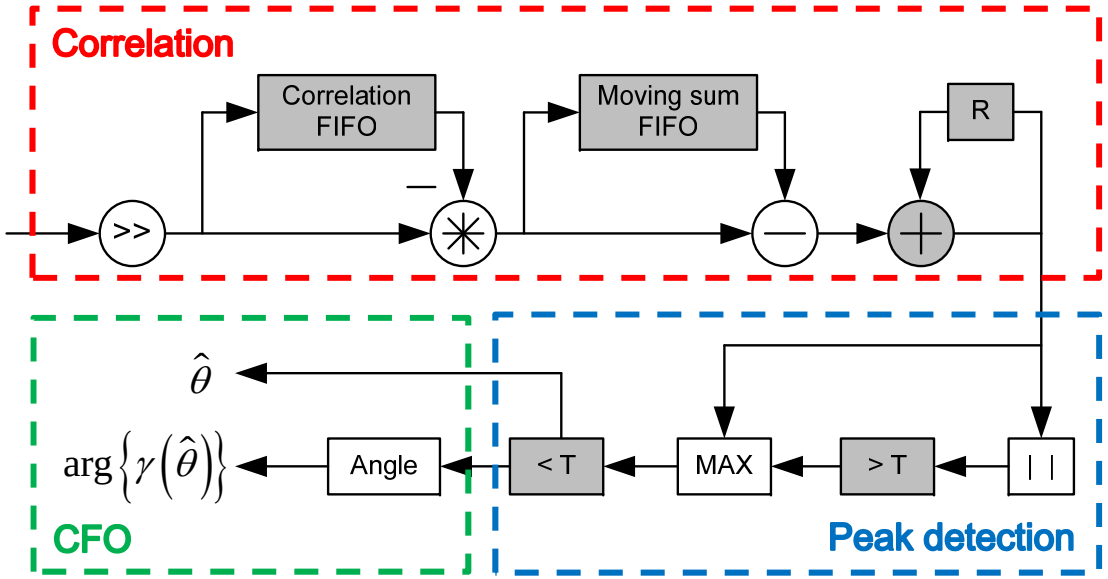


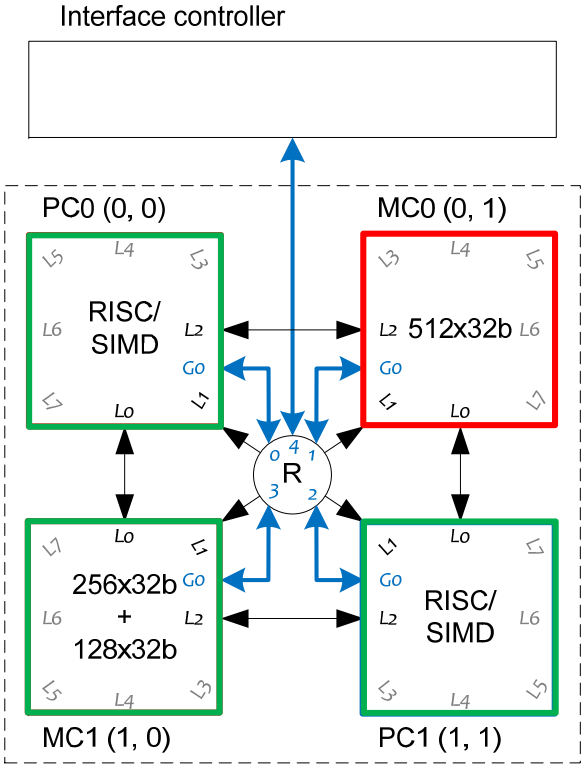
Mapped onto a reconfiguarble processing array:

- flexibility since multi-standard
- hardware reuse since sync only part of the time

Multi-standard OFDM time synchronization

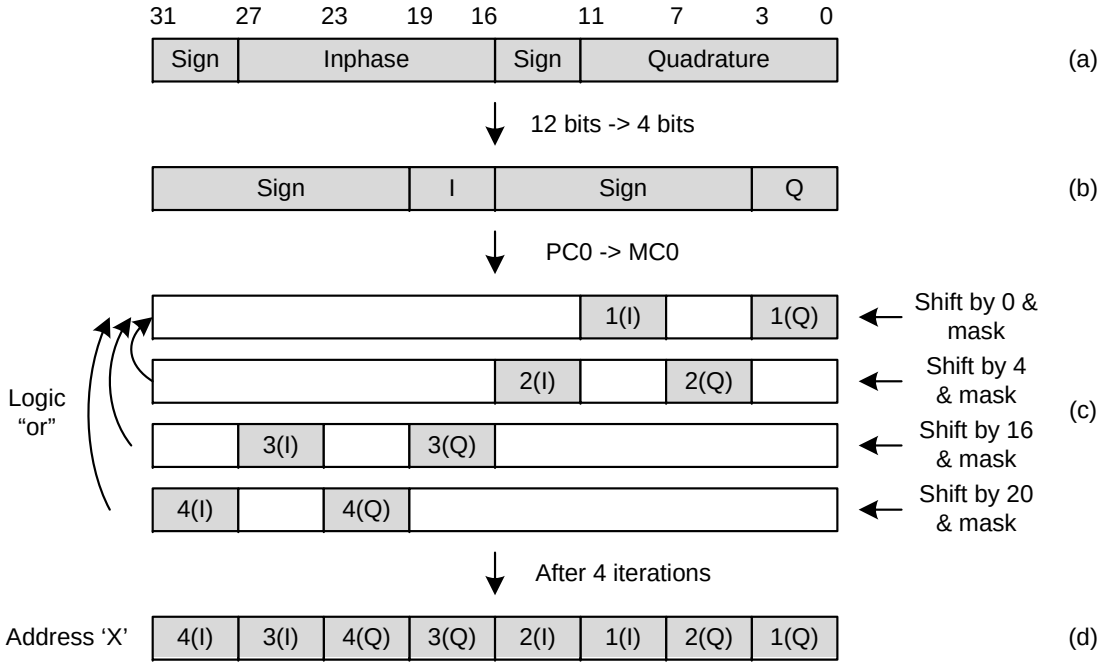
- Multiple radio standard support
- Dual-standard concurrent support
- Scenario-aware adaptive resource allocation
- Expandable to more streams





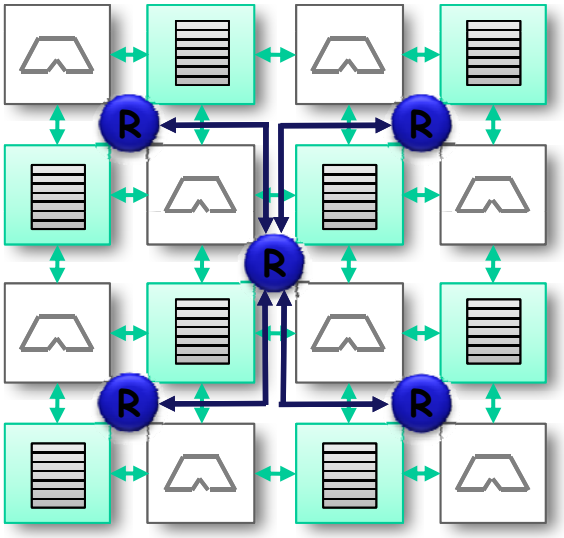
Interleaved data storage

- Micro-block function in MC eliminates data alignment operations in PC.



Coarse-grained reconfigurable architecture

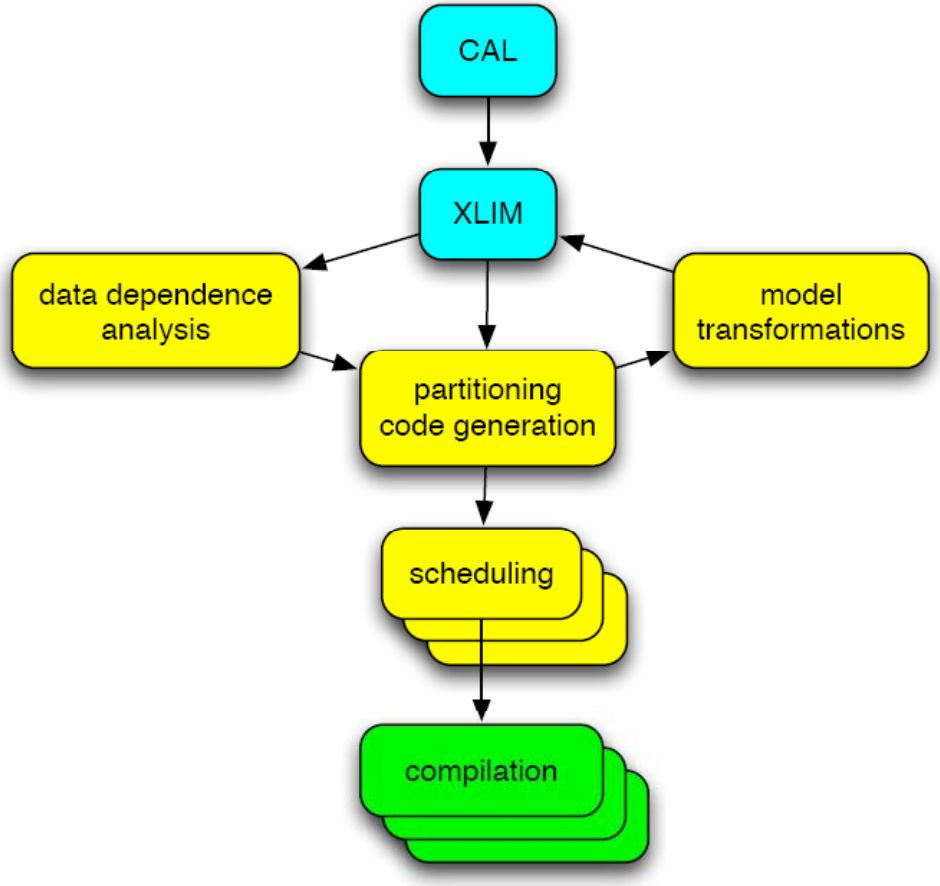
- Heterogeneous cell array.
- Decoupled processing and memory cells.
- Dedicated local connections for high data throughput.
- Hierarchical global routing network for communication flexibility.
- Single-Cycle-Per-Hop communication latency.
- Centralized & Distributed cell configuration management.



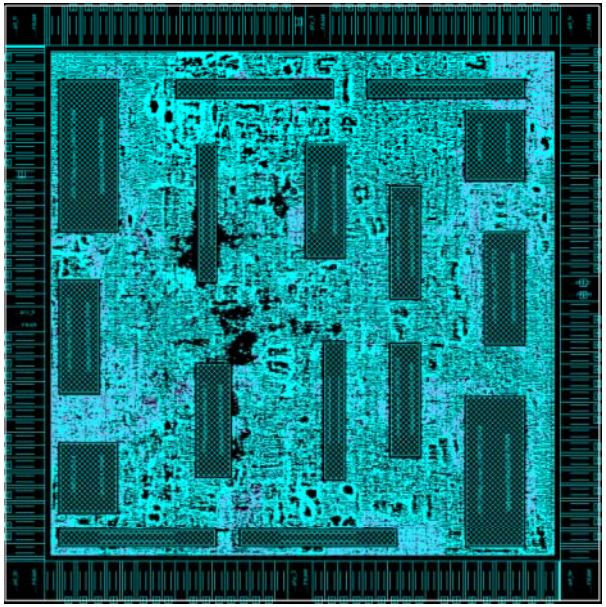
Application mapping with CAL

Mapping of applications and algorithms is a crucial task in order to make them useful.

- In cooperation with the computer science department at LTH.
- CAL, data flow language to specify parallelism for parallel hardware.
- Data centric application mapping.

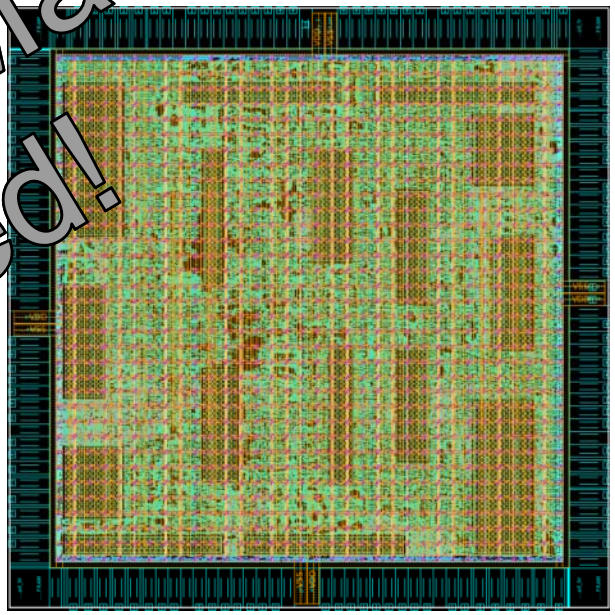


The Chip



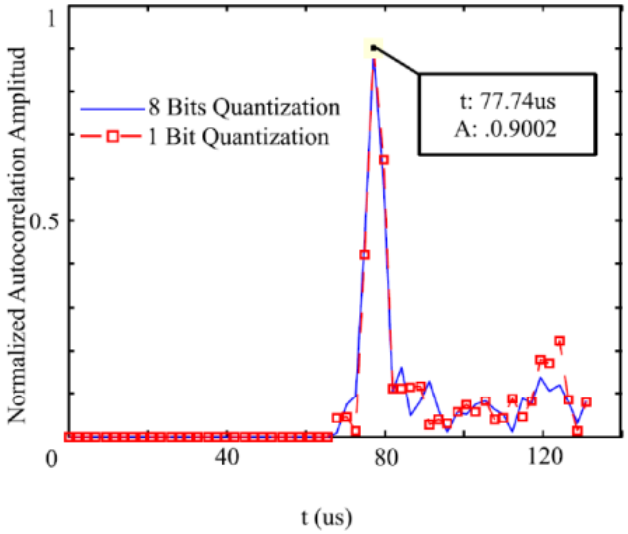
- Infineon 65nm CMOS process
- Total area *5mm²*
- 144 Pads
- Clock frequencies:
  - Main part 80MHz
  - Synchronization engine 320MHz through on-chip clock multiplier

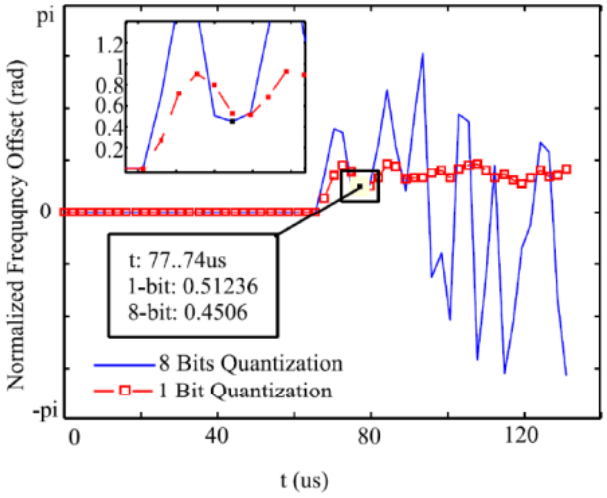
The Chip



Alternative: Sign-Bit Synch.

What can we do with only the sign of the IQ components?





Presented at ISCAS´10 and VTC´10.

Alternative: Sign-Bit Synch.

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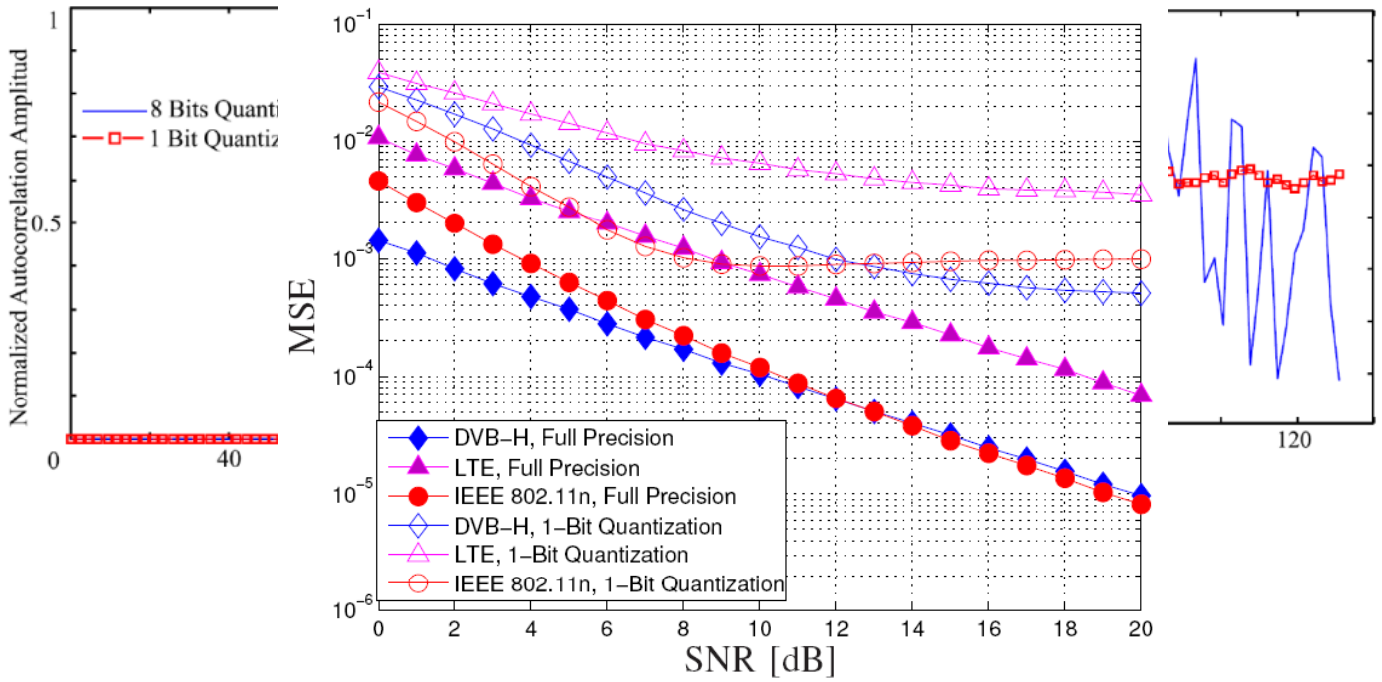
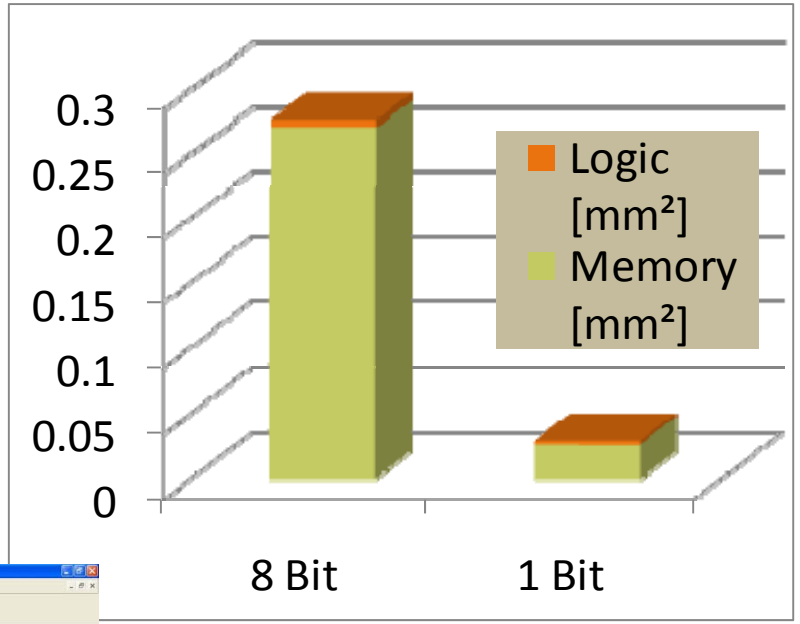


To be further evaluated, OK for coarse synch?

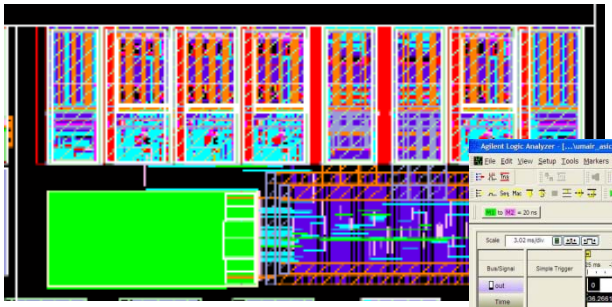
Sign-Bit Synchronization: implementation results

97% area reduction

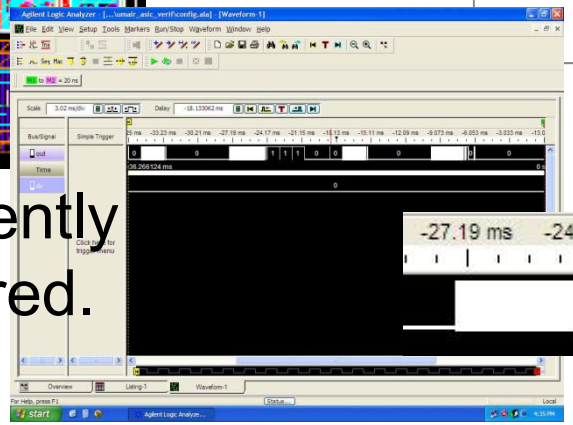


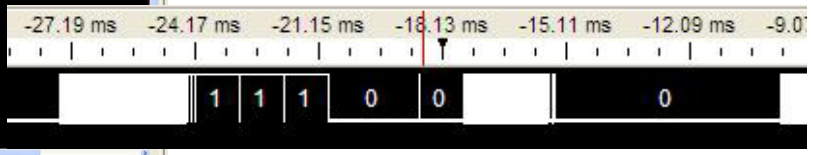
Process: ST65nm CMOS

	Memory in correlation	Memory in moving sum	Comb Logic	Total
Sign	*0.033*	*0.012*	*0.0018*	*0.047*
8 Bits	*0.25*	*0.4*	*0.006*	*0.668*



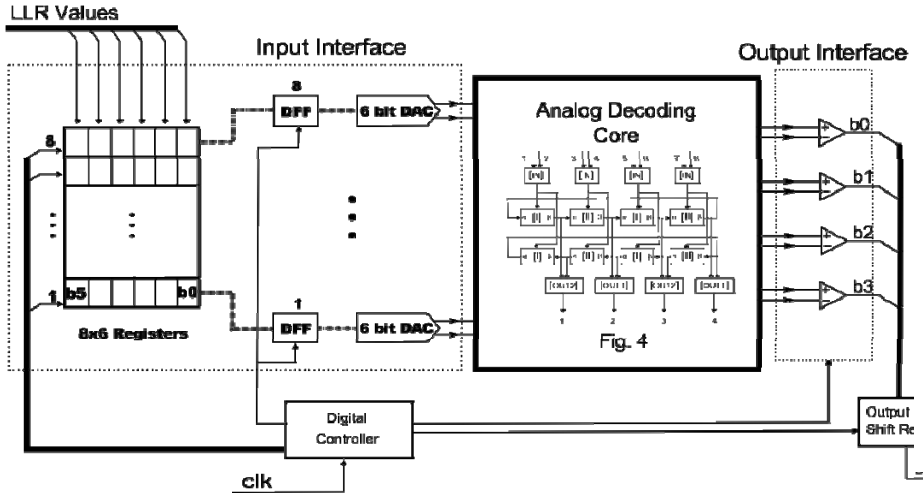
The chip is currently being measured.

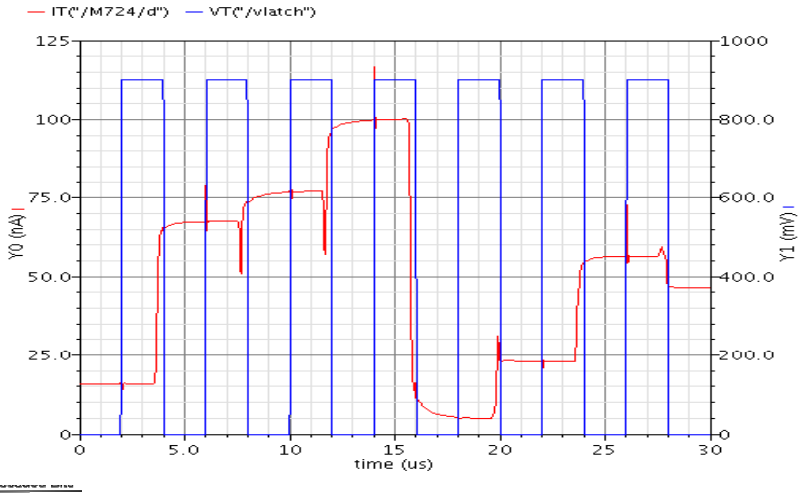


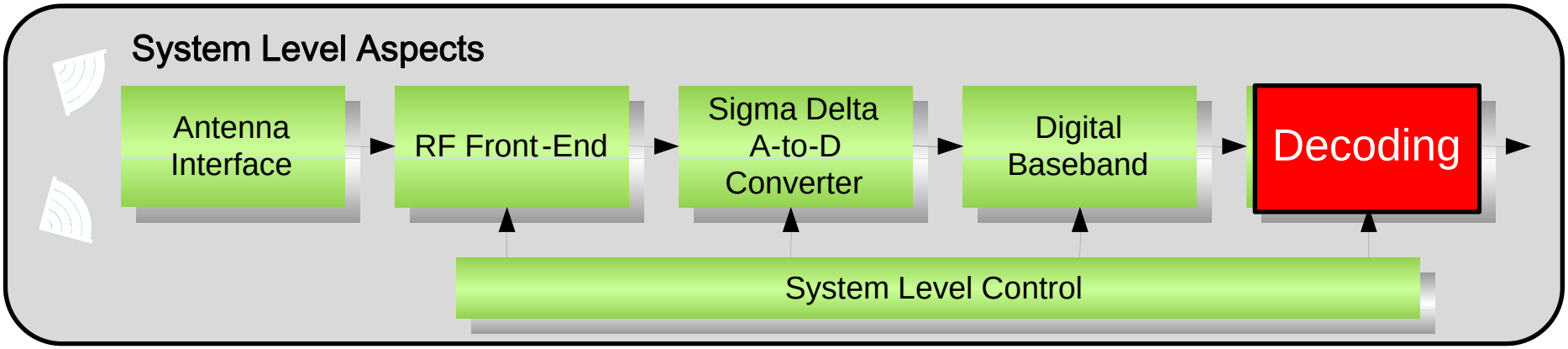


UPD: analog decoding

Analog decoder in a digital environment.



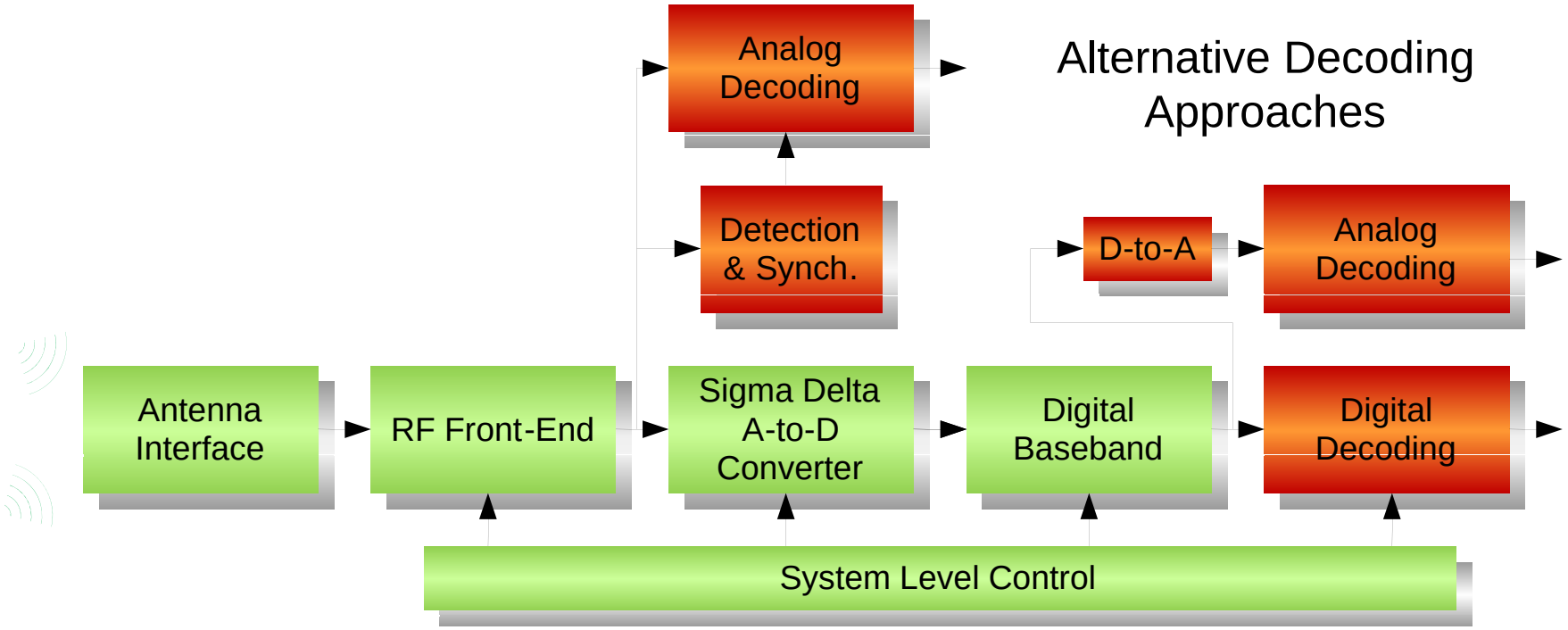




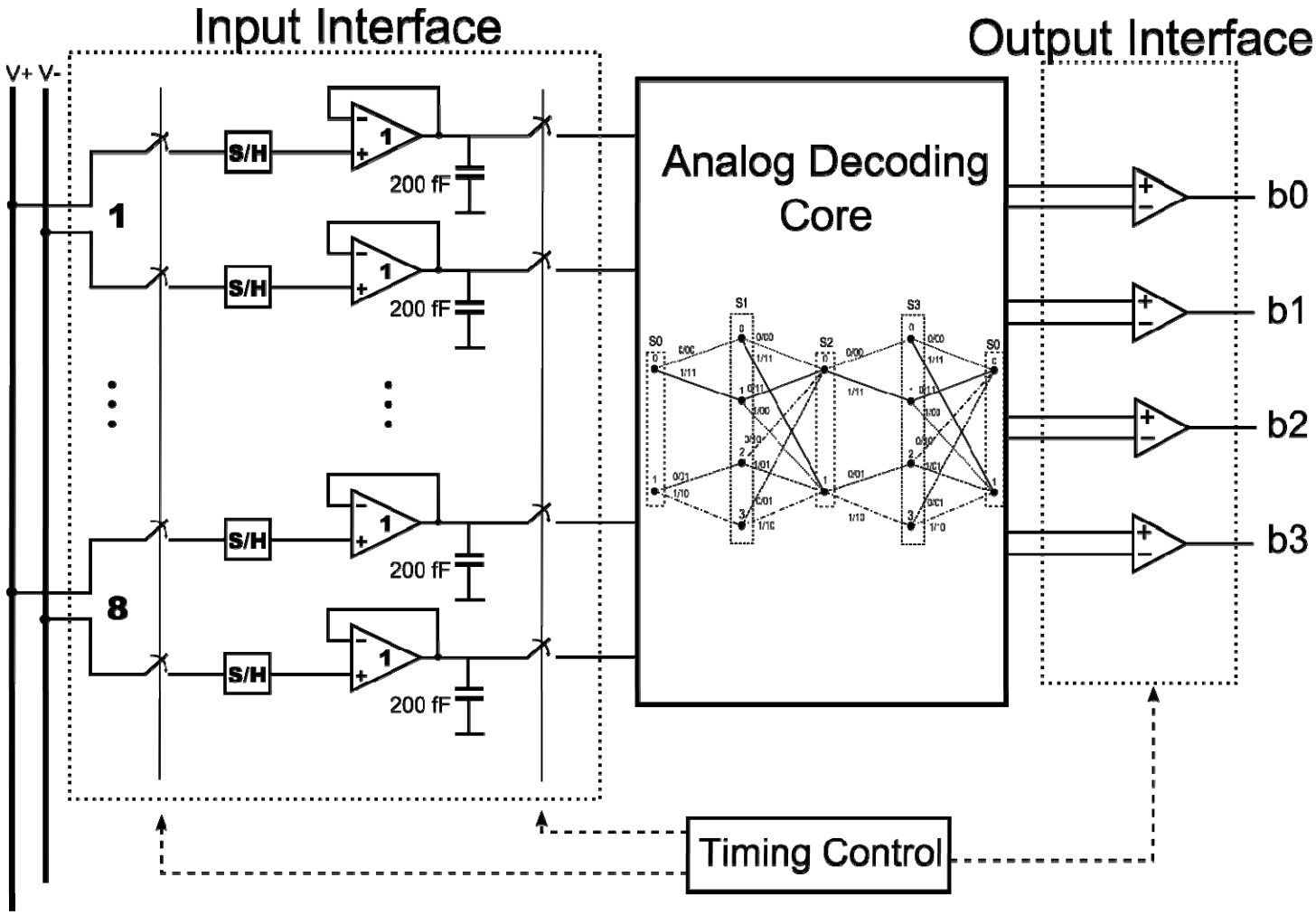
UPD: analog decoding

Why analog decoders:

- very low power consumption
- less area on silicon
- high throughput due to parallel computations



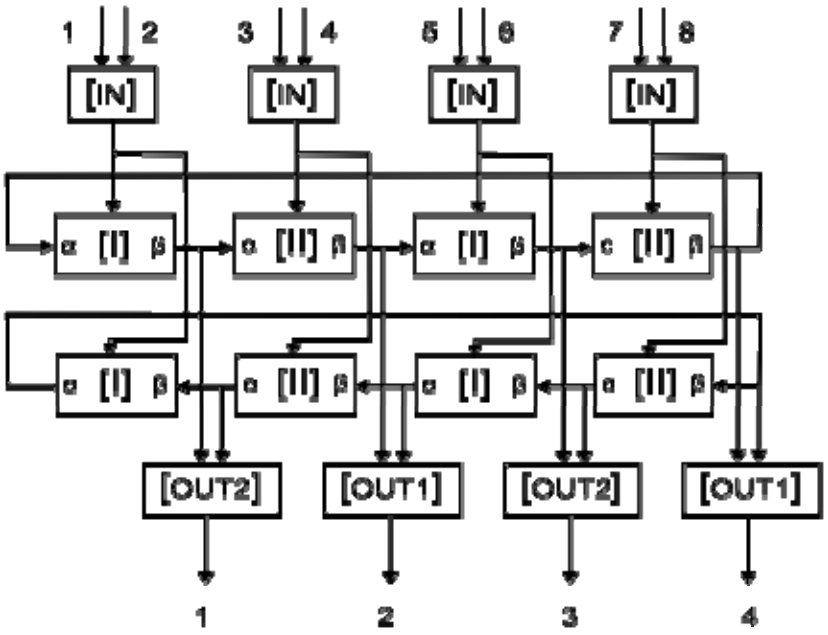
Analog decoder: analog in/digital out

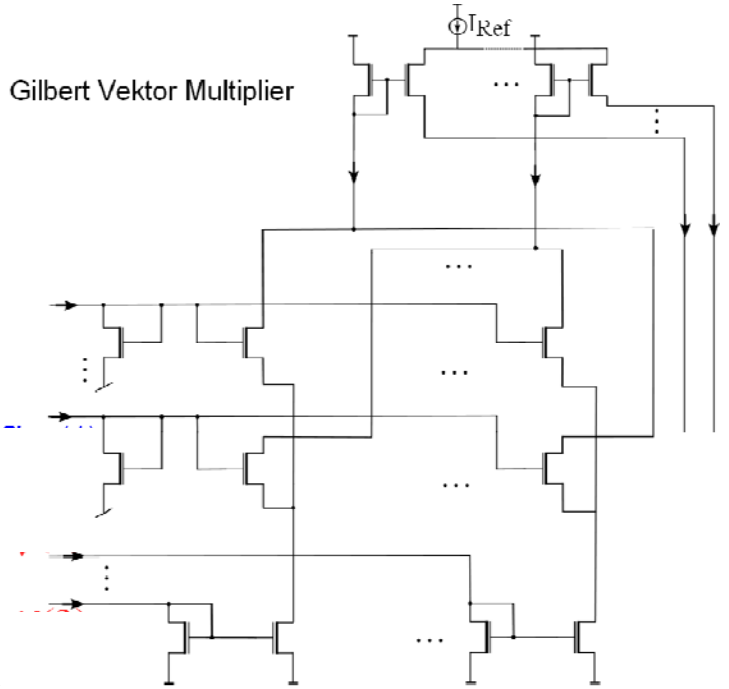


Analog Core Module for BCJR

Analog Core

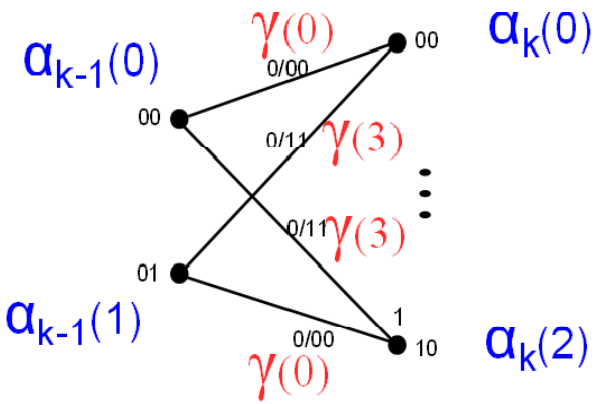
The structure of the core will decide the code, e.g. Hamming or tailbitingconvolutional (7,5)





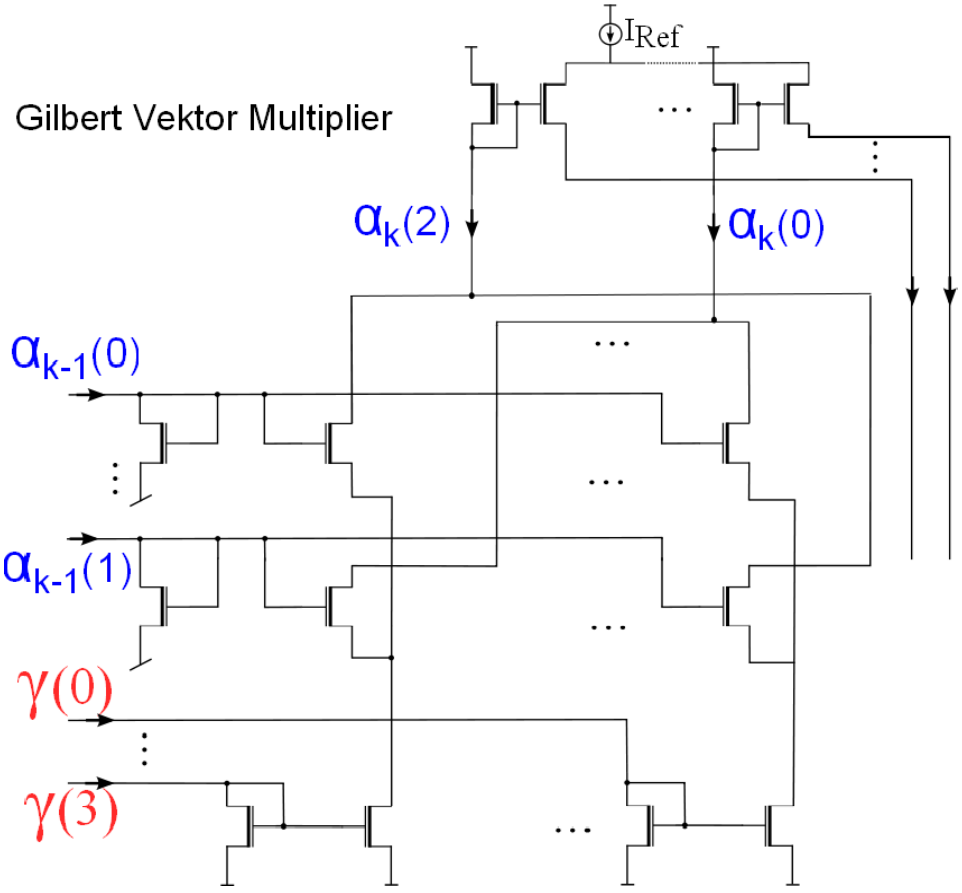
Analog Core Module used for BCJR calculations.

Analog Core Module for BCJR



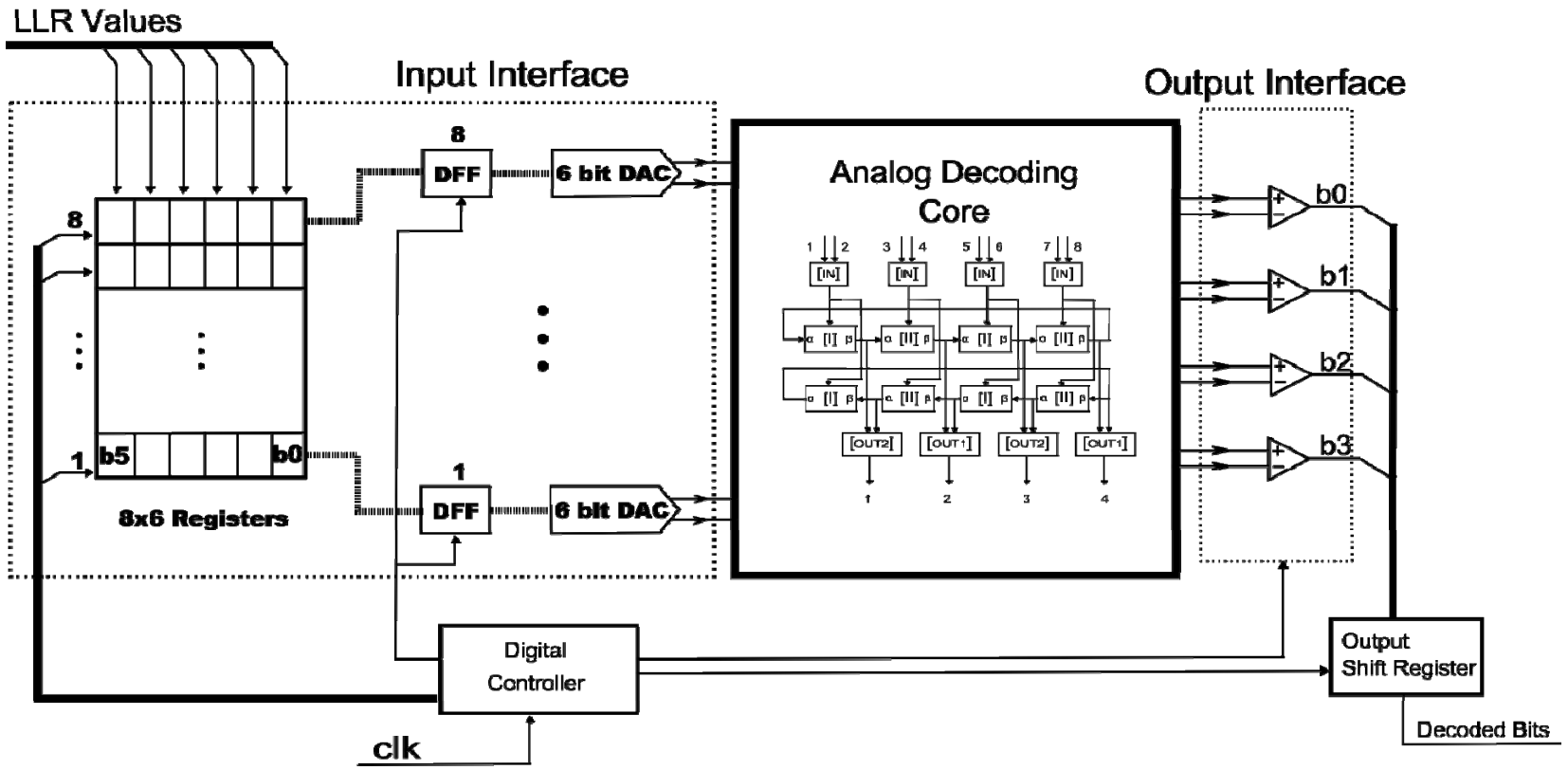
$$\begin{cases} \alpha_k(0) = \alpha_{k-1}(0)\,\gamma(0) + \alpha_{k-1}(1)\,\gamma(3) \\ \alpha_k(2) = \alpha_{k-1}(1)\,\gamma(0) + \alpha_{k-1}(0)\,\gamma(3) \end{cases}$$

Forward metric calculations in BCJR algorithm.
Backward in the same way.

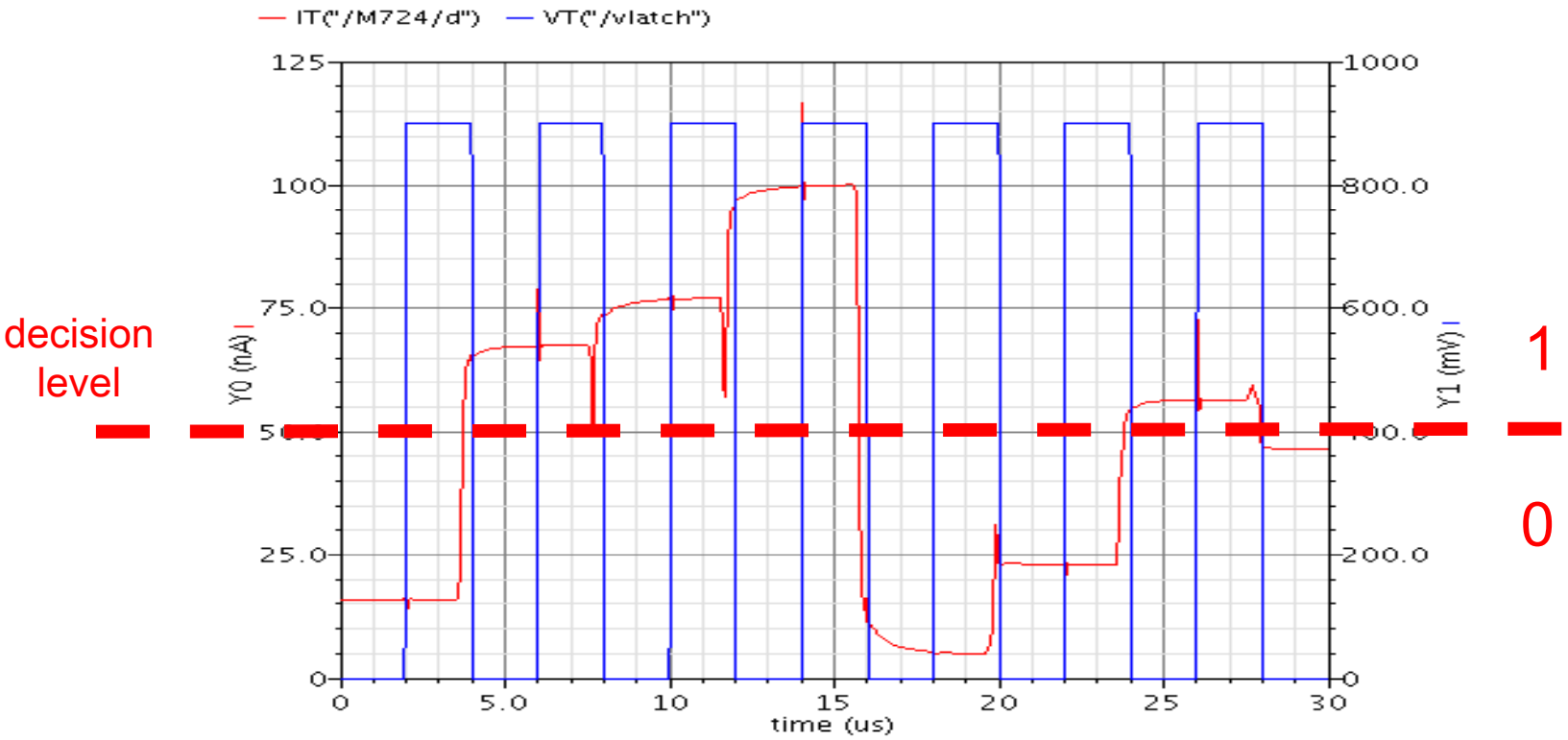


Equivalent analog circuit.

Alternative structure: digital in/digital out



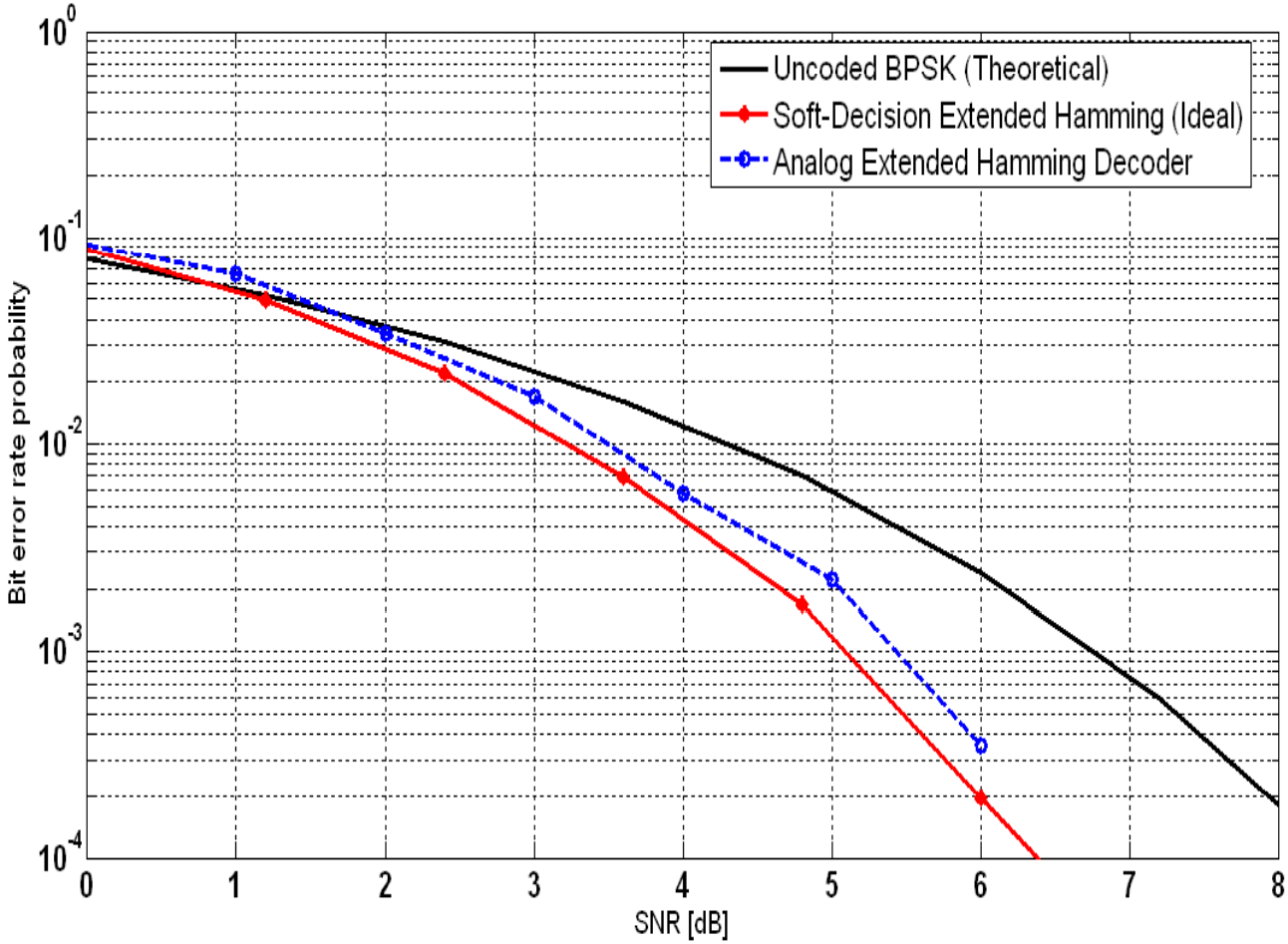
Decoder Output for a Single Bit



Cadence netlist simulations:

- Less than 4 µs is needed to decode the transmitted codeword
- Decision: when circuit converges to an steady state

BER performance

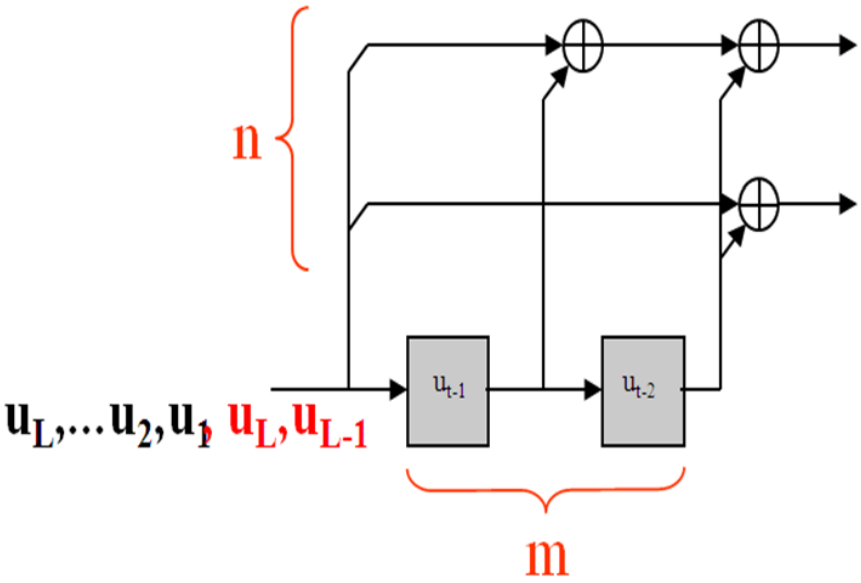


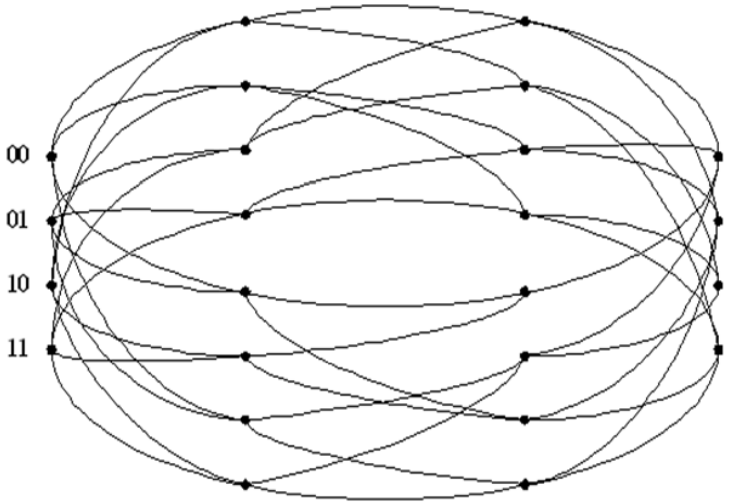
Results: Analog Hamming Decoder

Technology	TI's 65nm low power CMOS library
Supply Voltage	1.4 V
Input Voltage Range	400-800 mV
Clock Frequency	2 MHz
Decoder Throughput	1 Mb/s
Energy per decoded bit	22 pJ/b
Coding gain @ BER=10^{-3}	1.3 dB

	Power Consumption [μW]	Percentage [%]
Input interface	14	63.6
Decoder core	6	27.3
Output interface	2	9.1
Total	22	100

Future work: extend to Convolutional





Corresponding tail-biting trellis

Expectations: Better performance compared to Hamming decoder

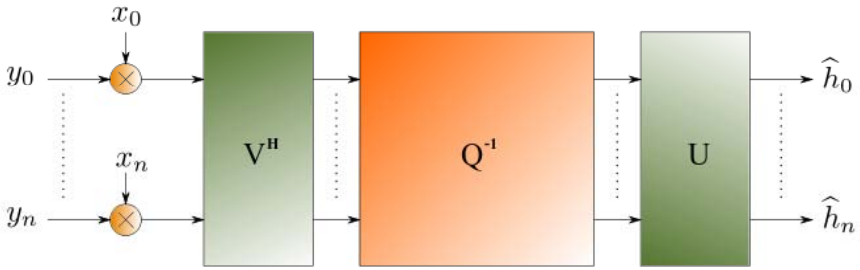
Cost: More complexity => More power consumption and area

How much? => Research is ongoing

SVD-based Channel Estimation

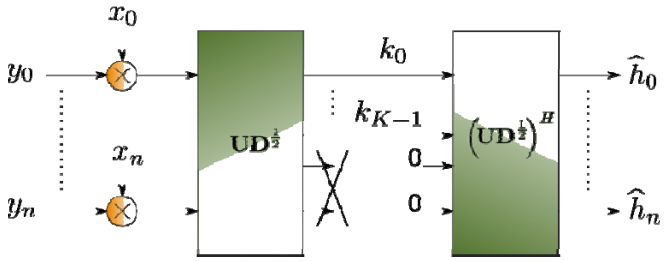
- SVD reduces the complexity of a linear MMSE estimator
  - A number of values are close to zero and can be ignored

$$W = UQ^{-1}V^{H}$$



SVD-based Architecture, where U and V are orthonormal matrices and Q−1 is a filtering matrix.

$$W = UDU^{H} = UD^{1/2}(UD^{1/2})^{H}$$



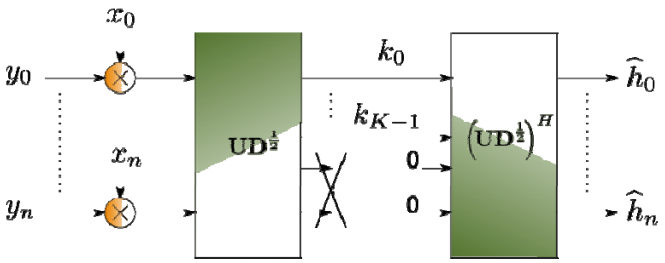
Conceptual Architecture showing a number of values ignored

Presented at NORCHIP 2009

SVD-based Channel Estimation

- SVD reduces the complexity of a linear MMSE estimator
  - A number of values are close to zero and can be ignored.
  - HOW MANY?

$$W = UDU^H = UD^{1/2}(UD^{1/2})^H$$



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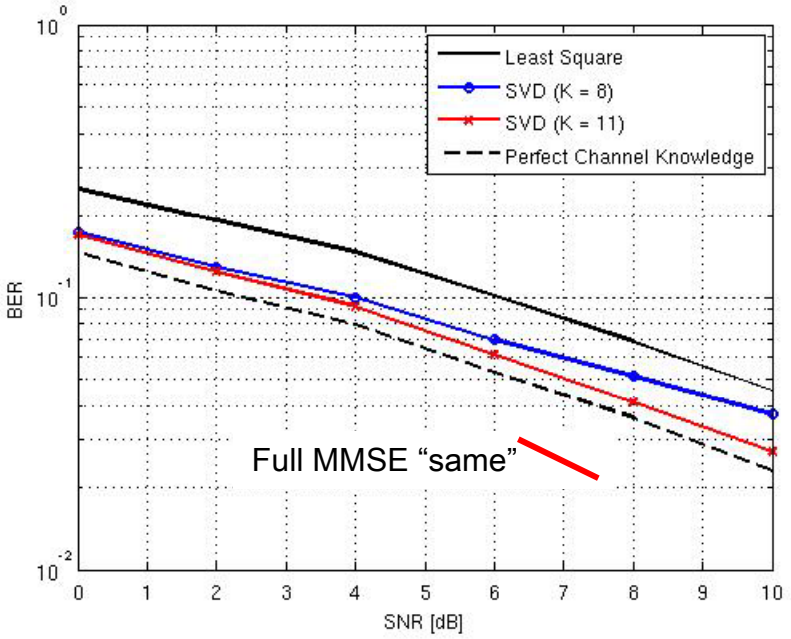


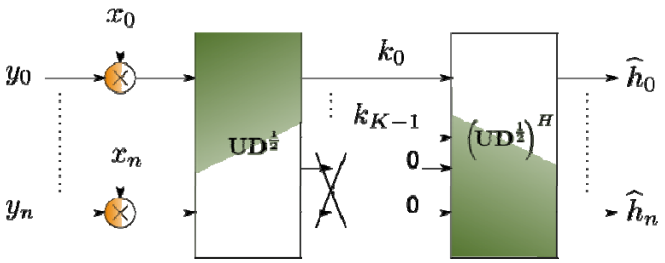
Where K=8 is the length of the Cyclic Prefix, i.e. CP + some.

Presented at NORCHIP 2009

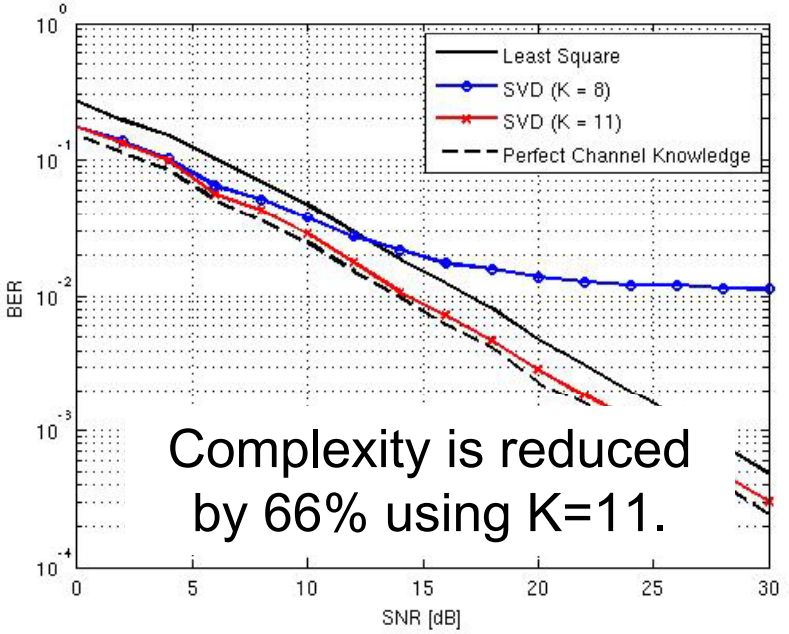
SVD-based Channel Estimation

- SVD reduces the complexity of a linear MMSE estimator
  - A number of values are close to zero and can be ignored.
  - HOW MANY?

$$W = UDU^H = UD^{1/2}(UD^{1/2})^H$$



Conceptual Architecture showing a number of values ignored



Where K=8 is the length of the Cyclic Prefix, i.e. CP + some.

Presented at NORCHIP 2009

SVD-based Channel Estimation

- An architecture using four multipliers has been designed for FPGA and ASIC.
  - FPGA: Functional verification and Resource Usage
  - ASIC in UMC130nm: Area and Power Simulation

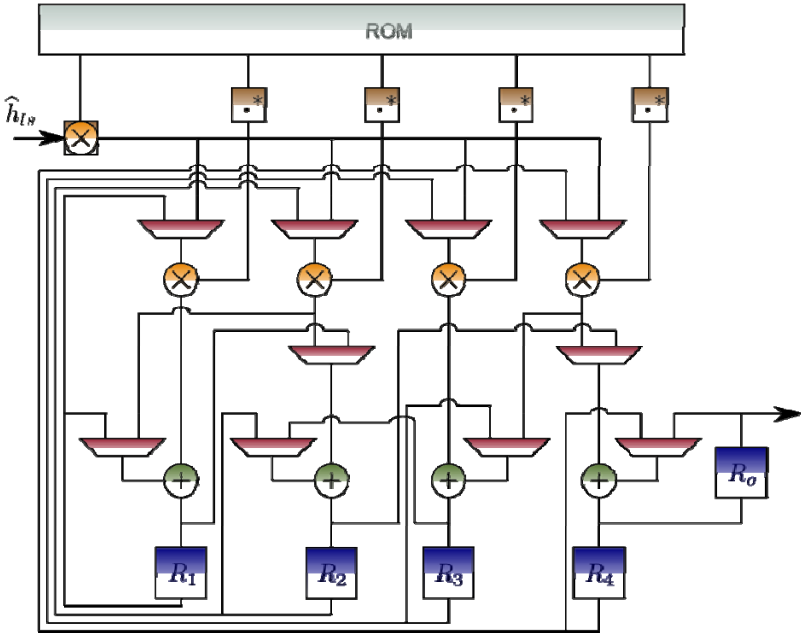


TABLE I
RESOURCE UTILIZATION IN THE XILINX VIRTEX-II PRO

Resource	Used Units	Available Units	Percentage Used
Slices	1304	13696	9 %
Slice Flip Flops	947	27392	3 %
4 input LUTs	2442	27392	8 %
IOs	56		
bonded IOBs	56	556	10 %
MULT18X18s	16	136	11 %
GCLKs	1	16	6 %

TABLE II
SYNTHESIZER REPORT FOR ASIC SYNTHESIS

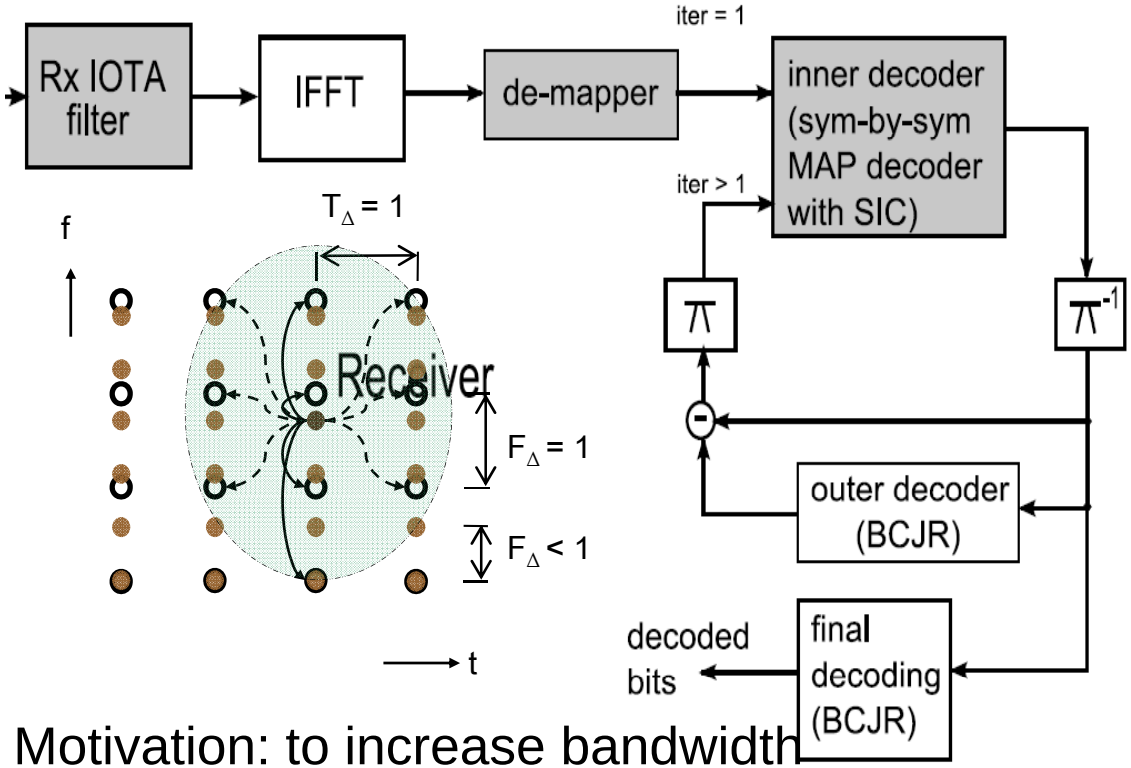
Constraint	Combinational	Noncomb.	Total	Max freq.
Max Speed	1.19 mm^2	0.18 mm^2	1.38 mm^2	179 MHz
Min Area	0.78 mm^2	0.18 mm^2	0.96 mm^2	101 MHz

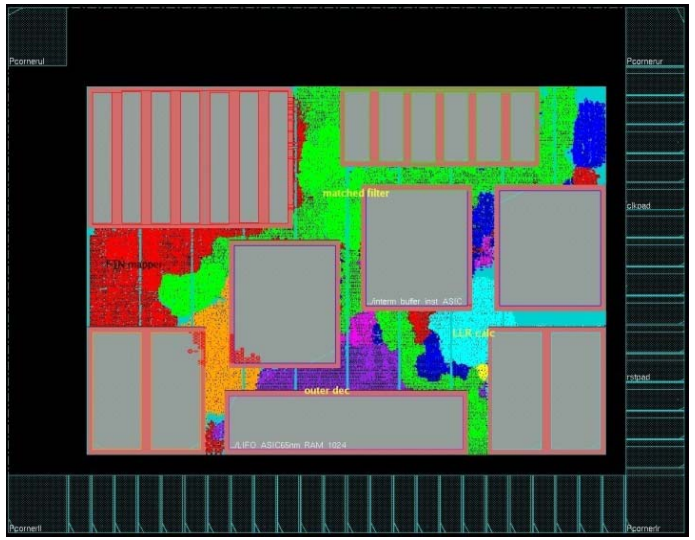
Simulated Power Consumption

- Average power consumption of 14.2 mW
- Peak power consumption 84.5 mW

...and now to: Faster-than-Nyquist (FTN) receiver

FTN iterative receiver





Designed for ST 65nm CMOS
Tape-out in November

Motivation: to increase bandwidth efficiency by compressing in time and/or frequency

Thank You!