A 110dB SNR and 0.5mW Current Steering Audio DAC in 45nm CMOS

Rahmi Hezar, Lars Risbo, Halil Kiper, Mounir Fares, Baher Haroun, Gangadhar Burra, Gabriel Gomez

Texas Instruments

Motivation

Targets:

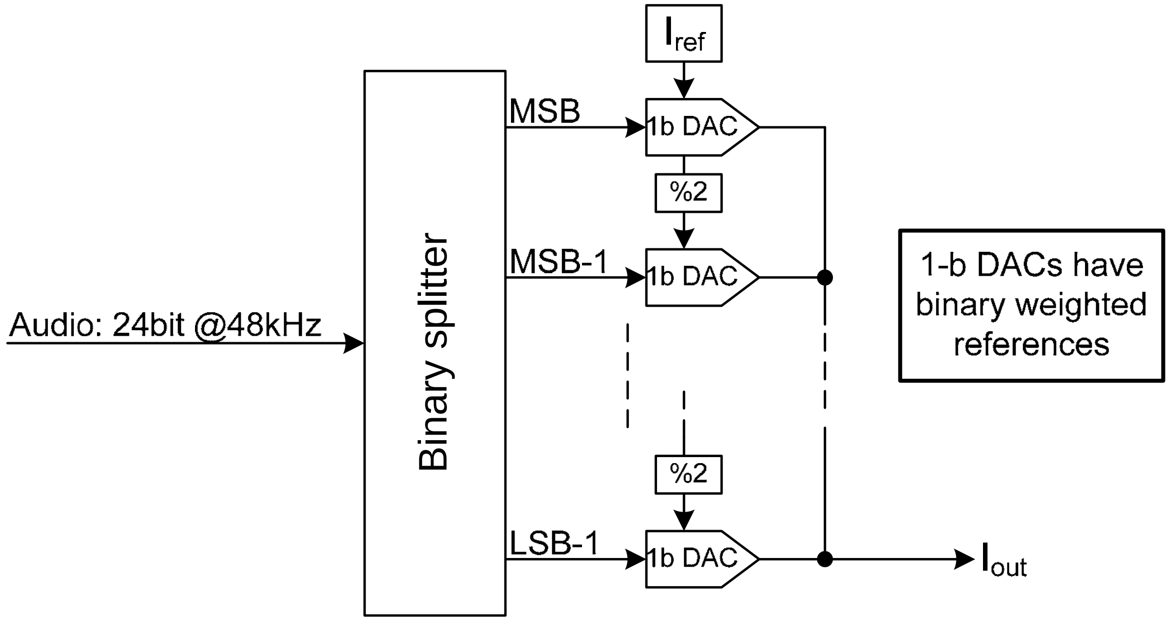
- Performance > 100dB
- Integration into very dense SOCs in standard CMOS (no mask adder)
- Low power consumption
- Low overall area

Method: Take advantage of

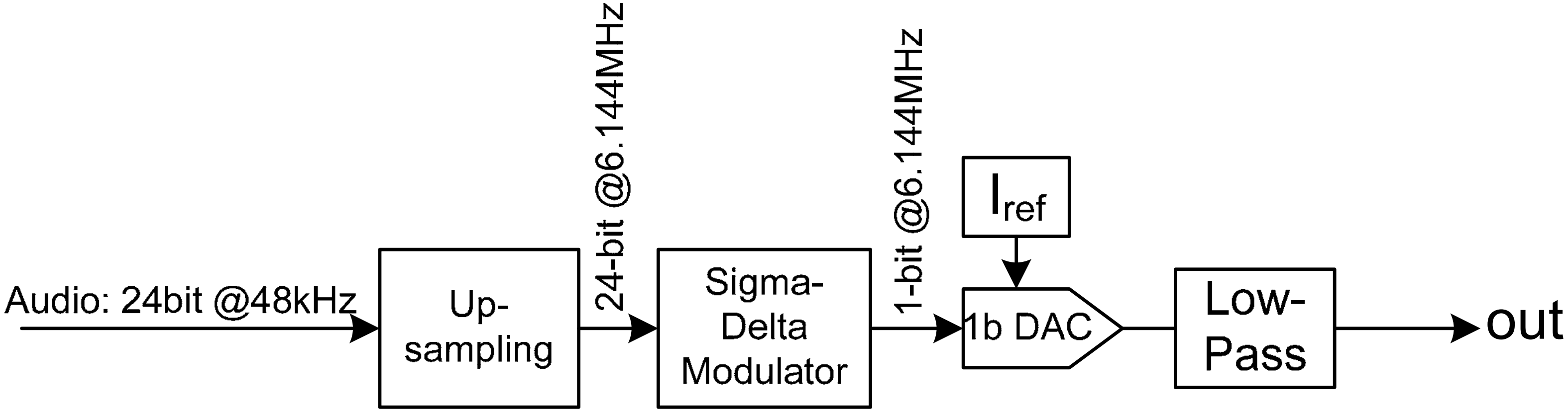
- Digital scaling
- Cheap digital gates
- Fast clocking

The Nyquist-sampling multi-bit DAC (from the CD childhood in the 1980ies)

- Pros
  - No out of band noise
  - Low jitter sensitivity
  - Very simple digital
- Cons
  - DAC control signals are grossly non-linear
    - Individual DAC outputs contain grosss amounts of THD, but cancels out in the final sum (ideal condition)
    - For example, the MSB DAC output is the sign of the input signal (always a square wave)
  - DAC reference mismatch causes cross-over distortion
    - High THD at low levels
    - Laser trimming needed to get better than ~12-14 bits THD



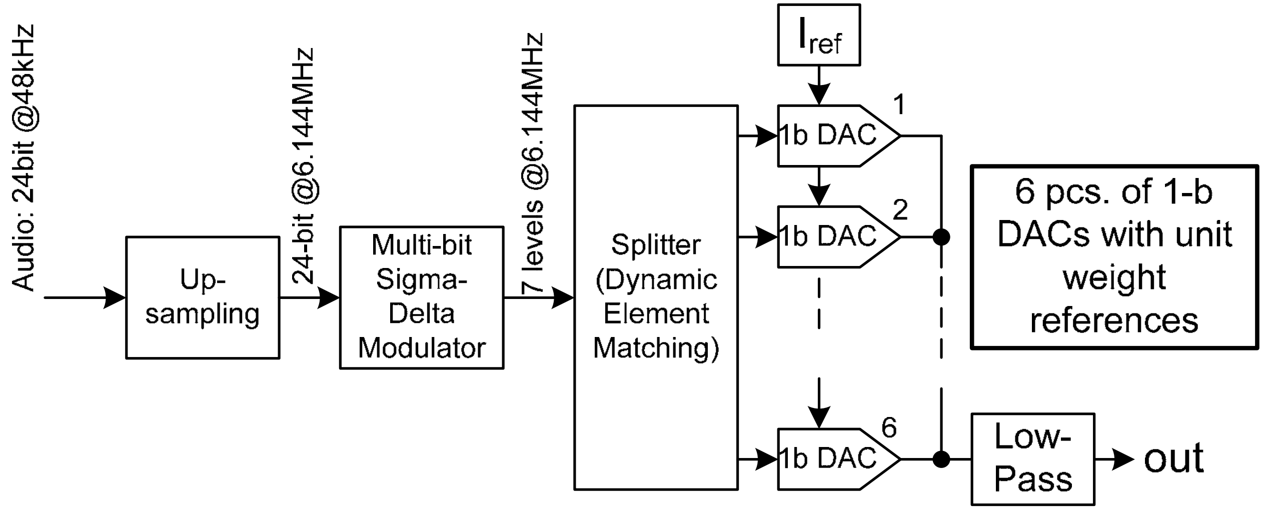
1-bit SDM DAC (1990'ies)



- Pros
  - Immune to mismatch (only one 1bit DAC)
  - No cross-over distortion
  - Immune to static amplitude non-linearities on the 1-bit signal

- Cons
  - Huge amount of out of band noise
  - Low-pass filter is demanding
    - High precision
    - Complex
    - Burns much power
  - Very sensitive to dynamic/ISI errors of the DAC
  - High jitter sensitivity (unless the filter is done as Switched Cap)

Oversampled multibit DACs



- Pros
  - Reduced out of band noise compared to 1bit
  - Relaxed filter requirements
  - Reduced jitter sensitivity
  - Individual 1bDAC signals contain the audio signal plus high-pass shaped noise
  - Mismatch error is high-pass shaped (1-st order using simple DWA rotation and 2nd order using 2nd order DEM with higher complexity)
    - Tolerant to DAC mismatch

- Cons
  - Still has many of the draw backs of the 1-bit DAC
  - Many segments needed to reduce the out of band noise and jitter sensitivity
  - Still high sensitivity to dynamic errors on the 1bDACs
  - The filter is still a challenge
  - Complex Splitter/DEM needed

DAC using 4:1 weighting on elements
Bob Adams (ADI), ISSCC'98

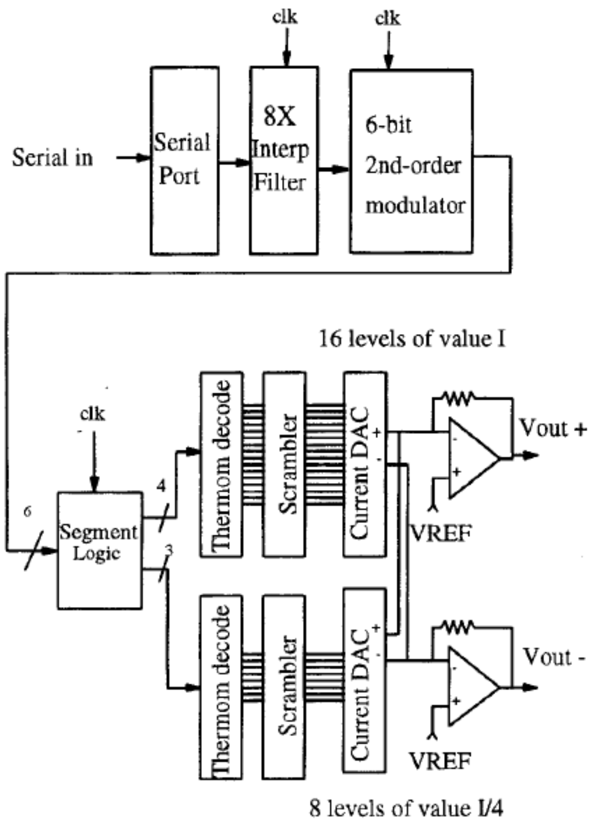


Figure 1: Chip block diagram (1 channel of 2).

3204:
~12 effective levels
(incl. The AFIR)
6x4=24 segments used

ADI:
64 effective levels
8+16=24 segments used

—

ADI has about 12dB less
out of band noise

4:1 weighting maps well into a process with good matching

Still mismatch shaping

More efficient "middle of the road" approach between unit- and power of two weighting

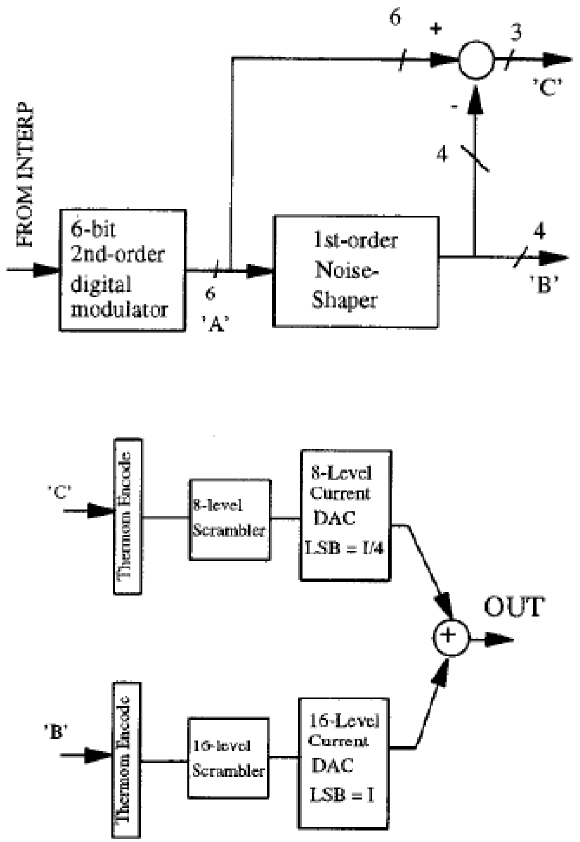
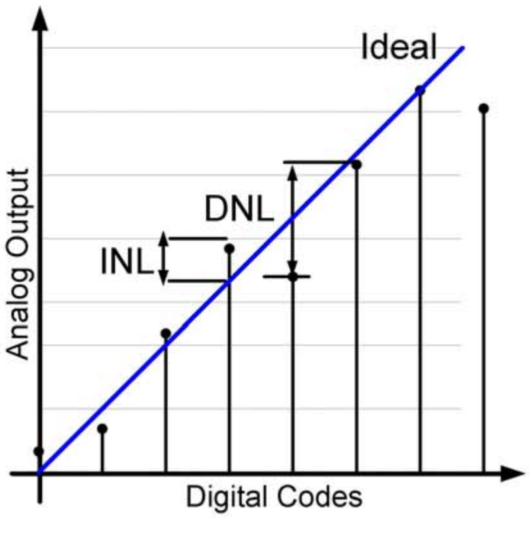


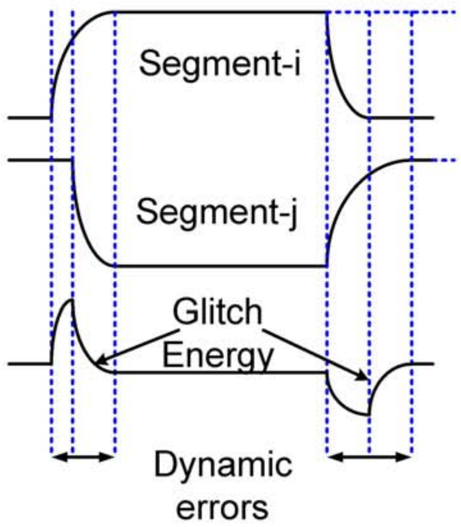
Figure 2: Noise-shaped segmentation circuit.

Dominant Error Sources

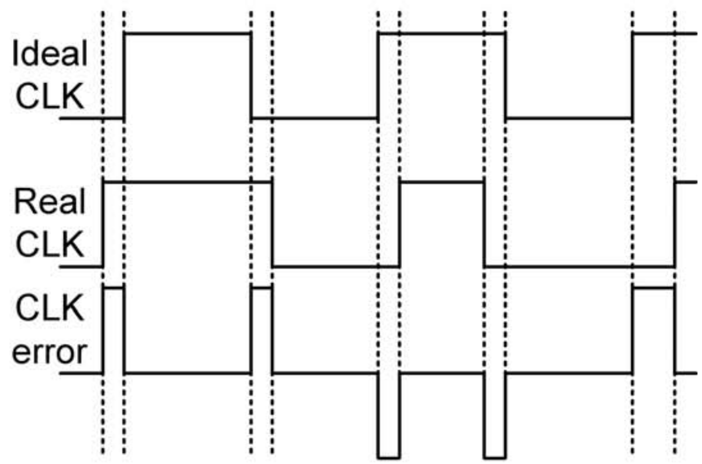
- DAC Element Mismatch
- DAC Asymmetrical Switching (ISI)
- Clock Jitter
- Amplifier Nonlinearity



Element Mismatch

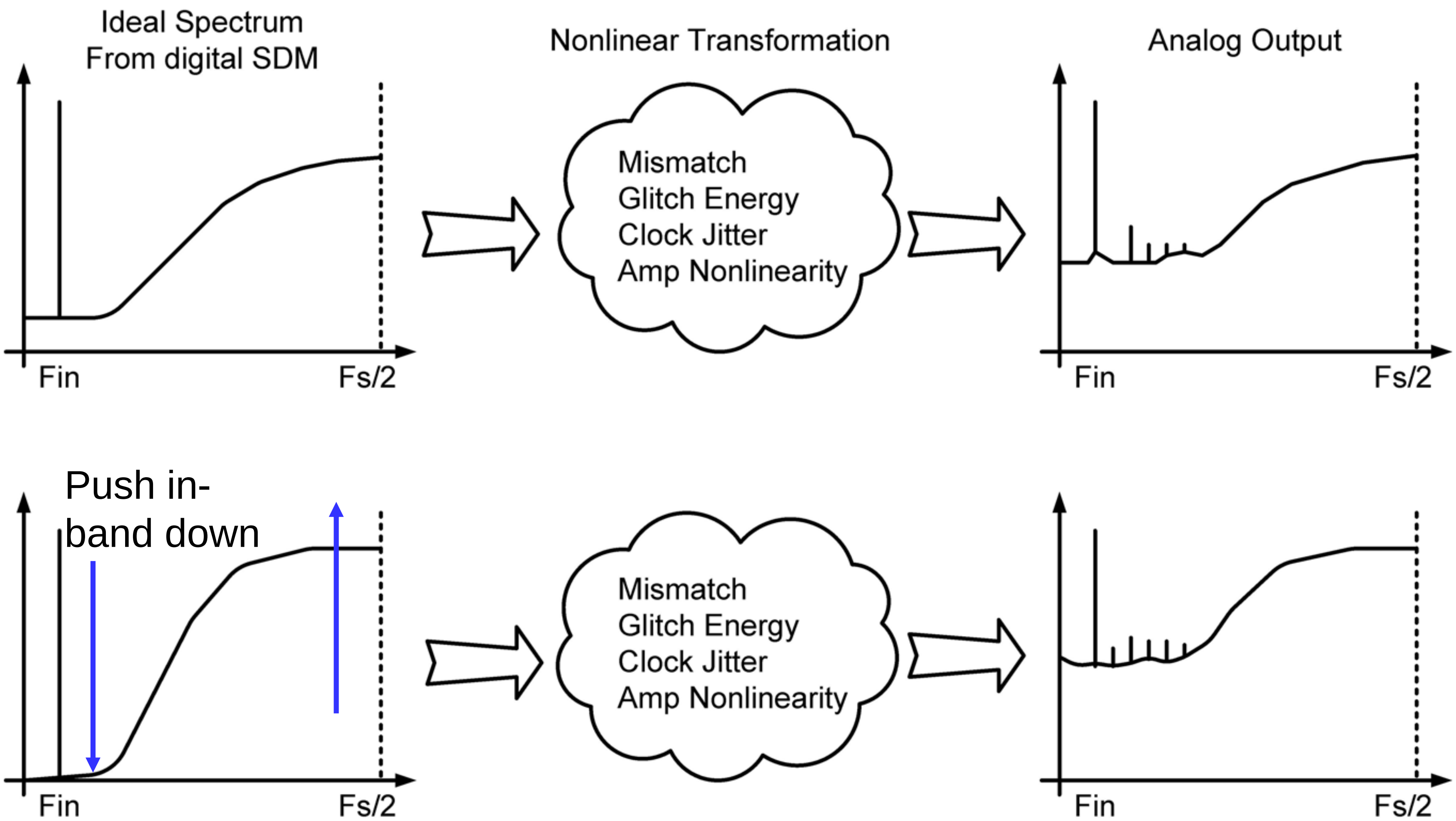


Asymmetrical Switching



Clock Jitter

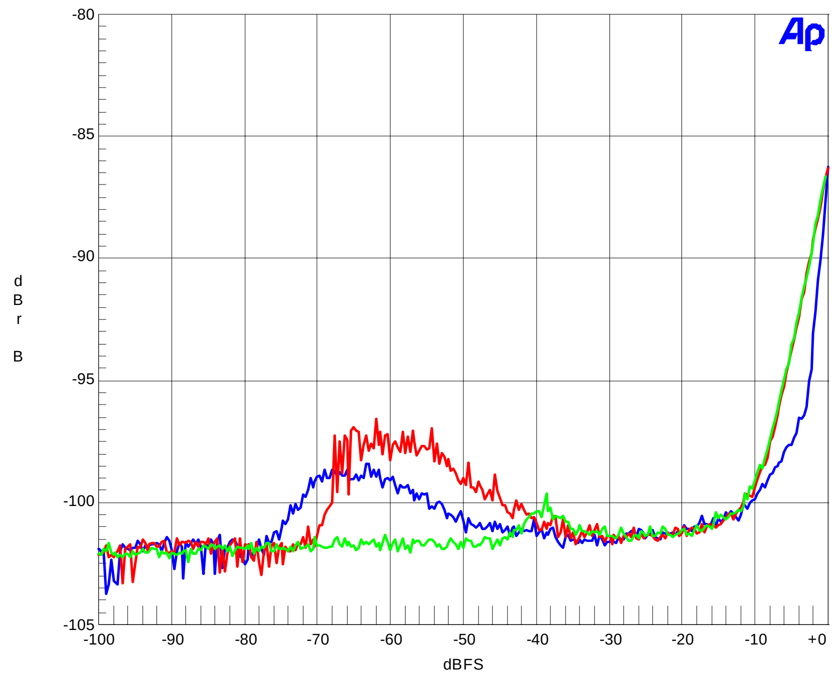
Impact of DAC Non-linearity



➢ We need to reduce out of band noise

Example: DAC prototype problem

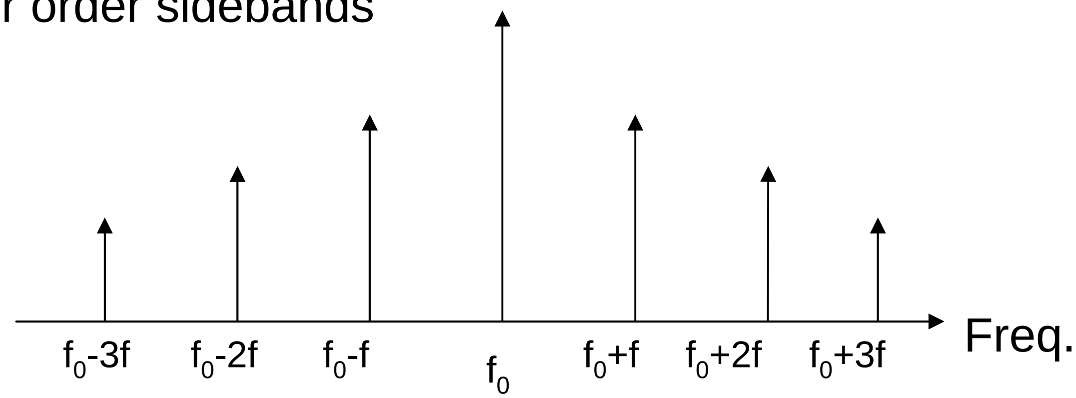
- Issue: bumps on the THD+N vs level graph
- Ruins the DNR datapoint at -60dBFS input signal
- Bump is due to harmonics
- What is the root cause?
  - Problem identified to be due to modulator tones



FM modulation theory

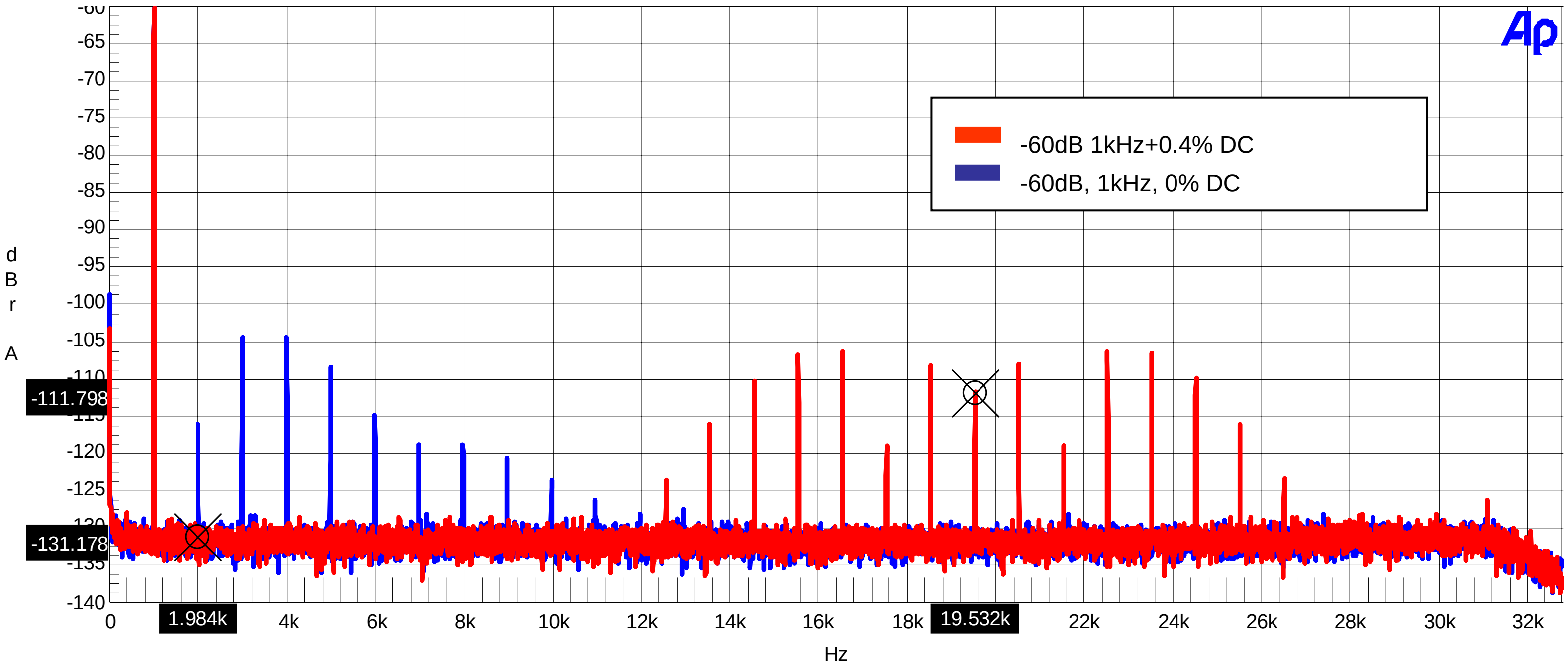
- A sinusoidal carrier at frequency f_0 is FM modulated by a signal with frequency f and amplitude A (e.g. audio signal)
- The FM modulation produces side bands at offset frequencies being harmonics of the audio signal frequency f
- The relative amplitude of the harmonic side-bands are given by Bessel functions
  - $J_n(K_{FM}A/f)$
  - Where n is the harmonic offset, A is the modulation amplitude and K_{FM} is the voltage-to-frequency scaling constant (Hz/Volt), f is the modulation frequency (audio signal) and J() is the Bessel function

- AM (amplitude) modulation only produces 1st order sidebands and not the higher order sidebands



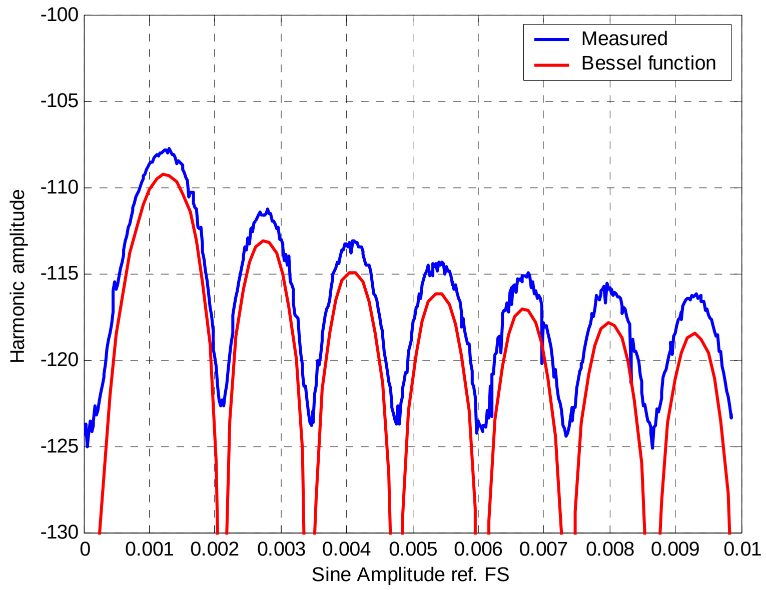
Validation of the FM theory using the DAC prototype

- 0.4% DC offset moves the carrier from 0Hz to ~19.5kHz (K_{FM}=4.88MHz/FS)
- Side-bands at 19.5kHz+-n*1kHz as expected, side-band amplitudes match the harmonics for zero DC offset
- Red graph with DC offset is a translation of the blue (zero DC offset) graph
- This behaviour excludes any amplitude nonlinearity as the mechanism behind the harmonic distortion



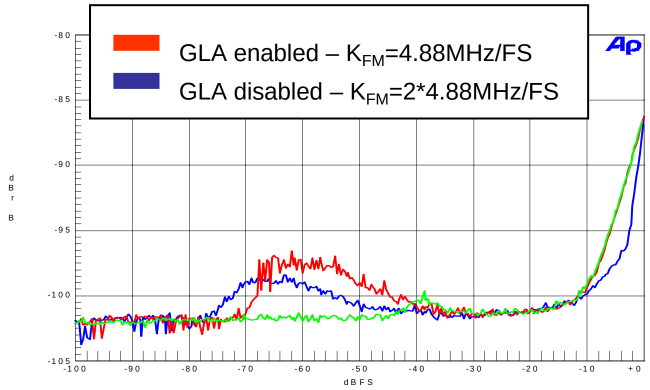
Comparison to measurements

- Plot showing the 2nd harmonic amplitude versus input amplitude for K_{FM}=2.44MHz/FS (FS=Full scale digital input) and input frequency f=1kHz
- K_{FM} was found by applying a small DC and measuring the tone frequency
- Measurements match FM theory very well
- **Such strongly frequency and amplitude dependent THD cannot be explained by the usual on-linearities such a cross-over distortion etc.**

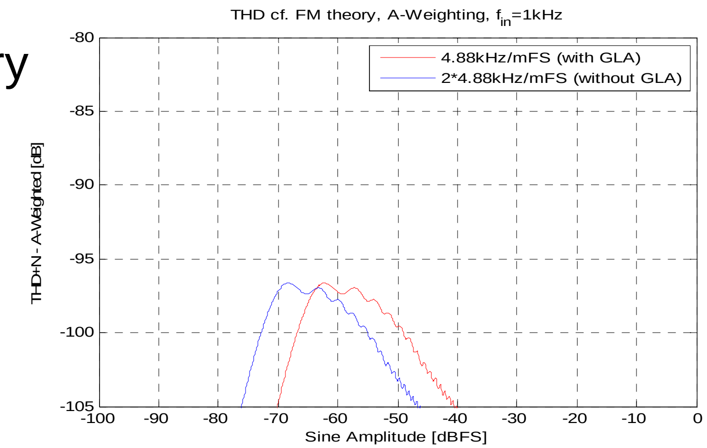


THD+N vs Amplitude plots

Measured



FM-theory

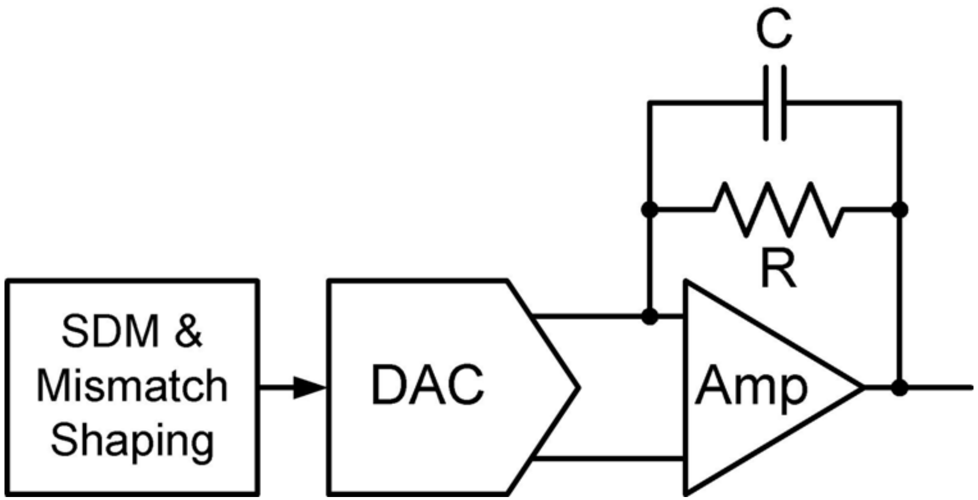


- Theoretical plot uses K_{FM} and tone amplitude matched from DC-input measurements
- THD+N drops off at higher amplitudes, sinces the harmonics spread across a wider and wider bands
- THD+N drops off fast at low amplitudes
- Measurements match theory very well
- Blue graph is for disabled GLA where the K_{FM} doubles – which gives a shift on the THD+N "bump"
  - Again mathcing measurements!
- **ISSUE: The FM harmonics dominate the THD+N at -60dB, ie. The DNR is degraded by 5-7dB due to the tone problem**
- **We need to suppres the tone!!**
  - **The tone is the root cause**

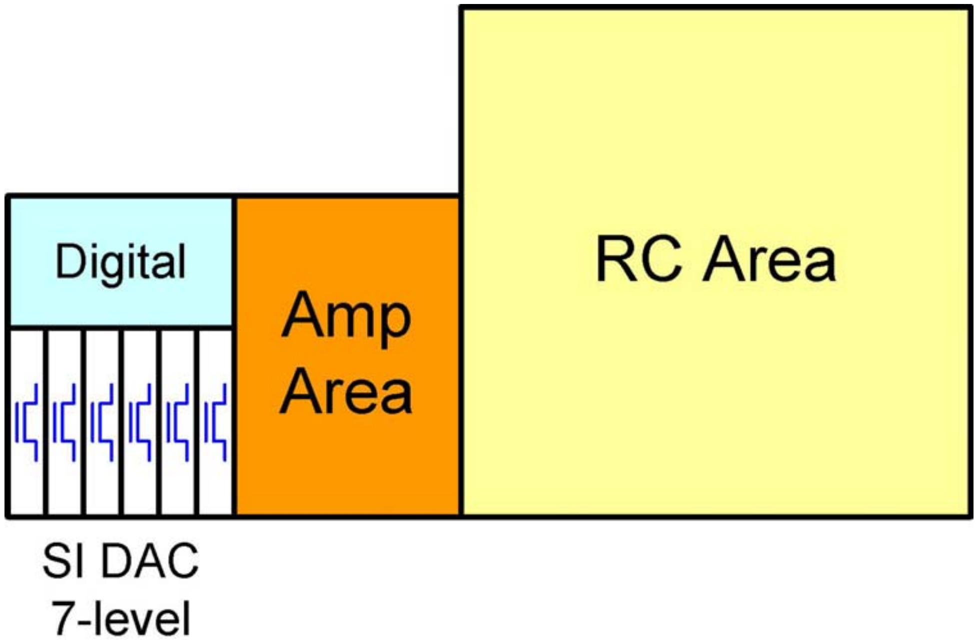
Root cause of the FM tones

- The popular and simple DWA (GLA) is a rotation scheme:
  - circular pointer
  - Pointer index incremented by the segment count every sample
  - The rotation speed is proportional to the signal
- This is almost like a VCO
  - We simply get FM modulation...

Cost of Filtering OBN

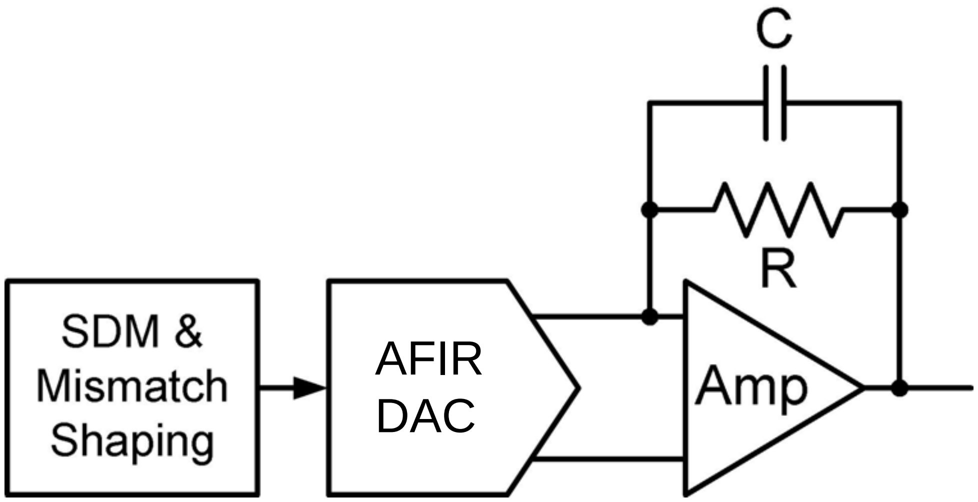


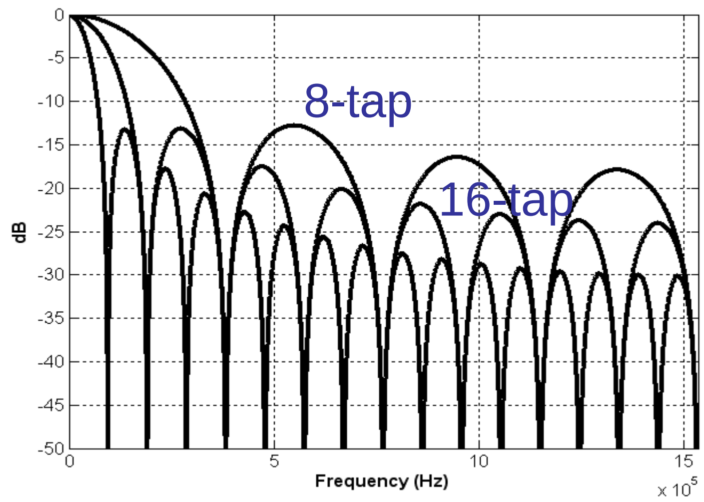
Classical RC Filtering of out of band noise

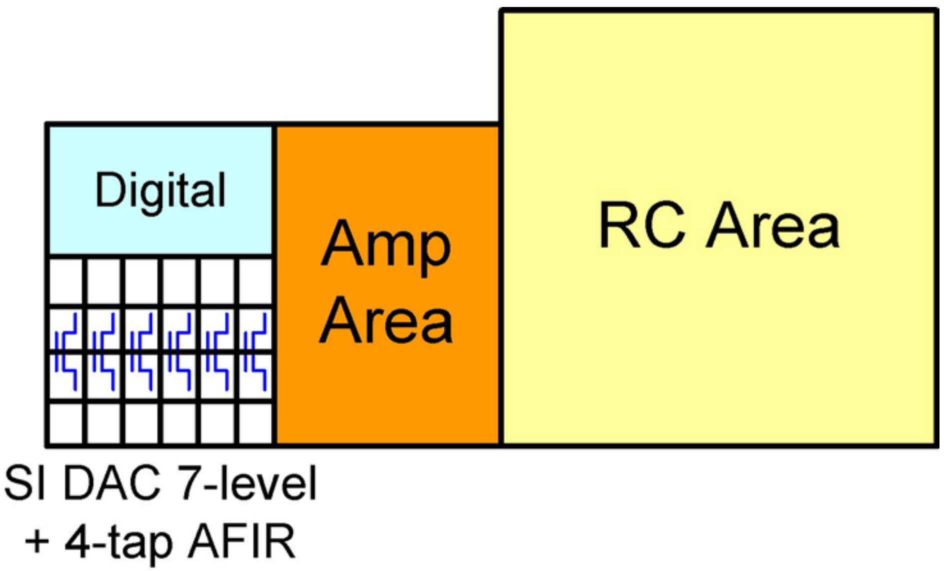


Area usage is dominated by RC filtering

Try Analog-FIR Filtering

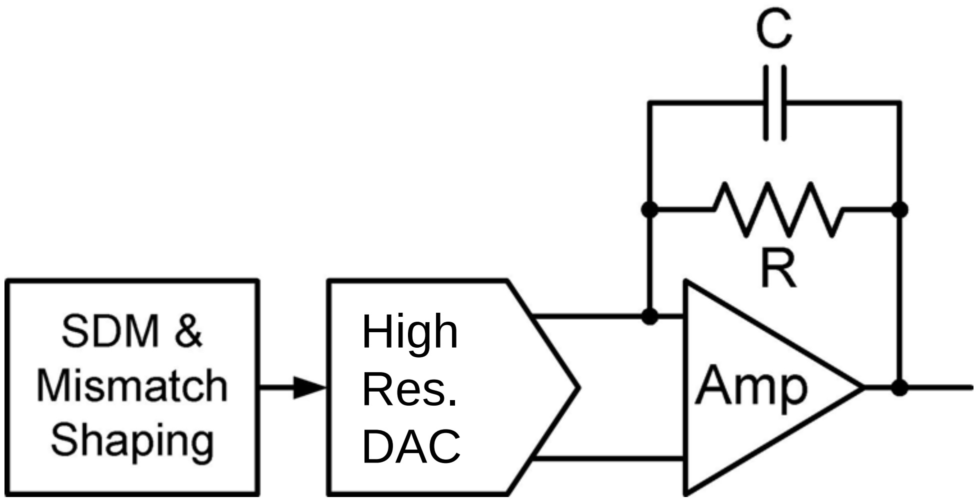




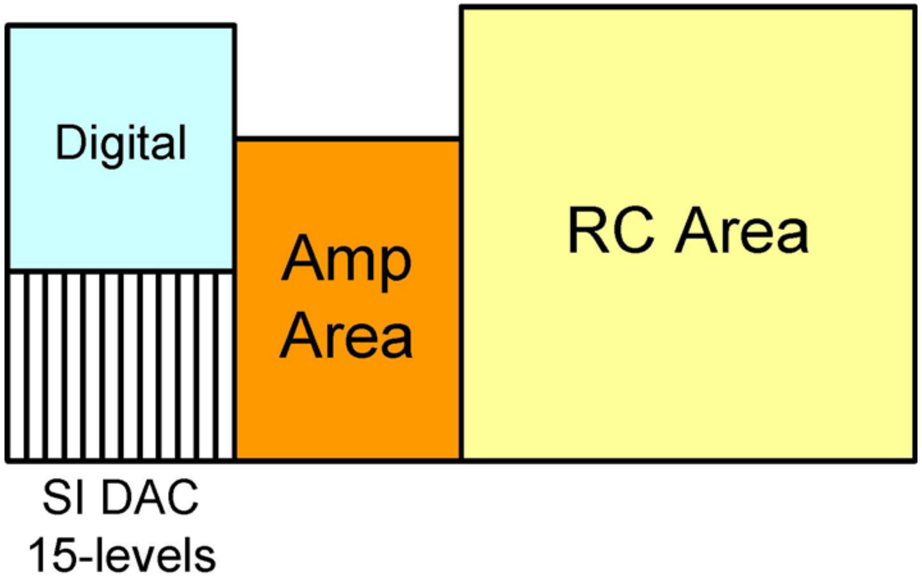


Unity FIR does not provide enough suppression.

Try Adding More Quantizer Levels

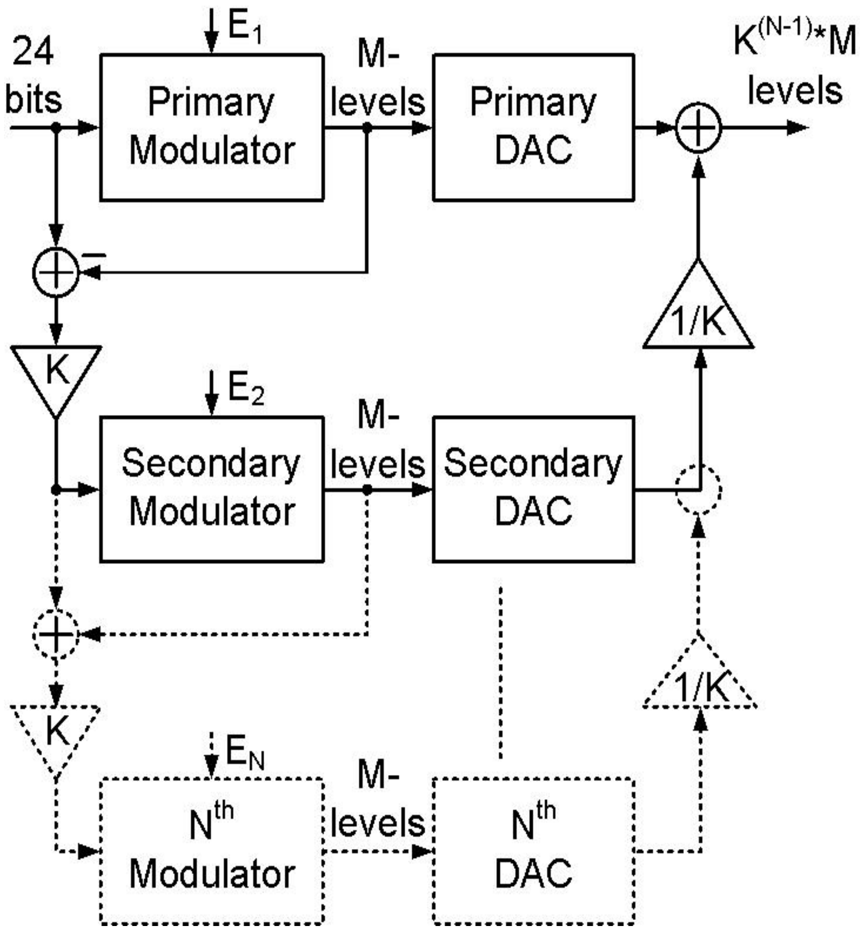


Increase quantizer resolution in the modulator



Similar type of reduction to AFIR plus the digital complexity

Cascaded Modulator Architecture



For a 2-level cascade

$$Y(z) = X(z) + \frac{1}{K} \cdot NTF(z) \cdot E_2(z)$$

Resolution is boosted by K.

For N-level cascades

$$Y(z) = X(z) + \frac{1}{K^{N-1}} \cdot NTF(z) \cdot E_N(z)$$

Impact of Mismatch on Resolution

- Ideal output for a 2-level cascade

$$Y(z) = X(z) + \frac{1}{K} \cdot NTF(z) \cdot E_2(z)$$

- If digital Kd and analog Ka do not match

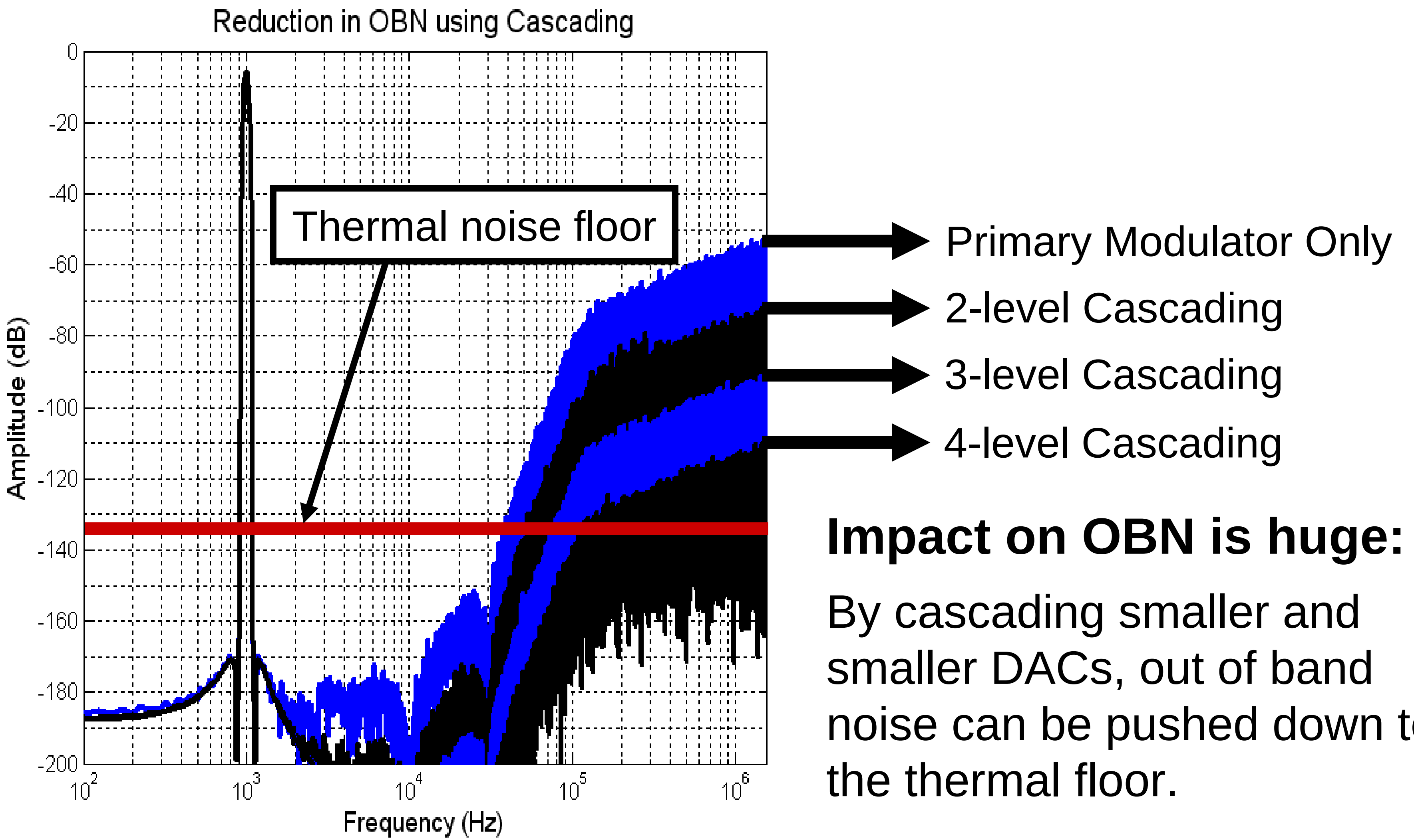
$$Y(z) = X(z) + \left(1 - \frac{K_d}{K_a}\right) \cdot NTF(z) \cdot E_1(z) + \frac{1}{K_a} \cdot NTF(z) \cdot E_2(z)$$

- Mismatch between Kd and Ka is shaped inherently
- Mismatches between the DACs are shaped similarly

This is not MASH

- Purpose of MASH is to get higher order from simple 2nd and 1st order modulators.
  - Same can be achieved with higher order single loop
  - The purpose of Cascade is to get finer quantization from coarse quantized modulators.
- MASH sub-modulators are summed in digital domain always
  - Cascaded modulators are summed in analog domain.
- MASH is very sensitive to analog/digital mismatch
  - Cascaded architecture has built in shaping

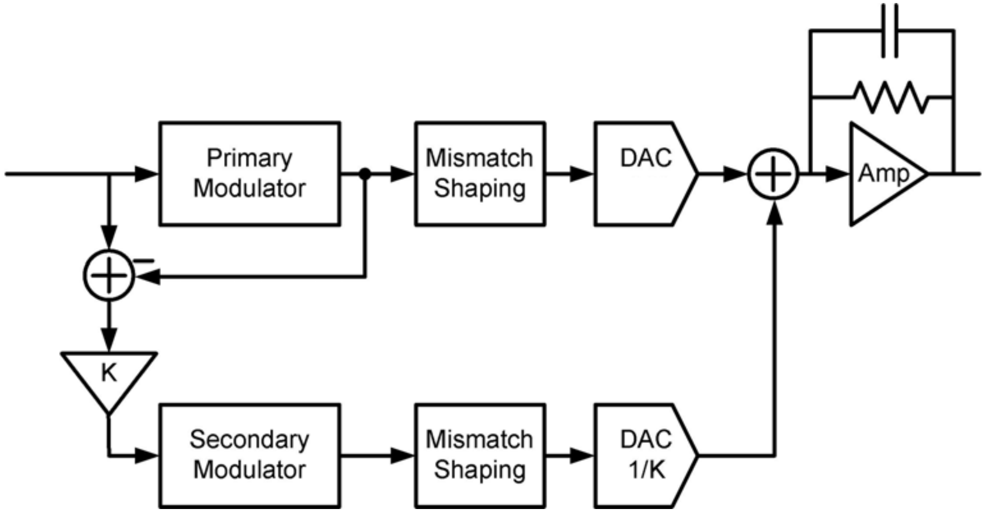
Reducing OBN Cost Effectively



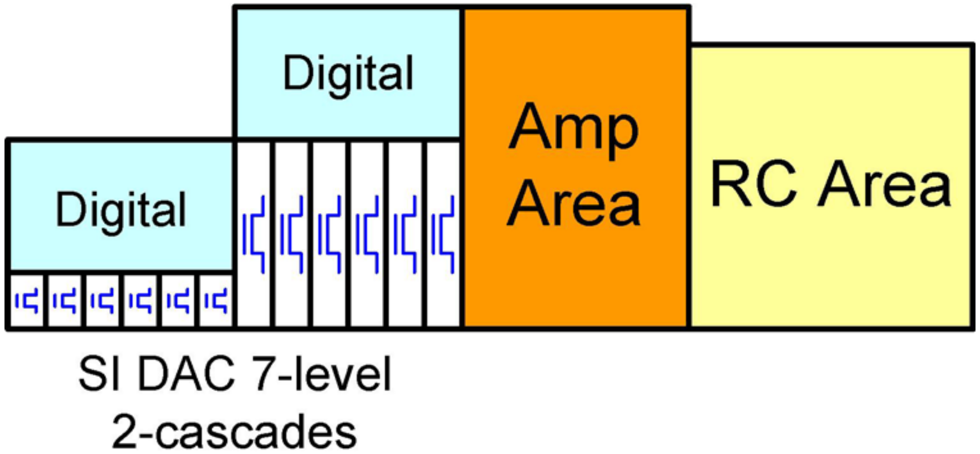
Impact on OBN is huge:

By cascading smaller and smaller DACs, out of band noise can be pushed down to the thermal floor.

Impact of Cascading on Area

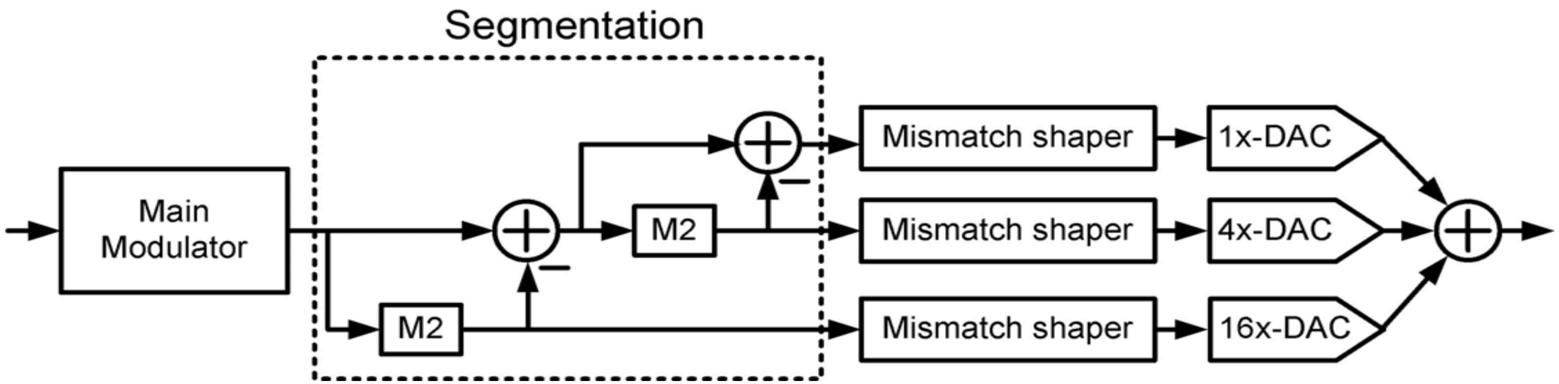


Cascaded architecture with secondary DAC

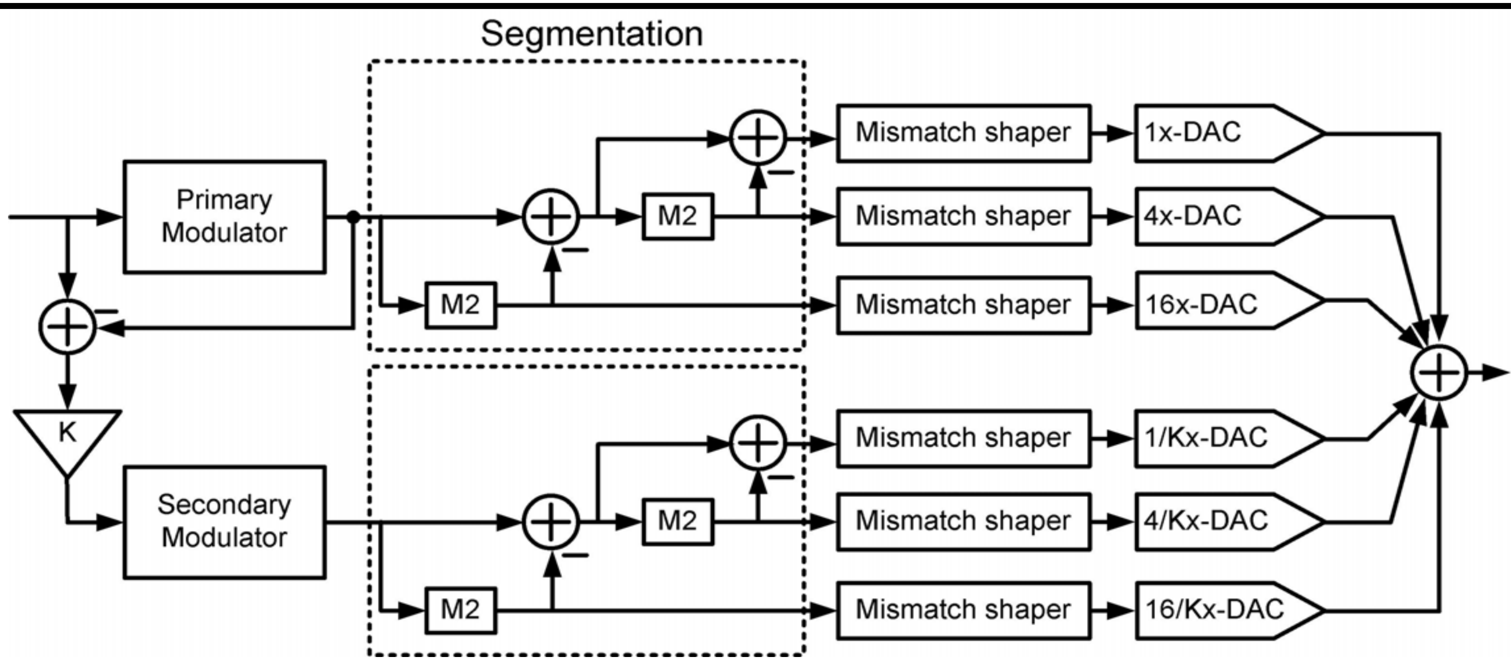


Resolution is increased significantly with a small DAC

Comparing to Segmented DACs

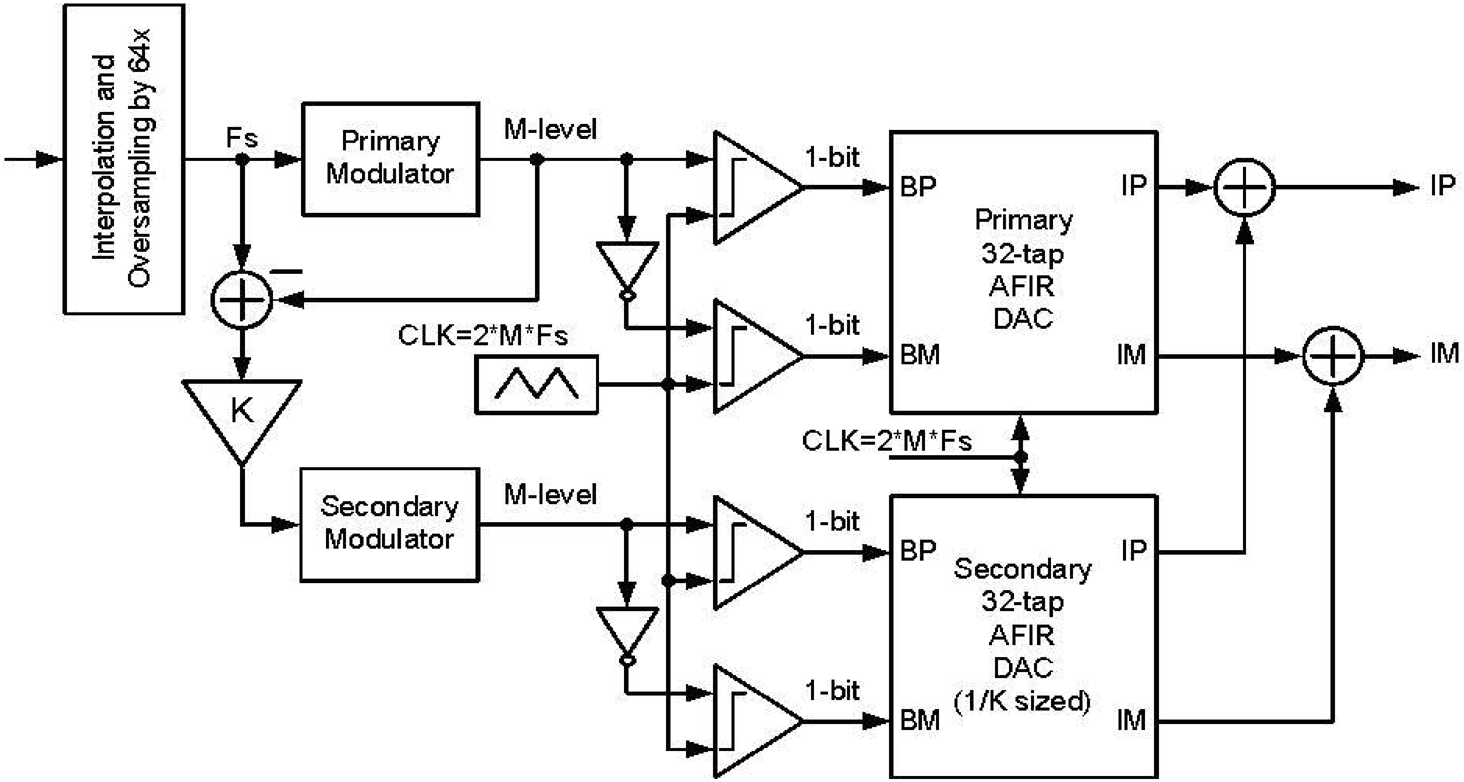


Segmentation is used for high resolution modulators



Segmentation and Cascading are not exclusive

Using PWM and AFIR in DAC

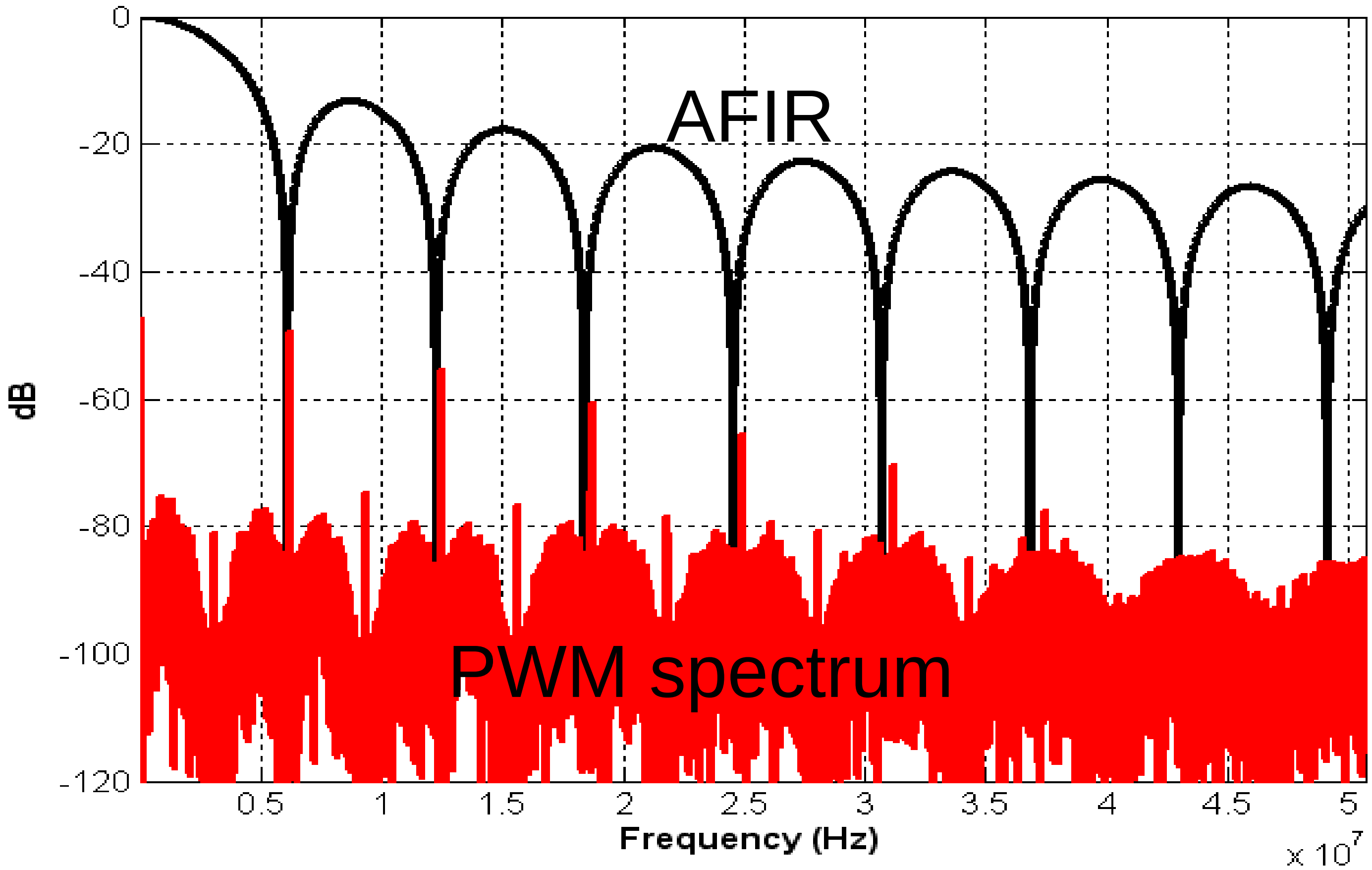


PWM: M-level data @ Fs → 2-level data @ 2*M*Fs

– 1-bit data is inherently insensitive to mismatch

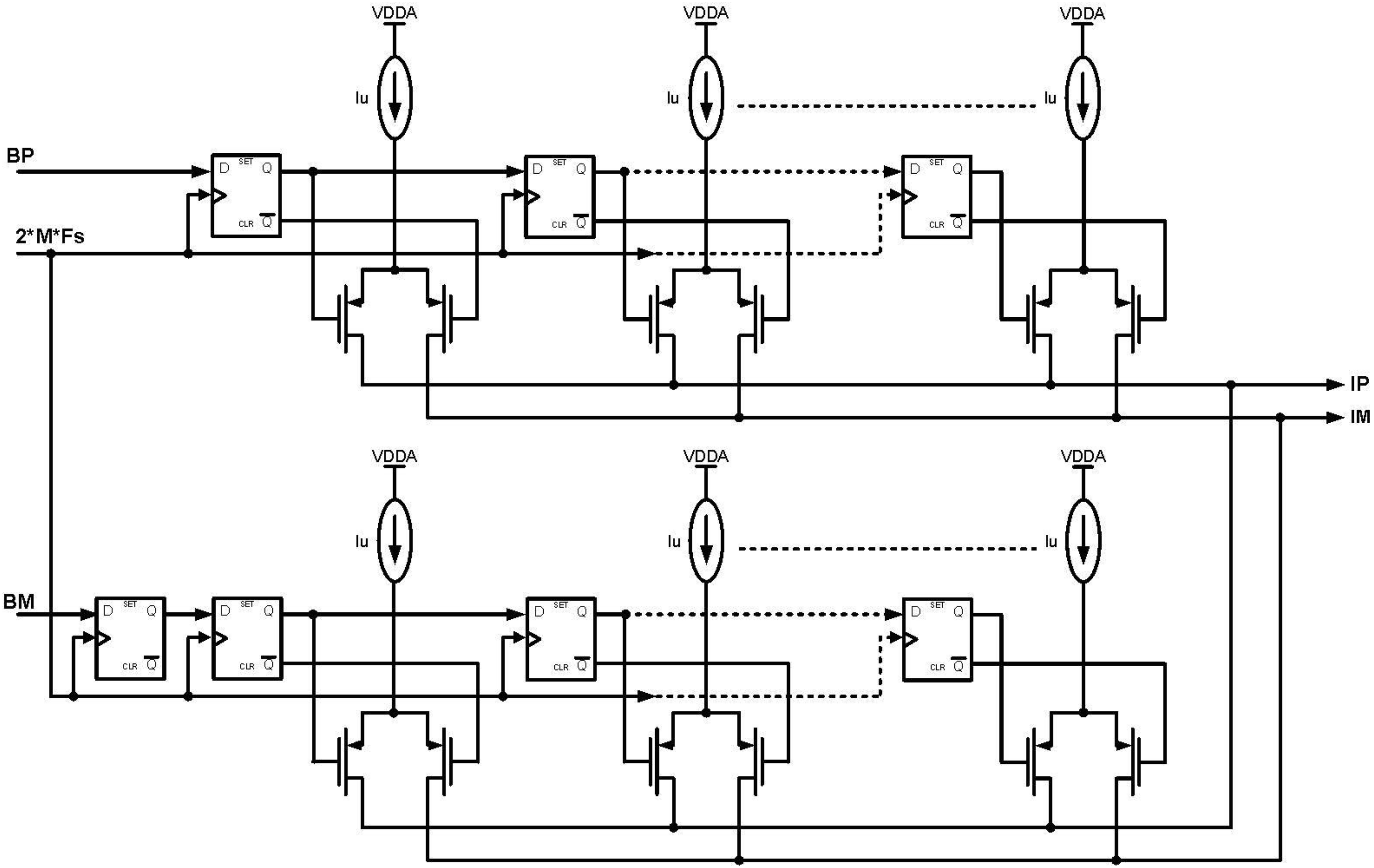
– Reduced sensitivity to asymmetrical switching

AFIR and PWM Spectrum

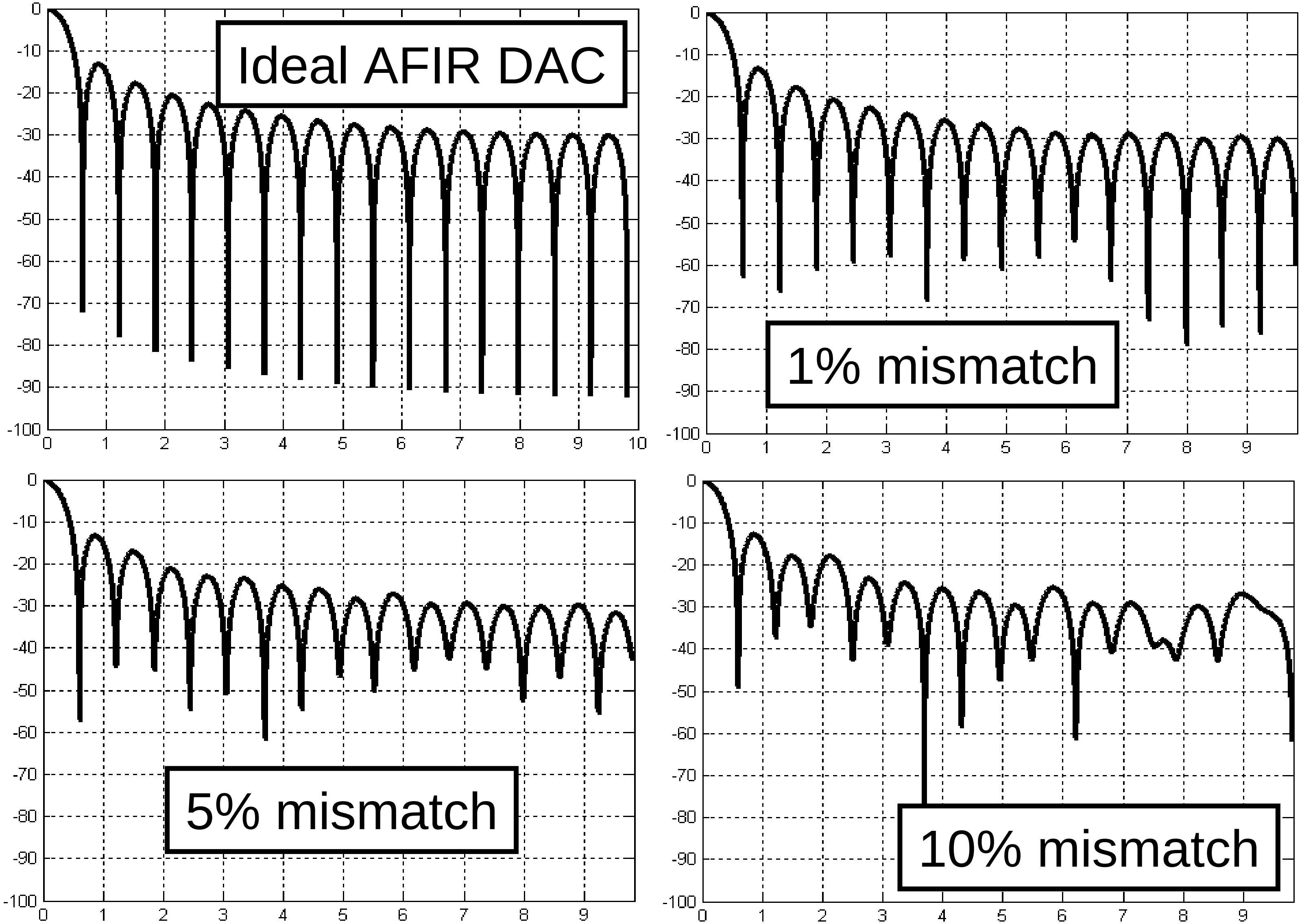


- AFIR notch locations align with PWM harmonics

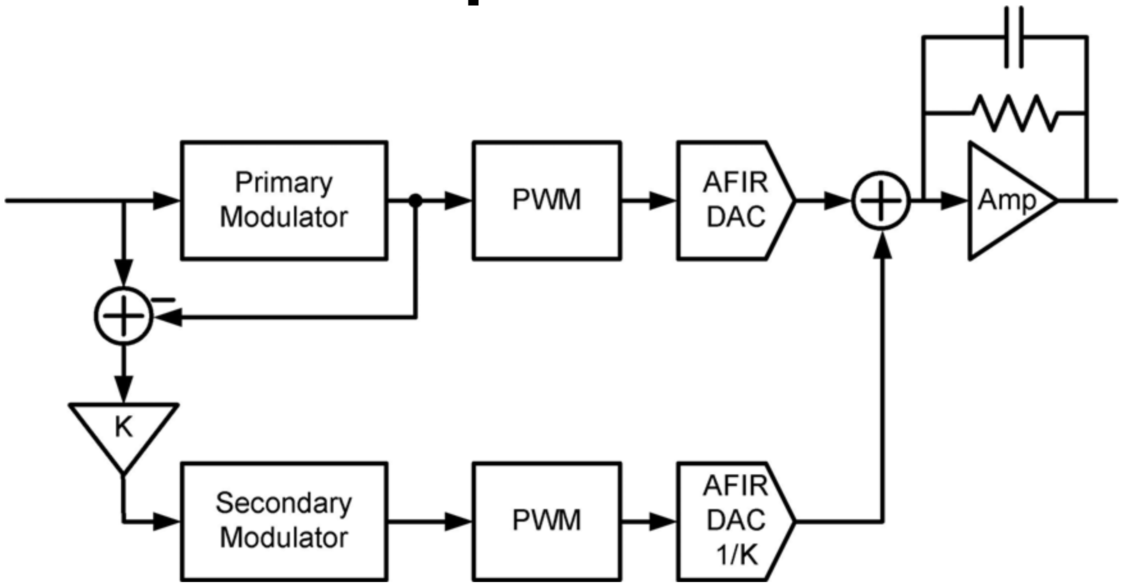
AFIR DAC Circuit



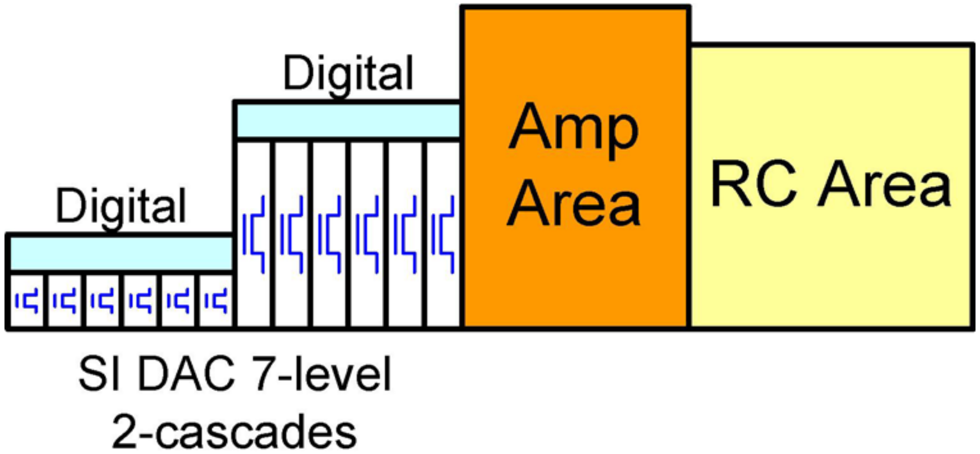
Effect of Mismatch on AFIR



Impact of PWM on Area

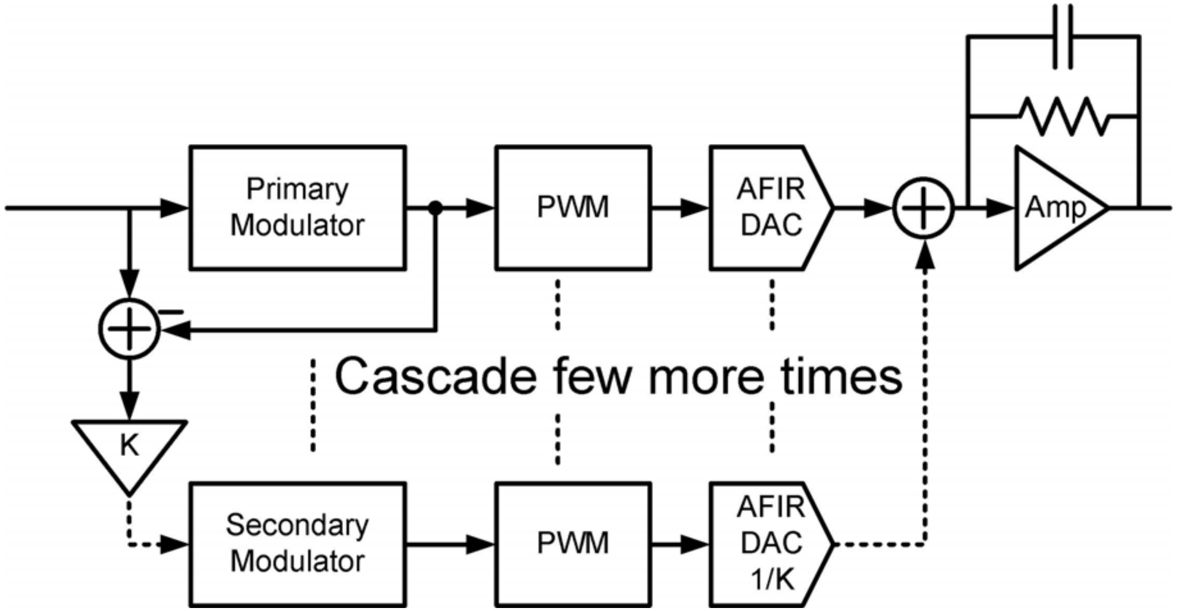


2-level Cascaded architecture with PWM and AFIR

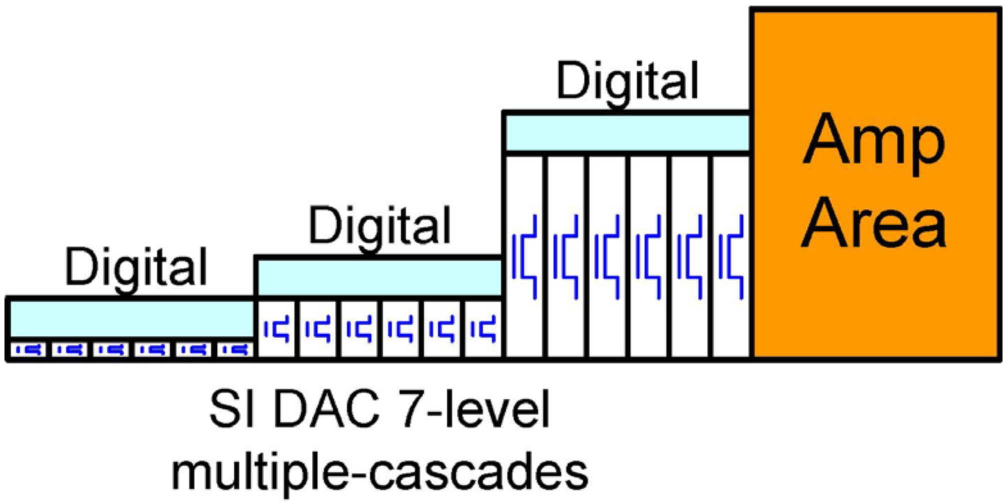


- Digital PWM costs nothing in gates.
- Resistant to mismatch and ISI
- Clock faster

Keep Cascading

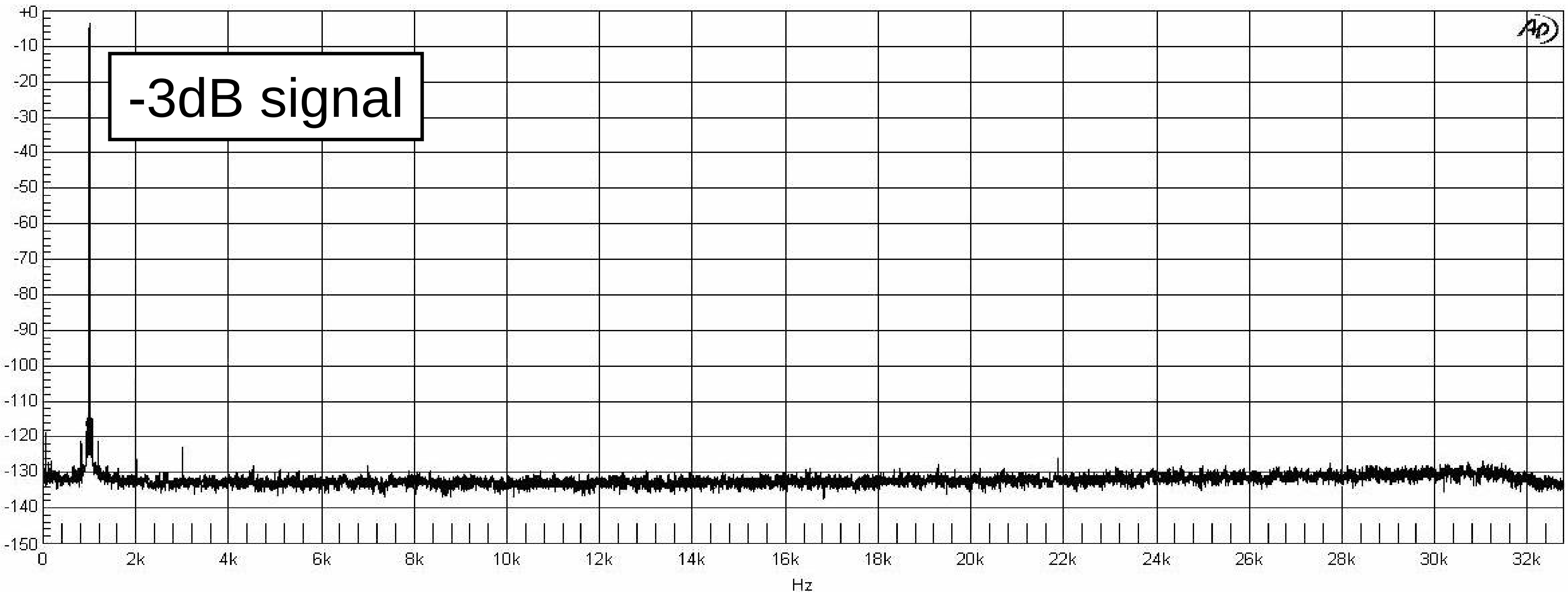


Multiple cascades combined with PWM and AFIR



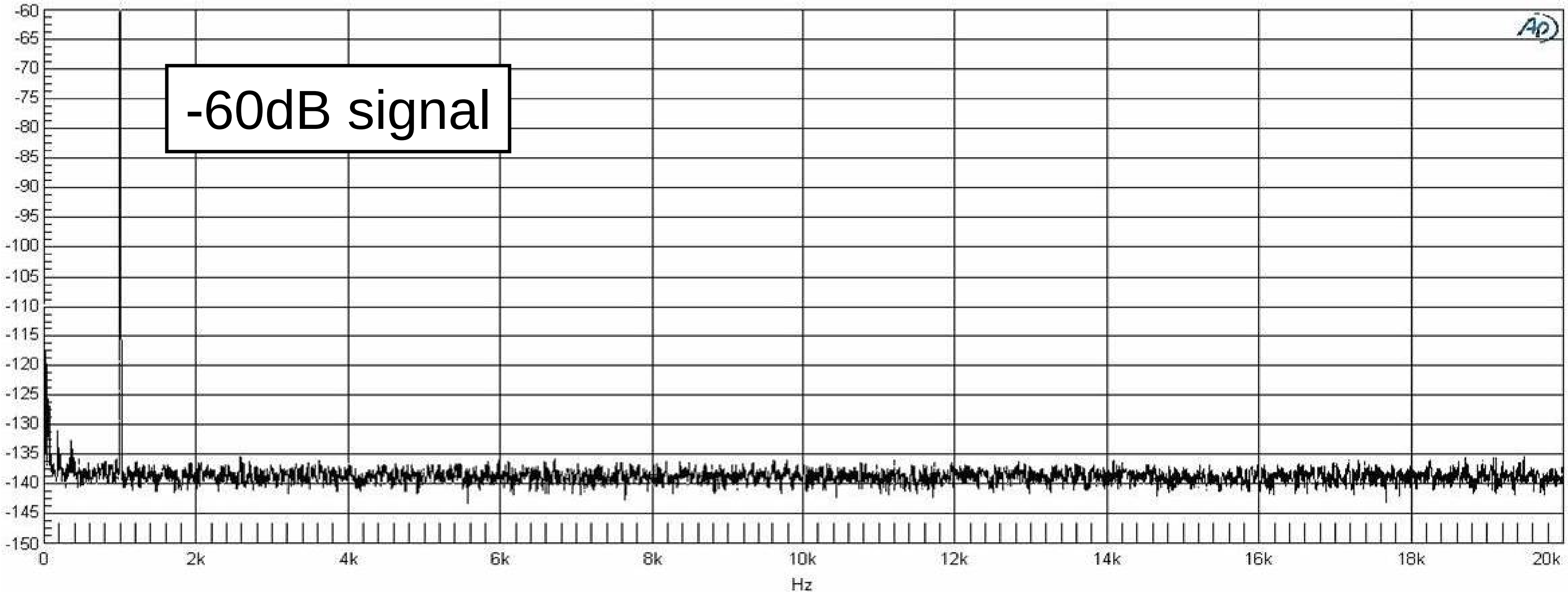
Can eliminate Cap area completely

Measurement Results



- Very low distortion at -3dB signal
- 2nd harmonic is down by 120dB
- 3rd harmonic is down by 118dB
- 60 Hz is visible around signal and DC

Measurement Results

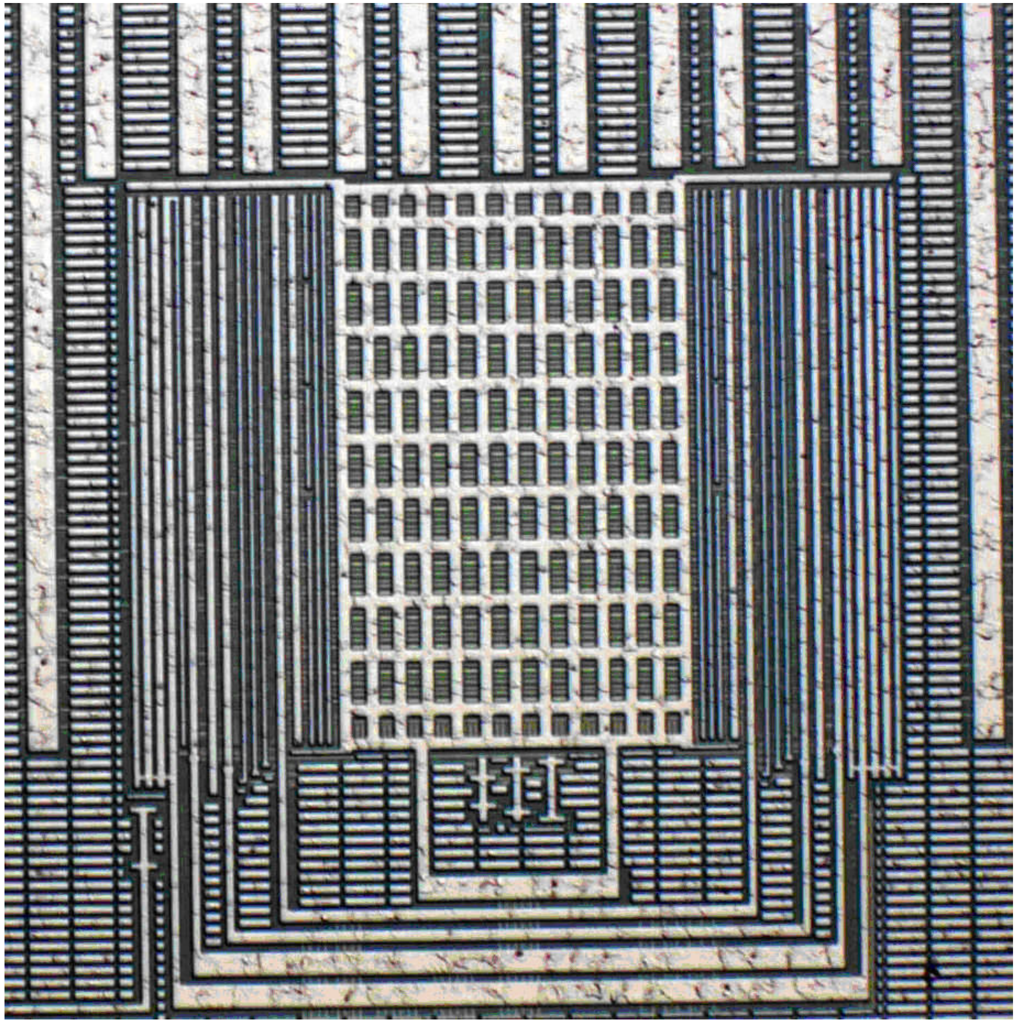


- ➢ No spurs and idle tones visible at low signal swing either
- ➢ 60 Hz and its harmonics is still visible around DC

Performance Summary

Process	45nm CMOS
Supplies	1.4V Analog/1.1V Digital
Full-scale differential output	176uA peak to peak
Digital power/DAC	0.1mW
Analog power/DAC	0.4mW
Total DAC area	0.045mm2
OSR	64
Clock Frequency	3.072MHz modulator clock 202.752MHz DAC clock
Dynamic Range (A-weighted)	110dB
THD+N	-100dB

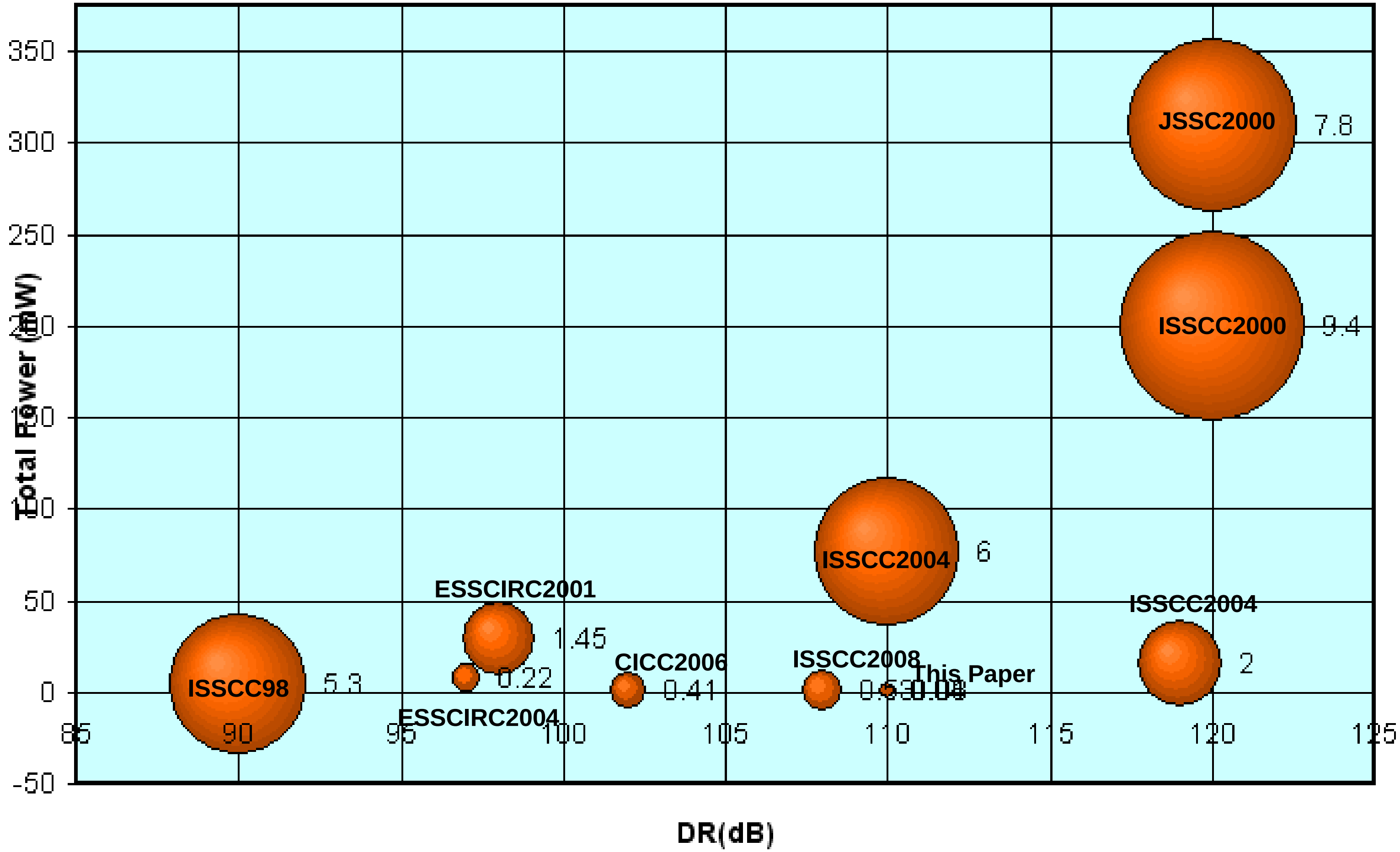
Die Micrograph



Summary

- Cascaded Modulator Architecture reduced out of band noise efficiently
  - Reduced sensitivity to analog error sources
  - Reduced RC area cost for post filtering
  - Analog amplifier design requirements are relaxed too.
    - Smaller dV/dt transitions allow a slower amplifier with low area and power.

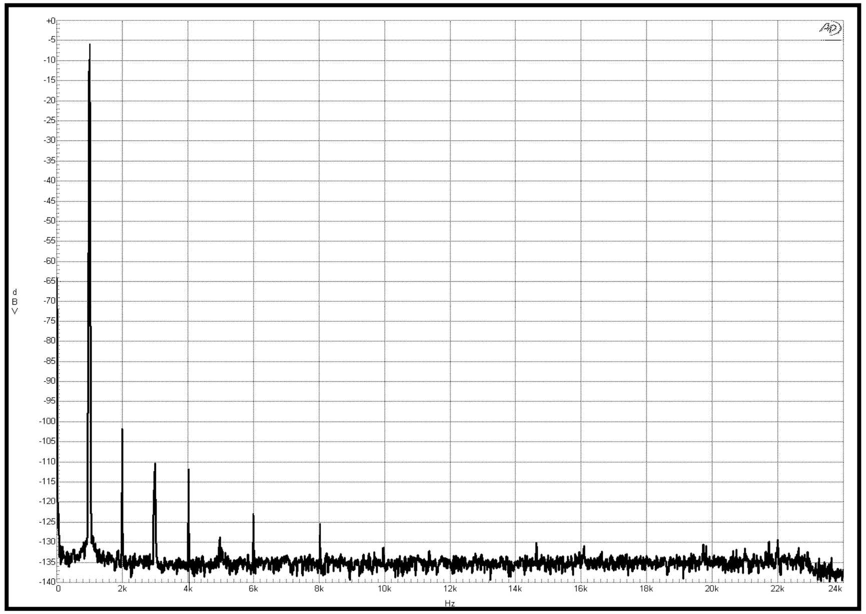
Supporting Data



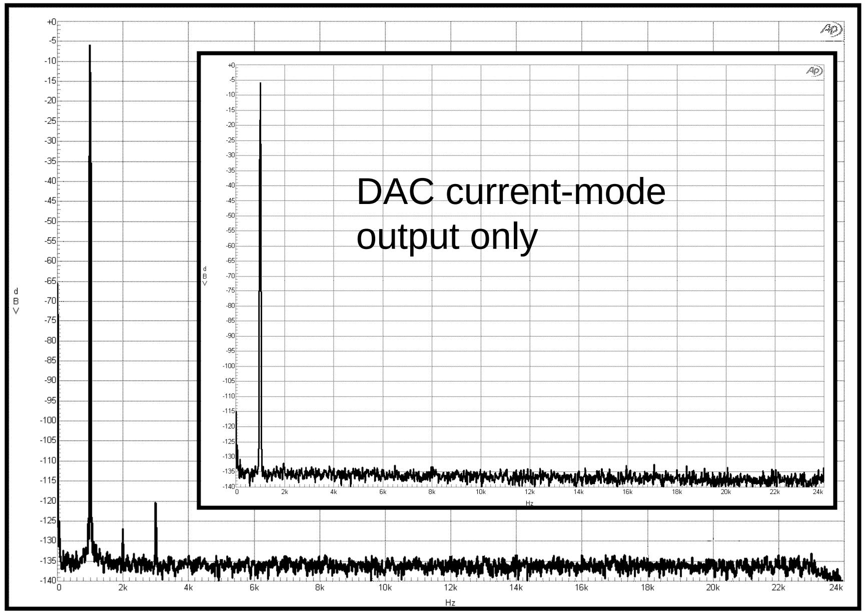
➢ An I2V converter has been designed and PGed for silicon testing. The simulation numbers for area power and performance for that is included above.

Preview: The ISI shaping algorithm

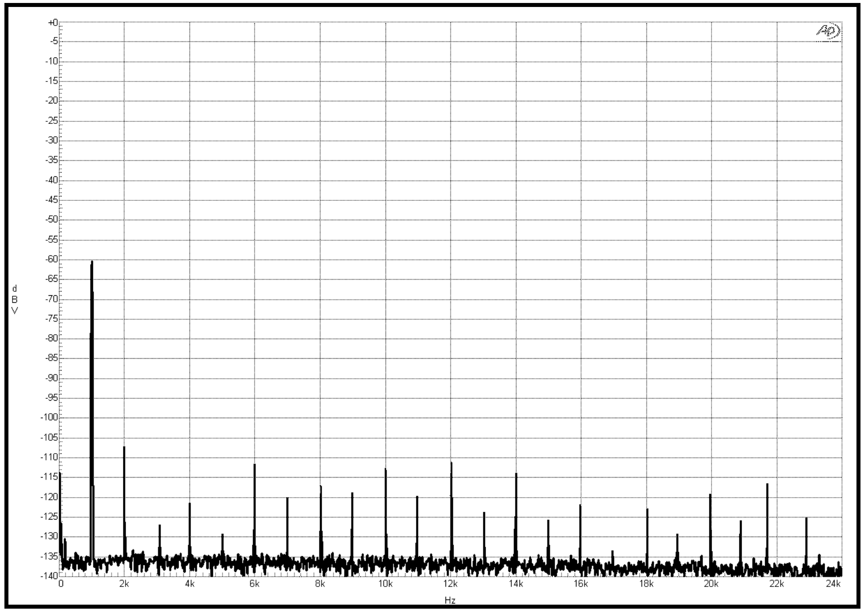
- New mismatch shaping algorithm:
  - Shapes static mismatch
  - Shapes ISI errrors
  - Runs at the SDM rate (unlike PWM)
- Silicon results on the next slides



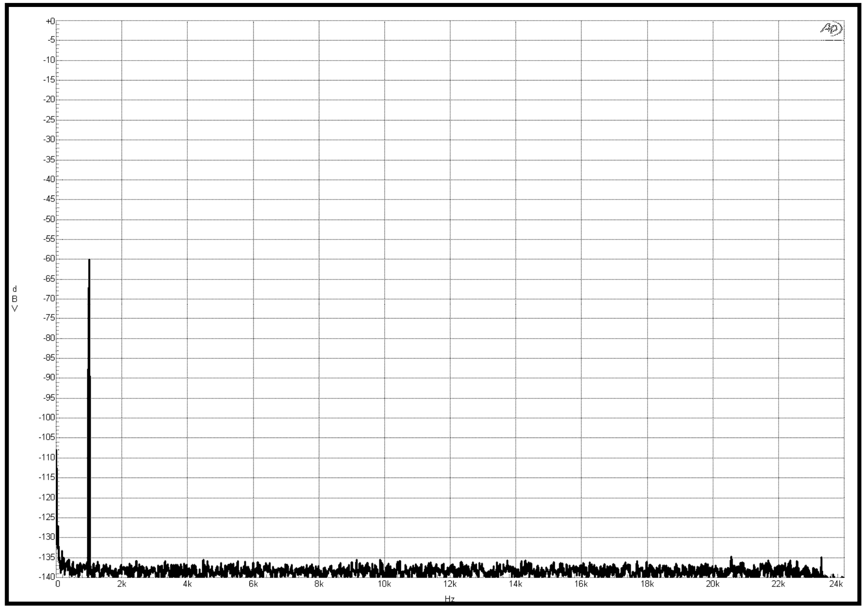
(a) Large Signal with DWA Rotation



(b) Large Signal with ISI-Shaping



(c) Small Signal with DWA Rotation



(d) Small Signal with ISI-Shaping