Cellular TX architectures for highly integrated tranceivers

Sami Vilhonen, STEricsson Finland

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Outline

- Motivation
- Specifications
- Topologies
- Things to consider

Why transmitter?

- Power consumption traditionally dominated by PA
- No killer blocks (like for example RX ADC)
- No complicated circuit design tricks needed to boost linearity or noise (like LNA)
- IQ Filtering requirements clear since nothing mysterious entering TX, unlike RX
- ---> BORING ! ! !

Why transmitter ?

- WCDMA DG09 changed thinking of current consumption
  - Lower Pout important -> tranceiver TX current consumption very important
- No SAW filters before PA
  - TX noise requirements exploded
- Gain range requirements harder than for RX, same time requirement for scaling down the current with gain
- Since we generate TX signal ourselves, we know what kind of signal it is and it gives as more freedom to play with it
- ---> BORING BECAME INTERESTING ! !

General specification

- Max Pout<10dBm (max 1V amplitude @ 50 Ohm)
  - Not too accurate spec but at least between -174 and +296dBm
- SNR > 160dBc/Hz
- Linearity (not applicable for polar TX)
  - 3rd order BB distortion better than -40dBc (single tone, HD)
  - 3rd order RF distortion better than -30dBc (two tone, IMD)
- Dynamic range ~80dB
- IQ bandwidth up to 10Meg
- Several bands with huge frequency spread
- Output matched
- LOW current consumption with all Pout values
- LOW silicon area and external component count

DAC and image filtering

- Current steering DAC's widely used
- Higher Fclk in DAC reduces filtering requirement, but increases current consumption of DAC
- High Fclk -> maybe passive RC filtering is enough
- Low Fclk means simple and efficient DAC but requires usually active filtering

- Not a bottleneck at the moment in TX
- Requires relatively small area and Icc
- It does not mean, that nobody can introduce new DAC which blows our minds...

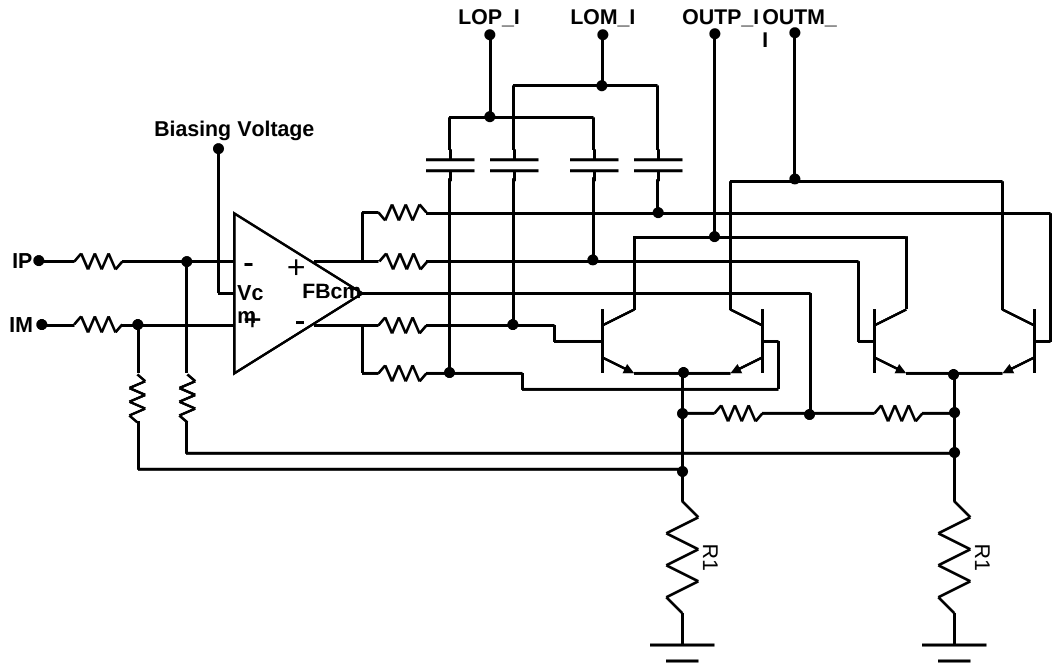
What would be the Mind_Blowing_DAC for TX?

- DAC driving directly PA
- About 14 enob for SNR
- Fclk in GHz range or lower Fclk with frequency up-conversion
- Sigma-delta converters not looking attractive, since there is no frequency band in TX where to push all the noise unlike in RX ADC
- Never seen yet, but please make one ☺

Modulator

- IQ-frequency translation to RF
- Current mode and voltage mode (i.e current output or voltage output)
- At BiCMOS time, thanks to BJT, allways current mode
- In CMOS voltage switching also possibility and very attractive

Current Mode Modulator



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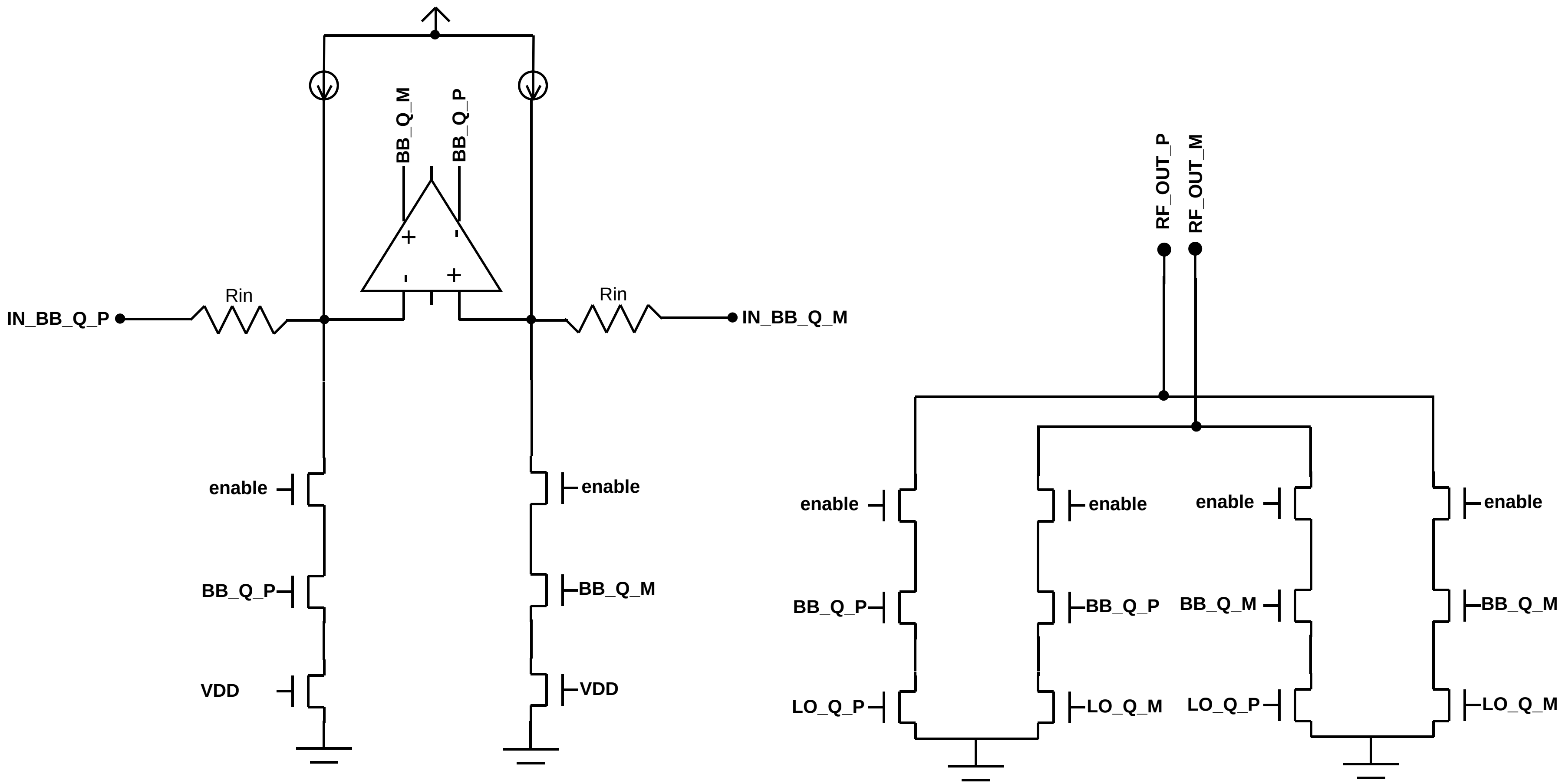
Current mode MOS example



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Current Mode Modulator

- Requires V to I conversion, which causes source of nonlinearity
- consumes DC current
- topologies usually require also several transistors on top of each other
  - Power supply limitations
- Flat response by nature
- Gain step possibility

Predistortion in current mode modulator

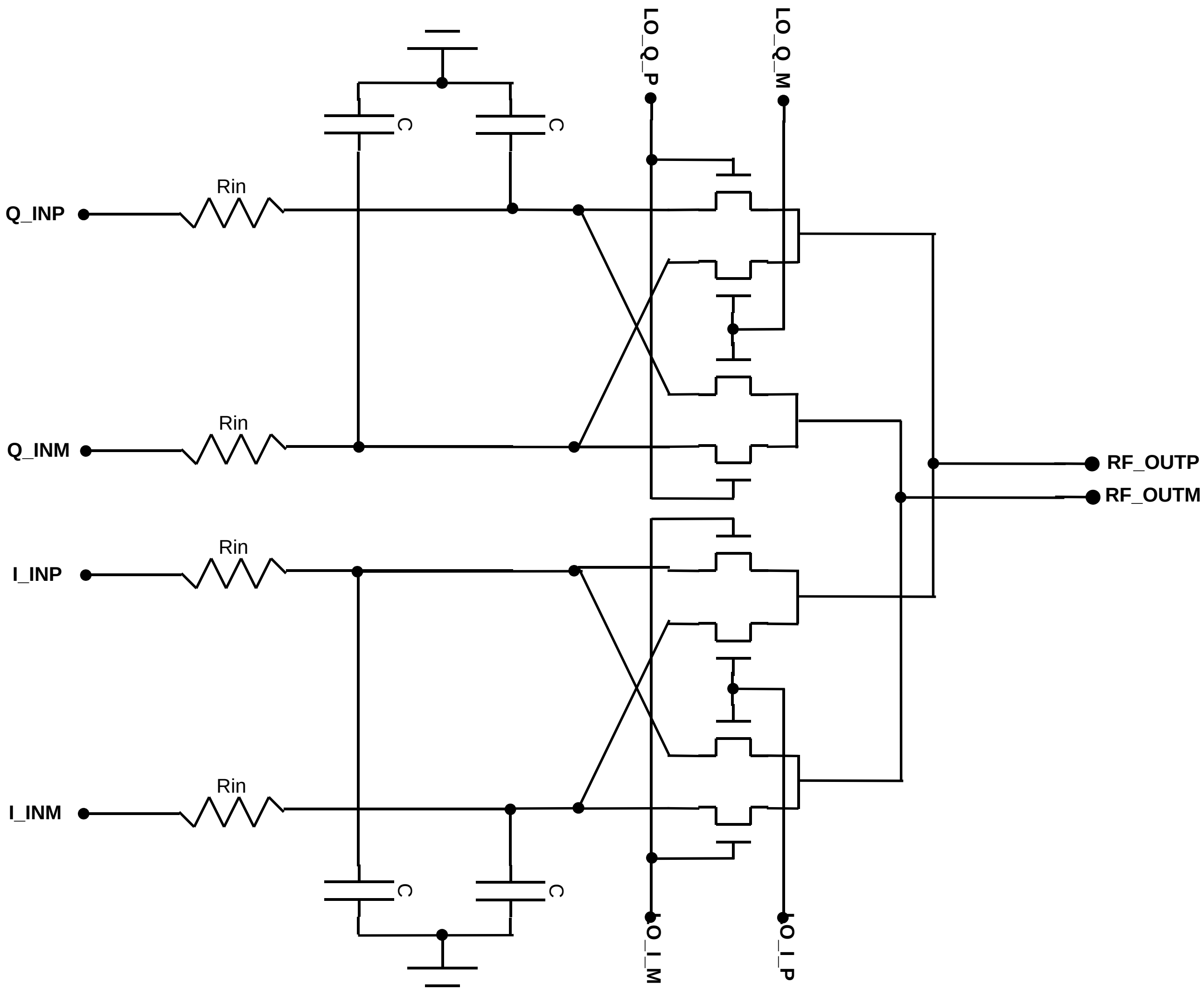
- Linearity limitation comes from BB linearity (if wanted signal is LO-IQ then linearity is at LO+3IQ)
- With 3rd order product better than -40dBc compression is in the order of 0.1dB

⇒Adequate SNR difficult to achieve with so low compression

⇒Predistortion pushes circuit into compression while maintaining linearity

- predistortion requires harmonics, so pre-modulator filtering can not influence 3rd harmonic
  - LTE 10Meg IQ means -3dB filtering frequency higher that 30Meg
- Matching in predistortion between main circuit and mirror circuit in significant role
  - Challenging to control specially if they run at different frequency

Voltage mode modulator



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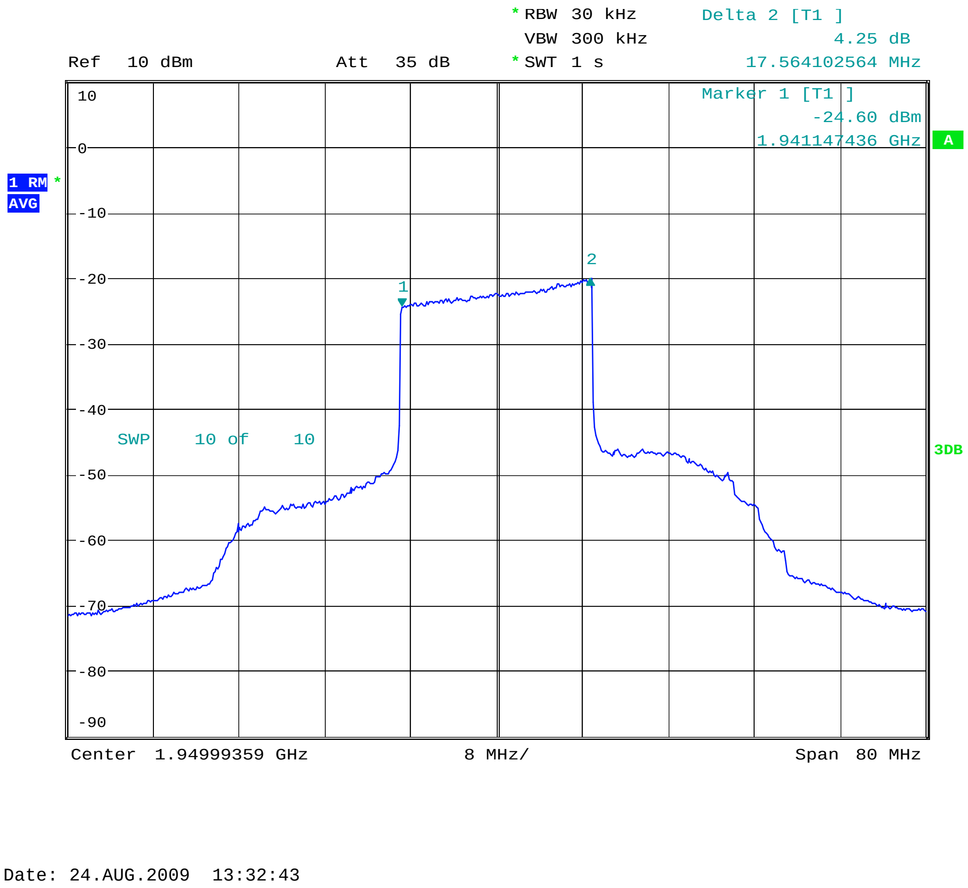
Voltage mode considerations

- No current consumption
  - Not true, since current for LO is significant
- Extremely good noise performance if Ron<<Zload
  - better noise = bigger switch= more current for LO
- Driving stage (filter for example) must be capable of driving small impedance
- Good linearity if Zon<<Zload with all input voltage values (and also that Zoff>>Zon)

Voltage mode modulator tilt

- frequency response different depending on which side of LO we are (tilt)

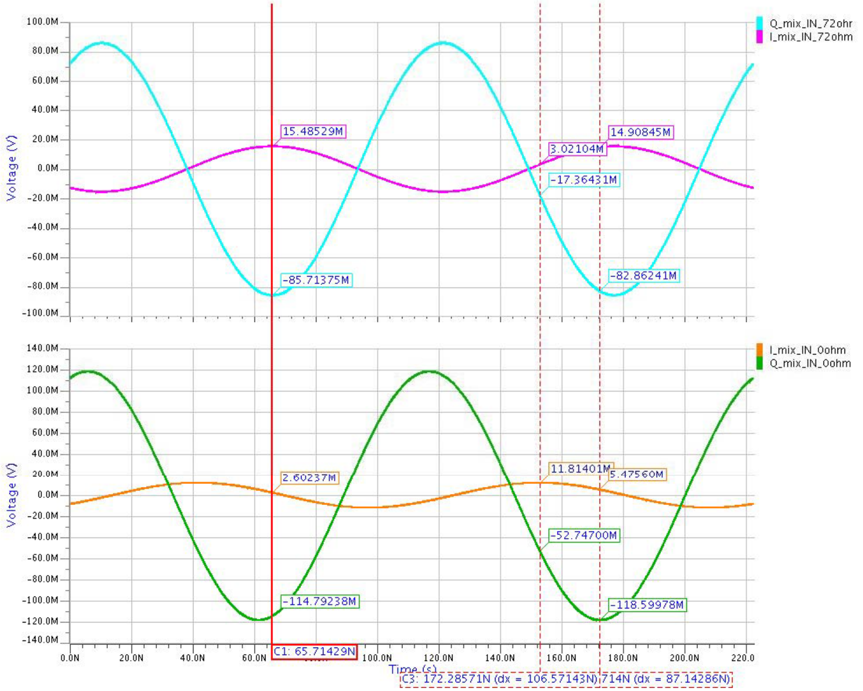


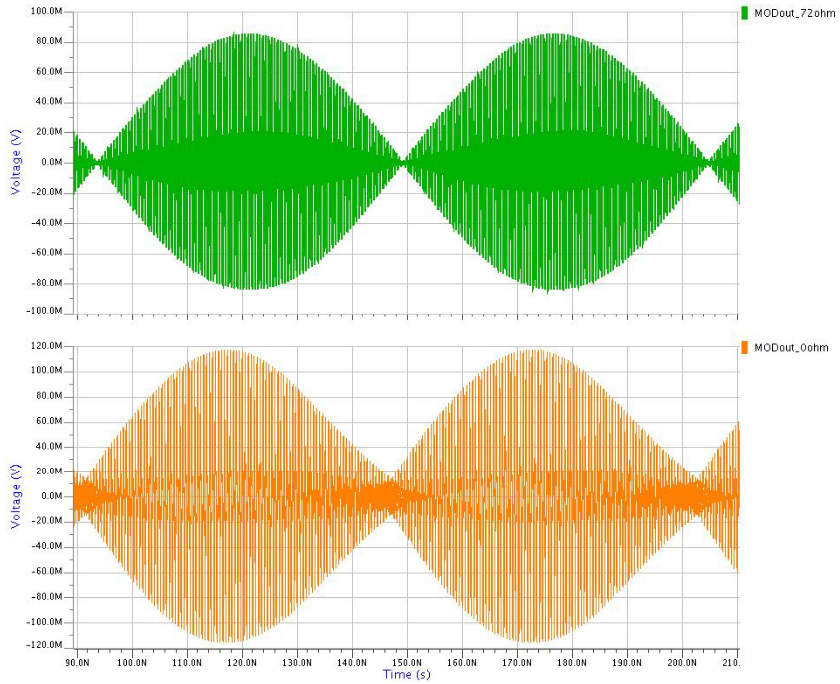
Tilt continue

- Generated because feeding impedance is not zero

  ⇒I signal will generate small voltage in Q

- Amplitude and phase of 'leaked' I-signal in Q depends on magnitude and phase of Q impedance





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Tilt solutions

- Infinite bandwidth for feeding stage
  - Or at least try to push bandwidth as high as the noise allows
- pure resistive feeding impedance
  - Or at least more resistive, for example adding series resistance
- pure resistive in the next stage
  - inductor at the output helps, but nobody likes them
- current mode input in next stage
  - remove 'memory' from output
- Predistorting I and Q
  - digital predistortion filter to shape I and Q accordingly
  - might need different settings depending on band, temp etc. if tilt is too big for starters

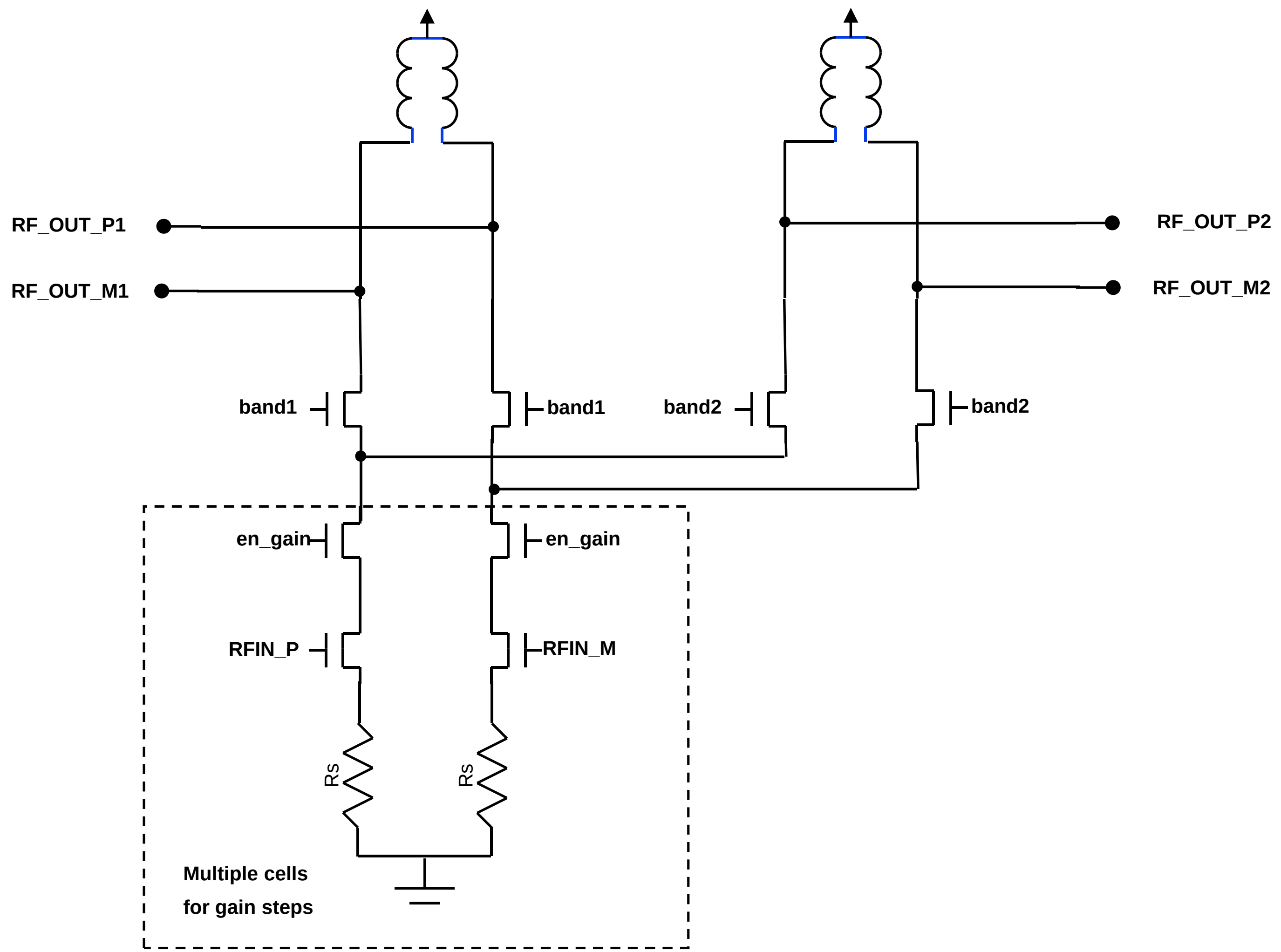
Gain steps in Modulator

- voltage mode modulators gainsteps only from attennuator in input or output
  - input attennuation degrades LO and unwanted supression
  - Output attenuator increases output capacitance, which increases previous stage current consumption
- Current mode modulators gainsteps easier
  - Several unit cells for example
  - increases however the complexity and therefore loading for LO-buffers
  - matching of V to I conversion between unit cells controlling LO and Unwanted supression

⇒Not possible to obtain as much dynamic range as from typical amplifier

⇒Still assuring performance over temperature and process variations during lifetime might influence your good night sleep...

Pre Power Amlifier, PPA



Pre Power Amplifier, PPA

- Increase dynamic range
- capable of delivering power
- matched output
- Small gain or otherwise requirements for modulator become unrealistic
  - +6dBm Pout, -162dBc/Hz => noise level -155dBm/Hz at output. 18dB PPA gain means -174dBm/Hz at the input...
- Some gain needed anyway because of low Vdd
  - +6dBm @ 50 Ohm = 630mV amplitude => 0dB gain means 630mV amplitude also in input...
  - Usually voltage gain is in the range of 2-6dB
- 3rd order linearity spec from RF linearity (two-tone)
  - can be usually compressed more than modulator
  - noise contribution from PPA usually less than -165dBc/Hz

PPA challenges

- max dynamic range in the range of 40-50dB
  - parasitic coupling makes gain step accuracy difficult with lowest gain values
  - gain step variation should still be in the range of 0.1dB PVTL (L=lifetime)
  - more gain steps = more complicated design = more parasitics = less isolation
  - Icc must go down with output power
- switchable loads for several bands
  - baluns used widely to get single ended output
  - parasitic capacitance increased with several outputs, but same time wider bandwidth is required...

3LO+IQ

- If wanted signal is at LO-IQ, then modulator generates also by nature 3LO+IQ at level about -10dBc
- If fed to 3rd order nonlinearity block with wanted signal, it will generate spurious at

$$f1-2 \times f2= 3LO+IQ-2x(LO-IQ)=LO+3IQ$$

which is BB linearity tone

- supression needed at least before PA
  - LC resonators are pretty much the only ones to help in this
  - levels of -30dBc at the output of the tranceiver are somewhat tolerable

2nd harmonic

- Wanted signal LO-IQ will generate in differential structure (like PPA) common mode signal at 2LO-2IQ
- If Fvco=2*LO then 2LO-2IQ is very close to VCO frequency
  - it will couple very easily to VCO core
  - maximum coupling usually with IQ frequency of PLL loop bandwidth
- Signal coming from VCO to divide-by-2 includes therefore spurious at ±2IQ
  - Divider output will also have spurious at LO±2IQ
- IQ-modulator will add offset of IQ for all of those and the interesting tone will be at LO-3IQ (other results are on top of other tones and therefore difficult to see, Wanted, Unwanted, BBDist)
  - if LO-3IQ level does not change by changing amplitude of TX, there is no VCO coupling from PPA

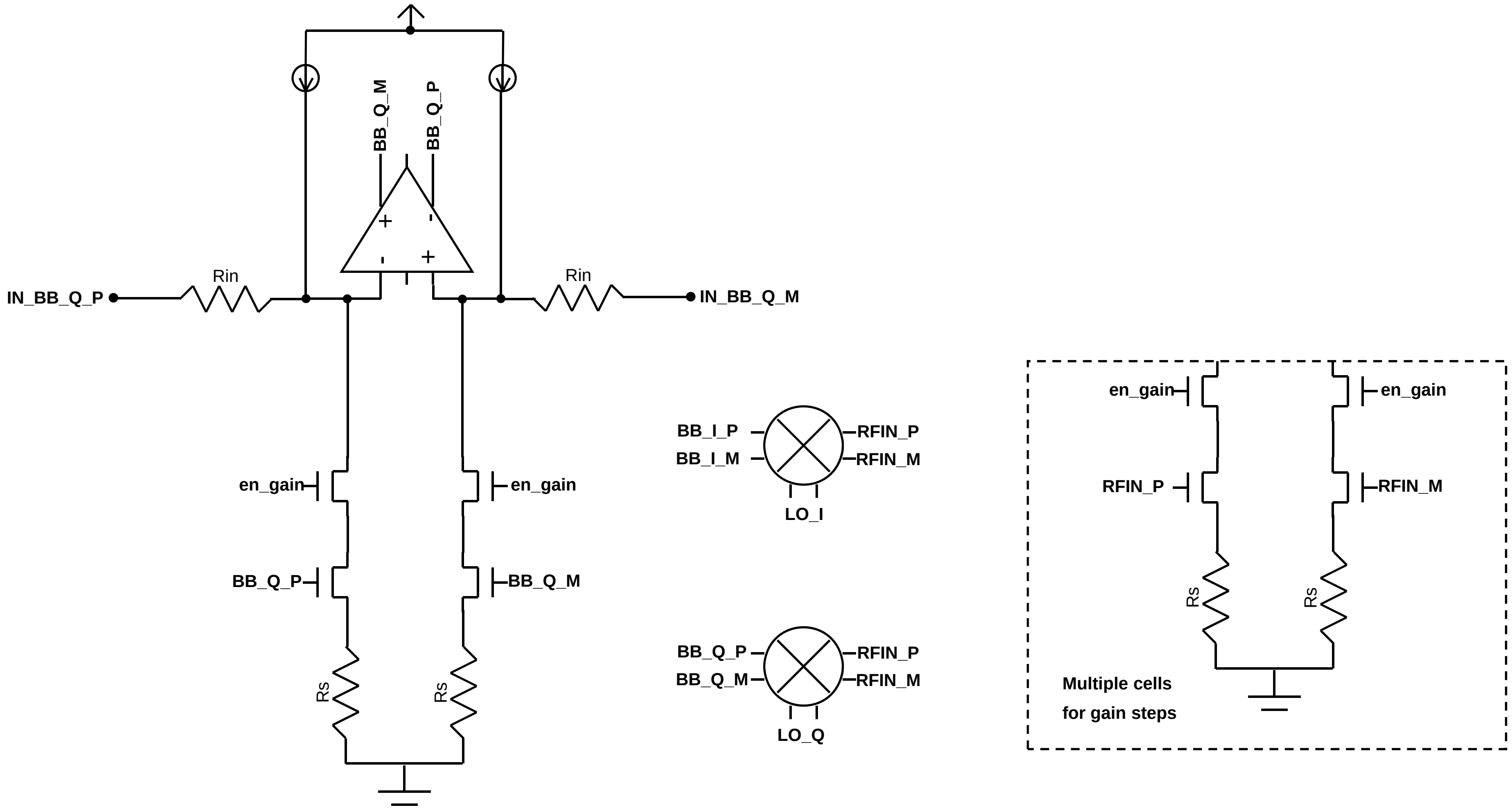
2nd harmonic continue

- Reducing 2nd harmonic is possible
  - higher common mode impedance at ground
  - Lower common mode impedance at VDD
  - Good AC connection between VDD and ground (= capacitor)
  - Shielding
  - 8-shape coils
  - Luck
  - correct duty-cycle of dividers
- Only visible with measurements of total tranceiver and therefore very difficult to model

Predistortion with Voltage mode modulator

- Predistortion does not help switches and there is no distorting V to I transformation either
- Predistortion can however be used to linearise next amplifying stage like PPA
- Same basic idea as with current mode modulator but now the mirror circuit is in BB frequency, main circuit at RF and connected via voltage mode modulator to eachother
- Voltage mode modulator predistortion is actually PPA predistortion

Predistortion with Voltage mode modulator



PPA predistortion considerations

- Improves performance for the most current consuming block
- improves PPA noise contribution (which is not much but anyway)

- Again, needs harmonics to work so you can not filter noise with narrow RC filtering
- Possible tilt in modulator tilts also harmonics => linearity improved differently depending on which side of LO we are
- BB frequency performance must match with RF performance in main and mirror circuits
- 3LO+IQ can be filtered only with PPA output impedance
- Gain range not enough with PPA alone => needs some other path for low powers

Additional blocking points for TX

- Production testing times MUST BE in the range of few seconds
  - Must avoid communication between measurement device and phone
  - Selftesting !
  - Gain steps to be quaranteed by design
  - Temperature variations to be quaranteed by design
  - Tight screening of chips in IC fab
- PA input impedance is not 50 Ohms in real life
  - still not OK to clipp the signal at the output of tranceiver even if ZinPA=150 Ohm
- WCDMA call is continuos => do not change things during it
- PA predistortion also under development => predistorted predistortion has allready huge bandwidth... ☺

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Conclusion

- Several possibilities exists to boost TX performance
- None of them seems to be perfect for everything
- Clever looking method is only clever, if it does work well in production

- Looks like TX is still waiting for it's goldrush...