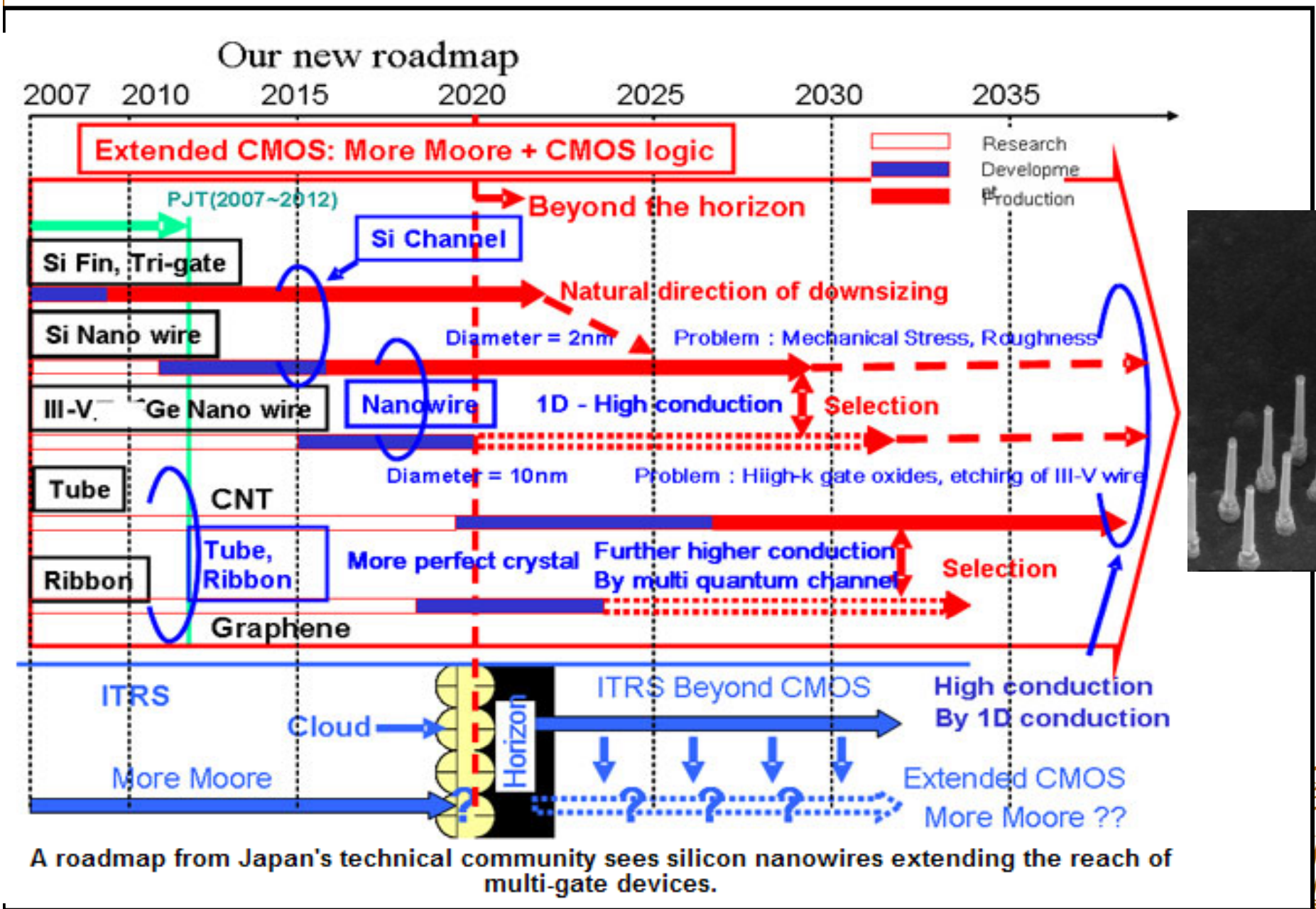
TFETs for Reduced Power Consumption

Lars-Erik Wernersson

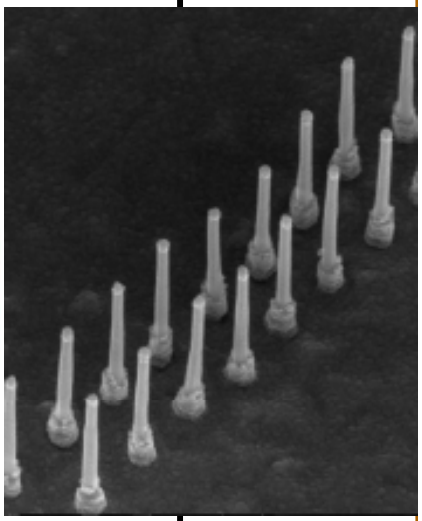
Electrical- and Information Technologies/
Solid State Physics Lund University, Sweden

- MOSFET fundamental limit of 60 mV/dec.
- TFETs device implementation
- Noise performance

Lund Circuit Design Workshop, Lund, Sweden

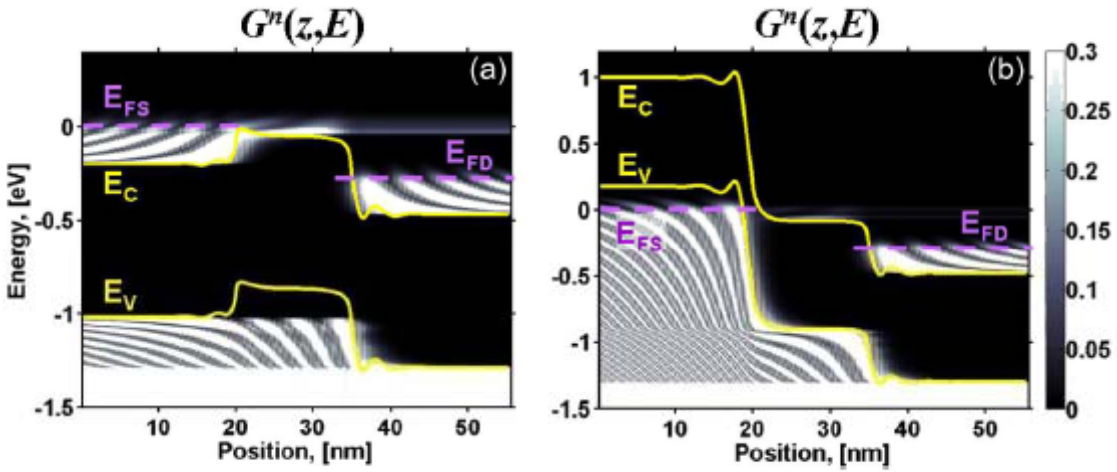


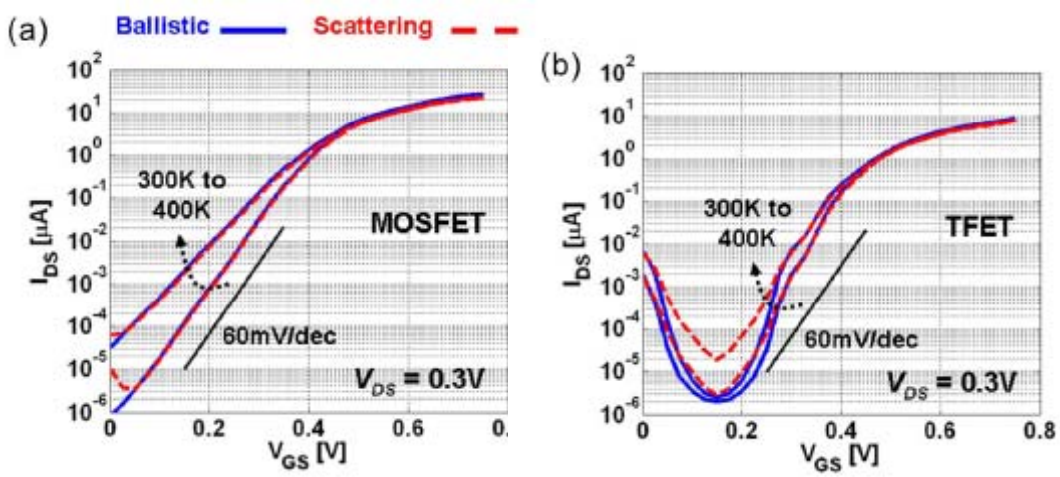
A roadmap from Japan's technical community sees silicon nanowires extending the reach of multi-gate devices.



How to overcome the 60 mV/dec. limit?

MOSFET **TFET**





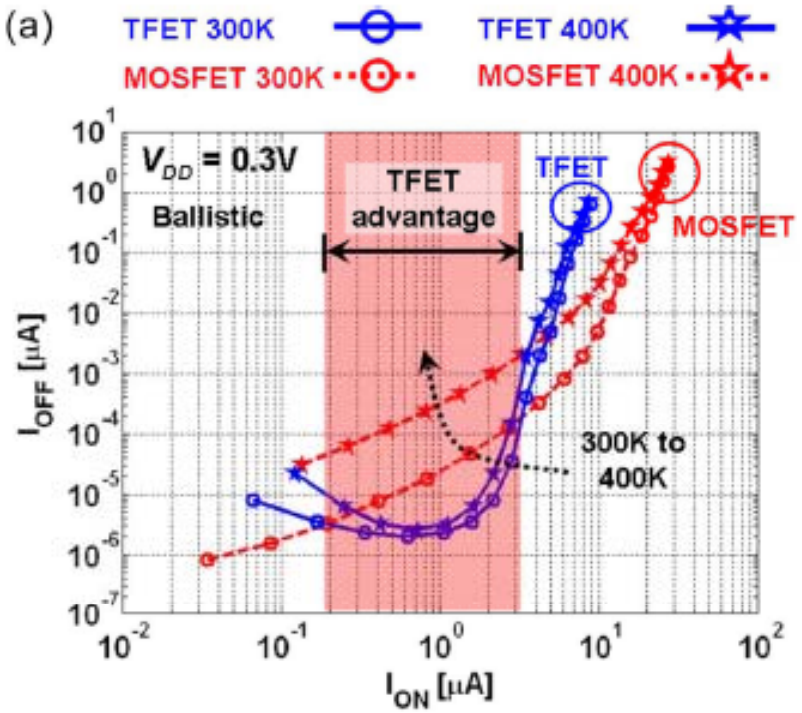
Introduce a bandpass filter!

A gated pn-junction!

Allows a reduction in drive voltage!

Koswata et al TED 56, 456 (2009)

The advantage is at moderate drive currents

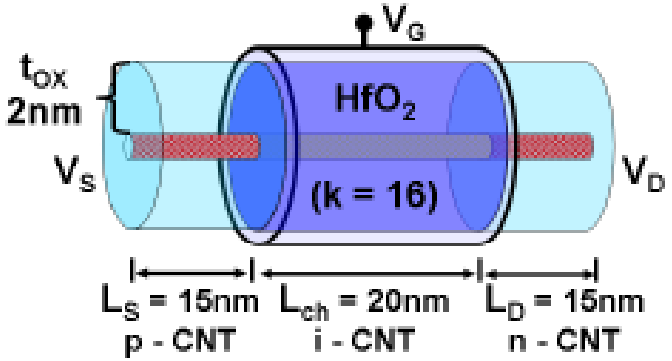


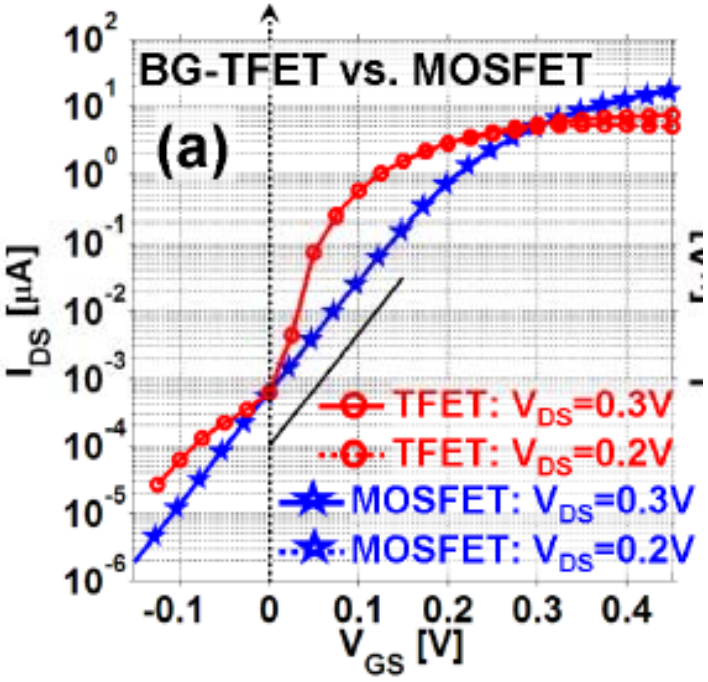
The pn-junction blocks the current and hence a lower I_{on} is achieved

Still advantages for moderate drive currents

Koswata et al TED 56, 456 (2009)

Heterostructure design





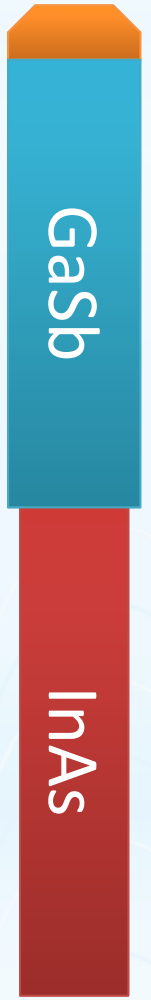
Use a NW to achieve good electrostatic control

Adjust the band gap to increase the tunnel probability and hence the drive current

Koswata et al IEDM 2009

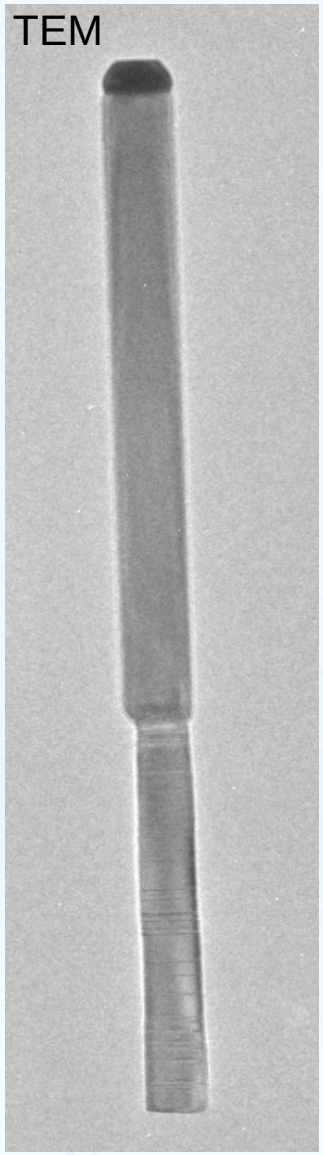
Method

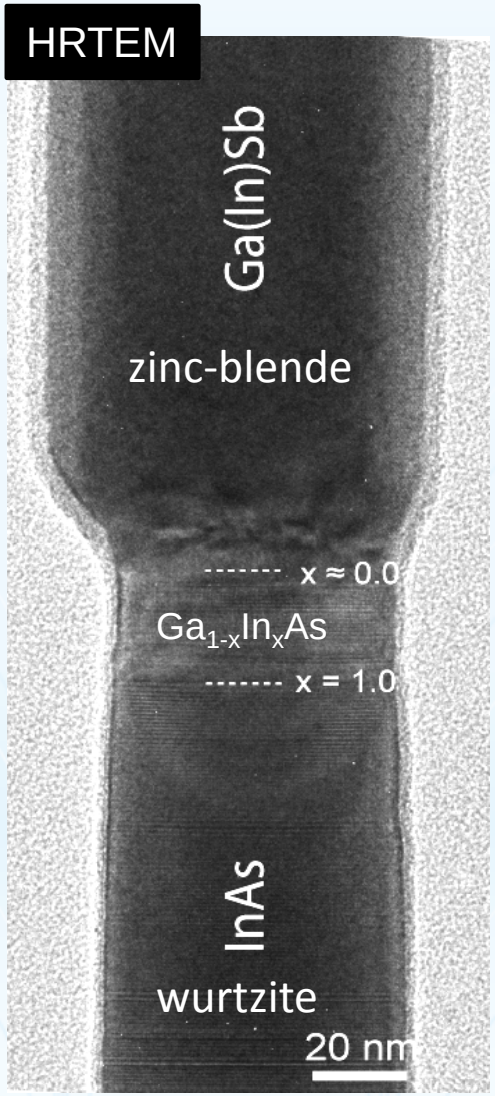
- MOVPE – AIX200/4, 3x2” or 4” wafer
- 40 nm Au aerosols on InAs(111)B substrates
- GaSb nanowire growth previously calibrated*
  - [TMGa] = $9 \cdot 10^{-6} \rightarrow 5 \cdot 10^{-5}$, V/III = 1 → 3
  - 550°C pregrowth annealing
  - 450°C for InAs, 470°C for GaSb
  - 13 l/min H_2 during cool-down

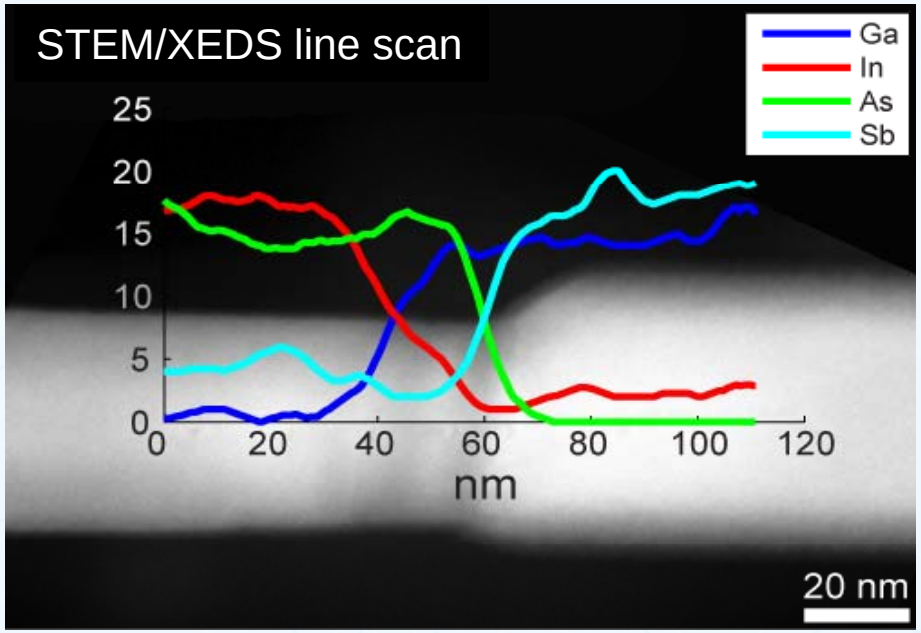


*Jeppsson *et al.* J. Cryst. Growth, 2008

Optimized structure



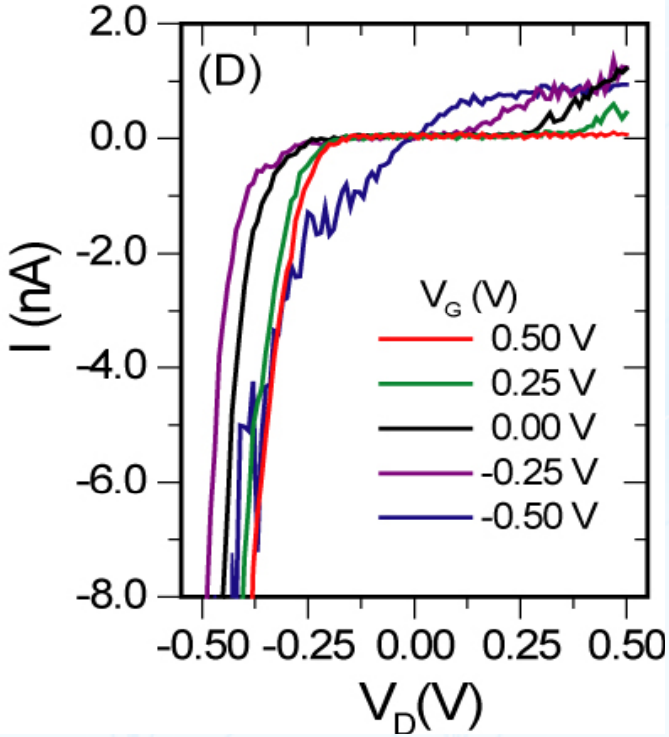


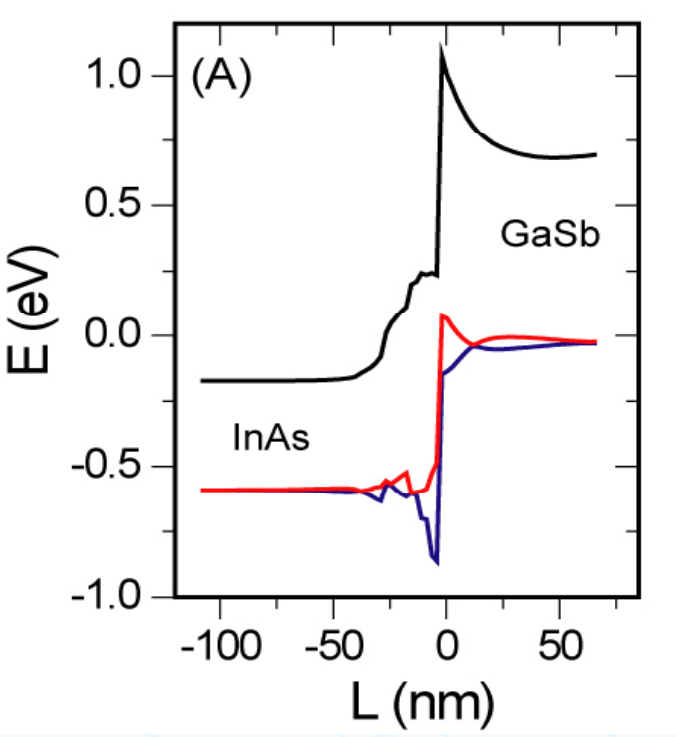


- 25 nm graded GaInAs barrier
- 5-10% Indium in GaSb
- 1-2nm InSb shell on InAs
  →Sb-As exchange

Transistor devices

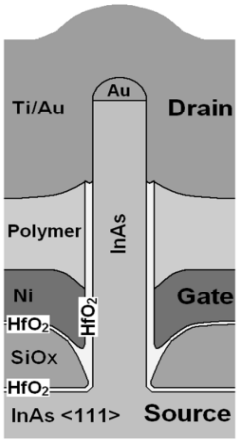
- Indications of band-to-band tunneling
  - Negative V_g opens up transport window at low bias
  - Strong gate dependence in forward bias
- Current saturation imply: impurity mediated transport

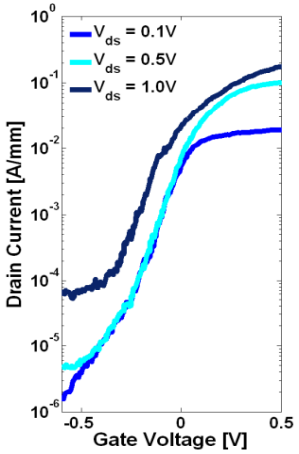


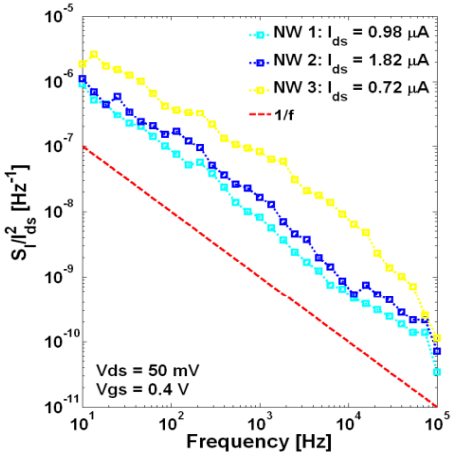


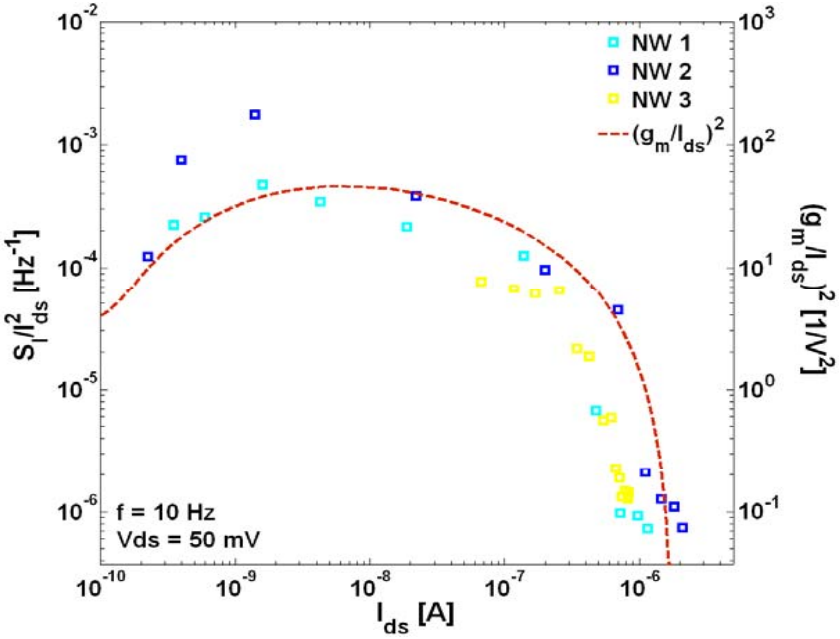
Low-Frequency Noise Measurements

Cross-section **DC-characteristics** **1/f-noise**









Average SS: **130 mV/decade**
Norm. I_{ds}: **0.16 S/mm**
V_T: **-0.1 to 0.0 V**

$$\frac{S_I}{{I_{DS}}^2} = \left(\frac{q^2 kT\lambda N}{f^\gamma WLC_{ox}{}^2}\right)\frac{{g_m}^2}{{I_{DS}}^2}$$

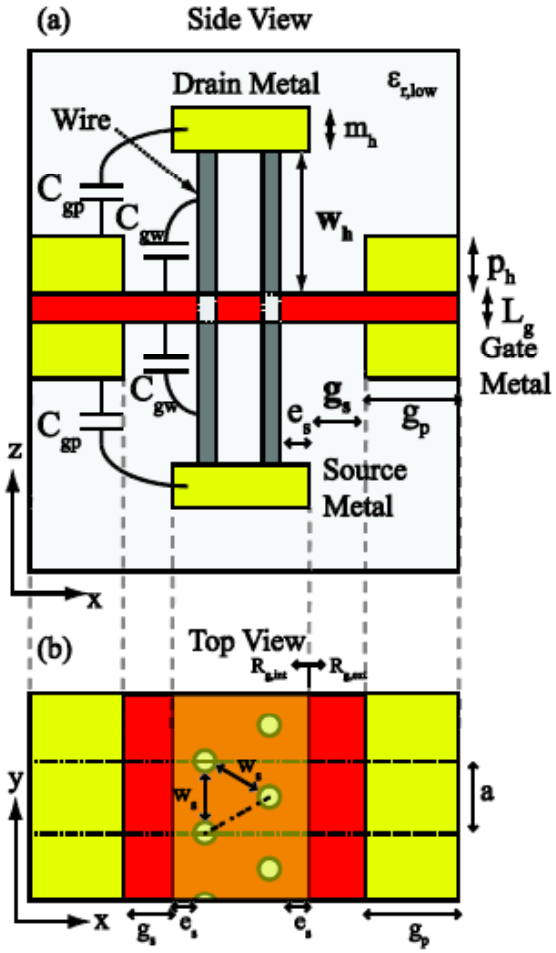
Hooge's Parameter: **4.2×10^{-3}**

Normalized 1/*f* Noise Figure: **7.3×10^{-7} Hz^{-1}**

Indication of number fluctuations.
Traps are equally distributed in energy.
Noise figure is comparable with other studies on NW FETs
The Hooge's parameter has a relatively low value.

Persson et al IEEE EDL, 31, 428 (2010)

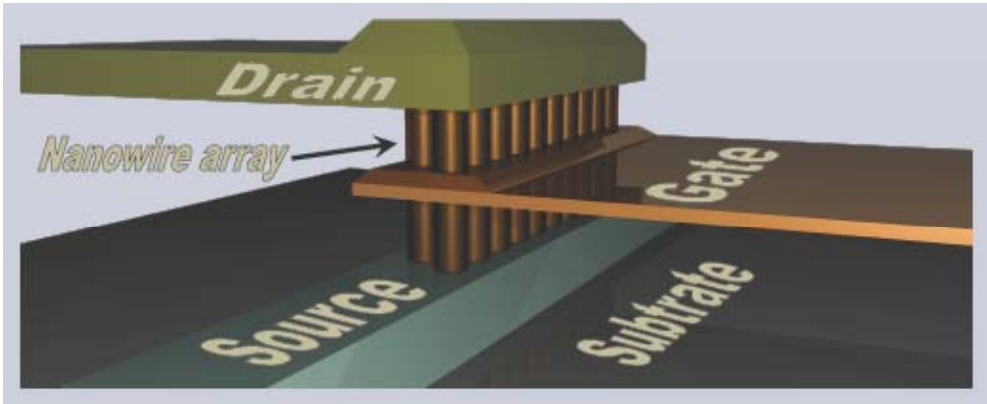
How to Reduce the Capacitances



Intrinsic gate capacitance may be low due to quantum capacitance

Gate capacitance is reduced by screening of field in row geometry

External parasitics need to be considered



Lind et al IEEE TNano 2010

The Team

Epitaxial Growth
Mattias Borg
Sepideh Gorji

Device Physics
Claes Thelander
Bahram Ganjipour

Applications
Erik Lind
Henrik Sjöland
Peter Nilsson
Piero Andreani
Anil Dey
Karl-Magnus Persson
Sophia Johansson
Martin Berg
Kristofer Johansson

Thanks SSF, VINNOVA, and VR for financial support!