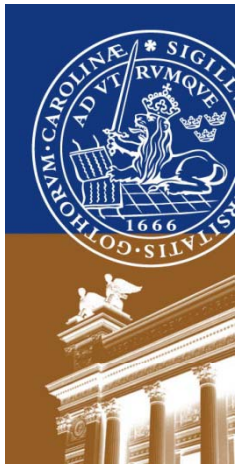
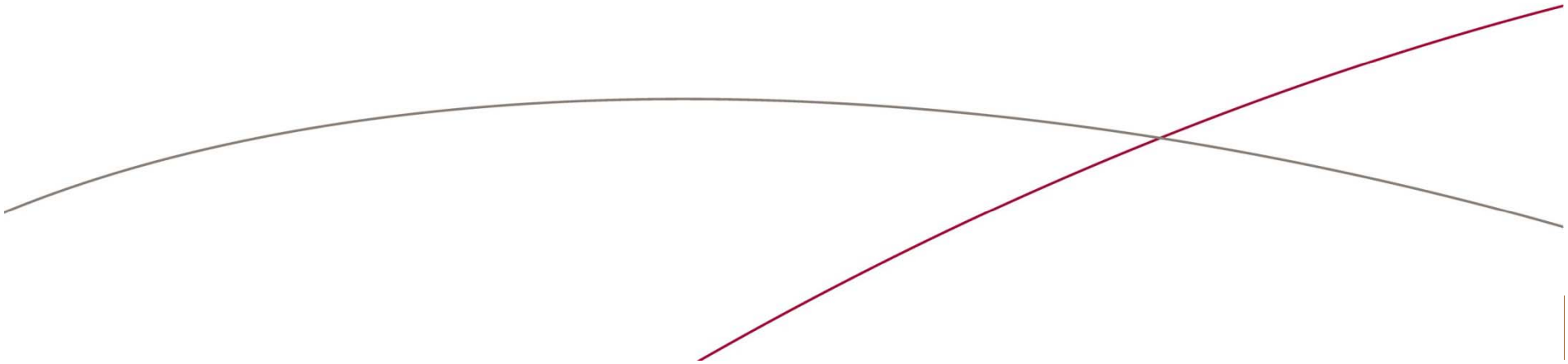


2010/11 – Advances in RF and mixed-signal cellular IC design

Mattias Andersson, Jonas Lindstrand, Martin Liliebladh, Ping Lu, Daniele Mastantuono, Luca Fanori, Martin Anderson, Lars Sundström, Pietro Andreani

Department for Electrical and Information Technology
Lund University



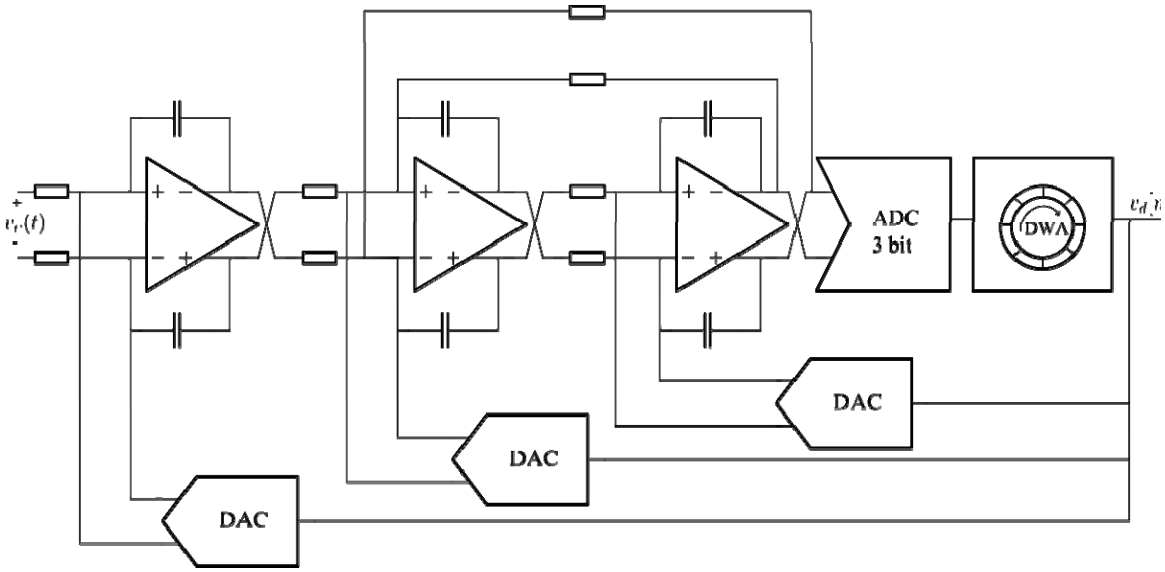
Overview

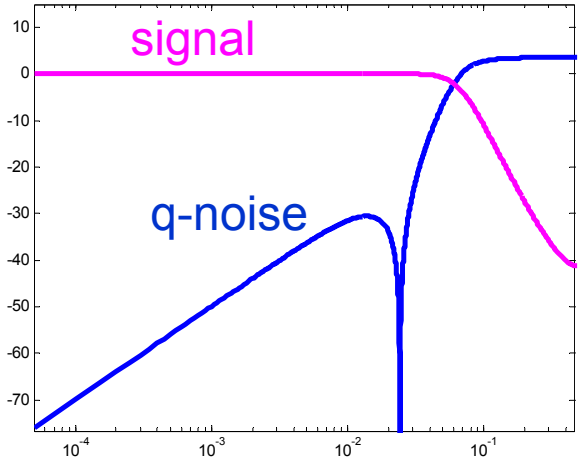
- An beautiful continuous-time ΔΣ A/D converter
  - Mattias Andersson
- An impressive 30dBm power amplifier
  - Jonas Lindstrand
- An amazing time-to-digital converter
  - Ping Lu

Continuous-Time ΔΣ ADC for LTE

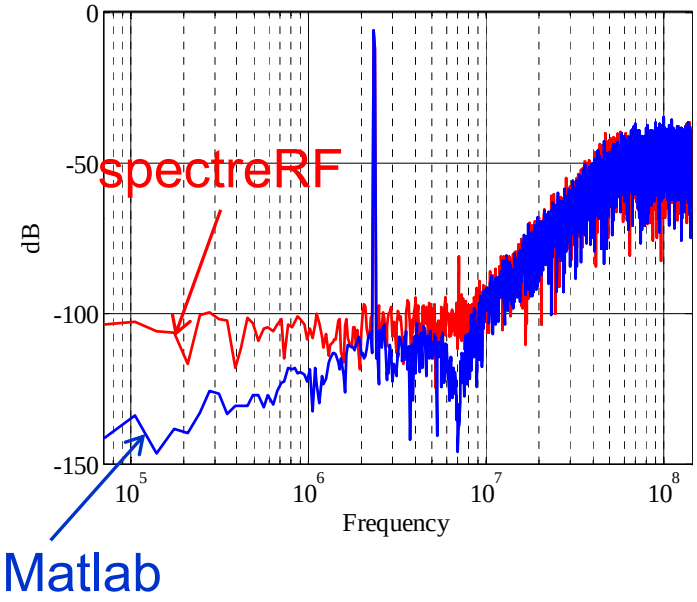
- 3rd order, 3-bit, f_s=288MHz, BW=9MHz (OSR=16)

Mattias Andersson

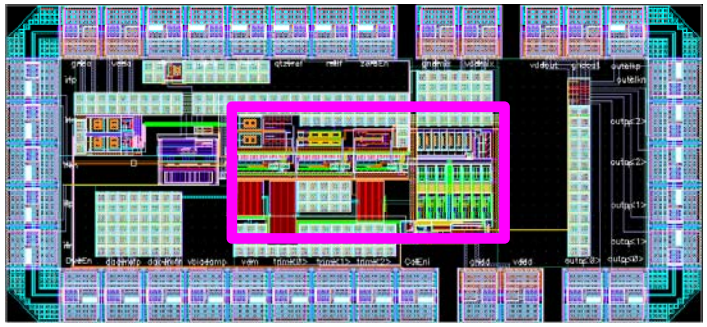




Simulation results



65nm CMOS

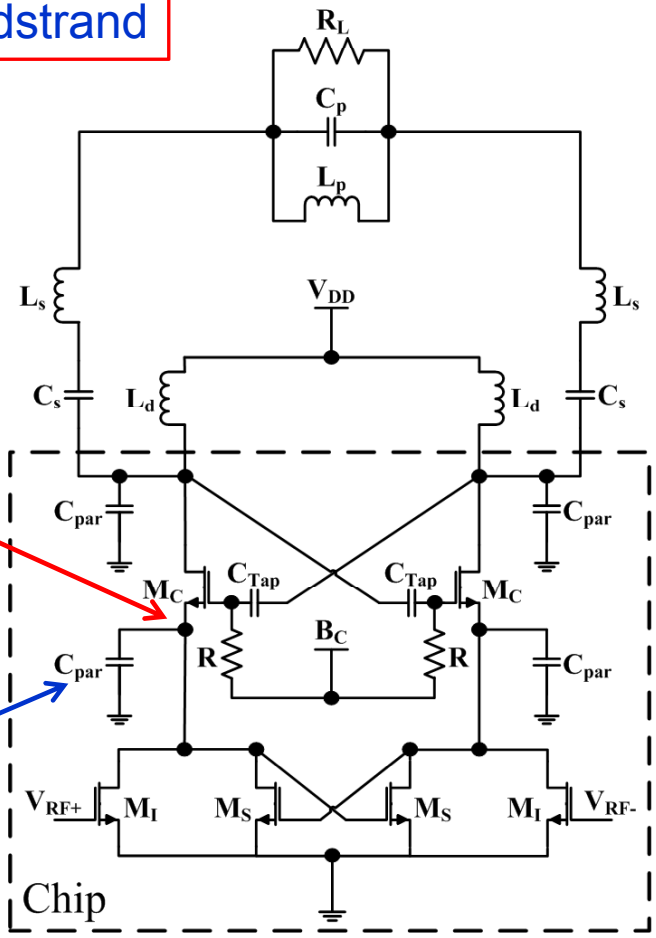


Very good predictions
with spectreRF +
transient noise

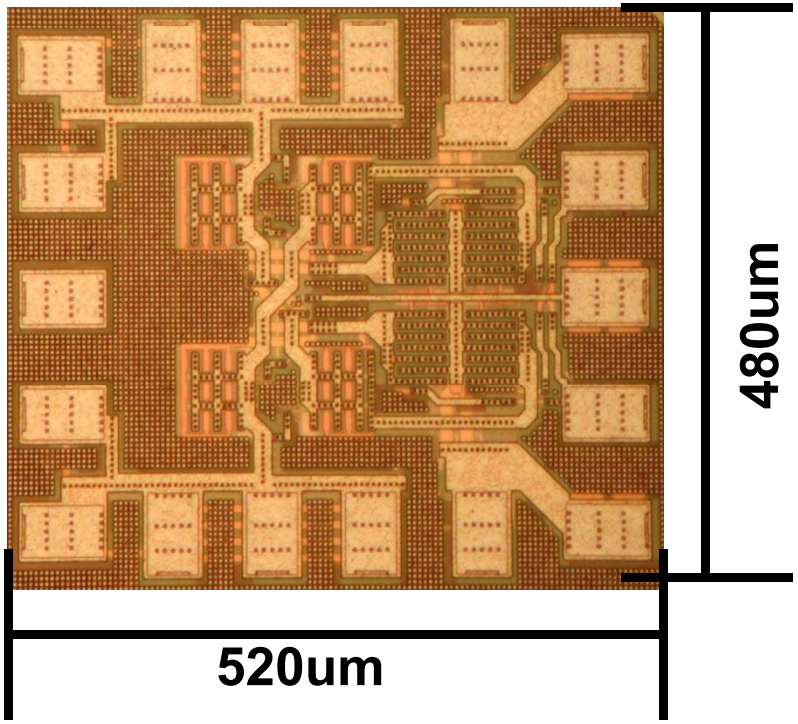
Power Amplifier in 65nm CMOS

Jonas Lindstrand

- Self-oscillating PA
  - Supply (V_{dd}) modulation
  - Reduced switching losses
- Wideband injection lock
  - Resistive injection node
  - M_S amplifies injected current
- Tapped cascode
  - C_{Tap} + $C_{par,Mc}$
  - Reduced stress on M_I/M_S
  - Reduced "SC" loss on C_{par}



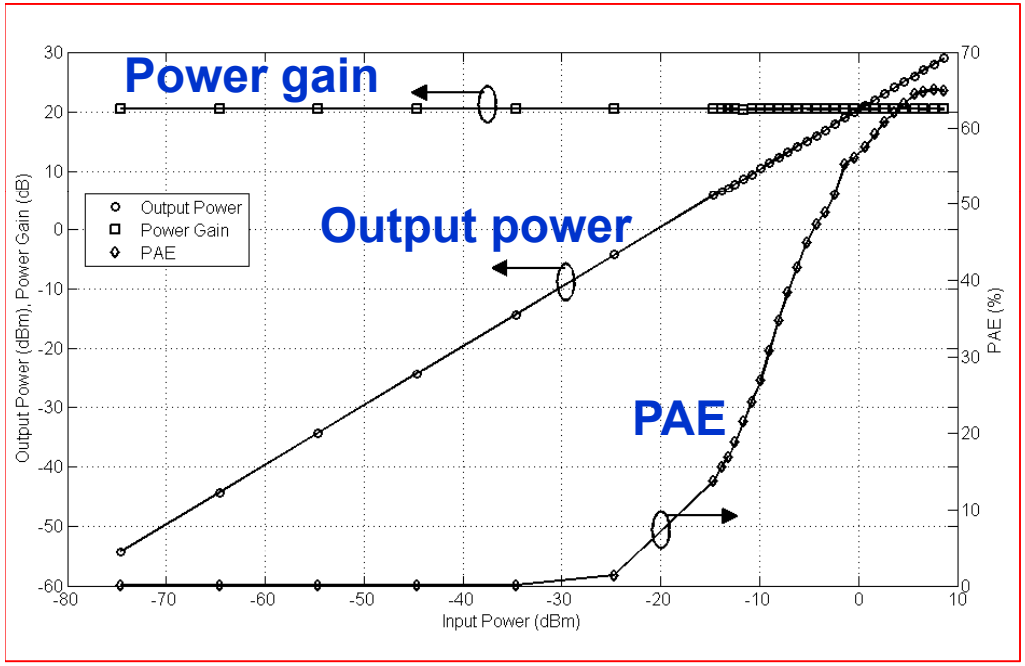
Chip photograph

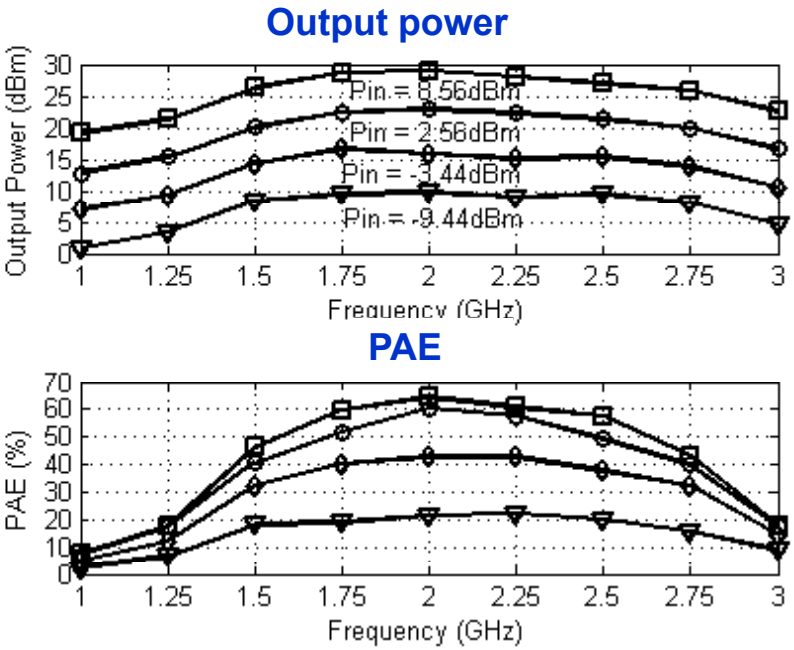


Presented at ESSCIRC 2011

Highest ranked paper in the RF sub-committee!

Measurement results





STATE OF THE ART!

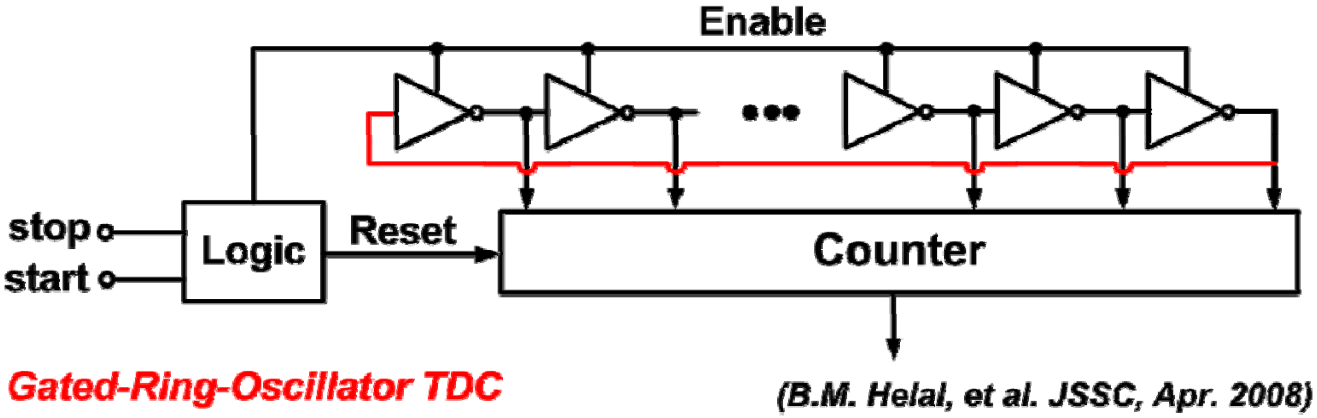
Time-to-digital converter (TDC)

Ping Lu

- Smaller TDC-cell delay (Δt_{delay}) → lower in-band PLL noise

- **Vernier TDC → τ_1-τ_2 = Δt_{delay} < τ_1 (τ_2)**
  - **However, a very large number of stages are required**

- **Ring-Oscillator (RO) TDC → large detection range with few stages**
  - ✓ **Gated-RO TDC → quantization noise pushed to high frequencies**



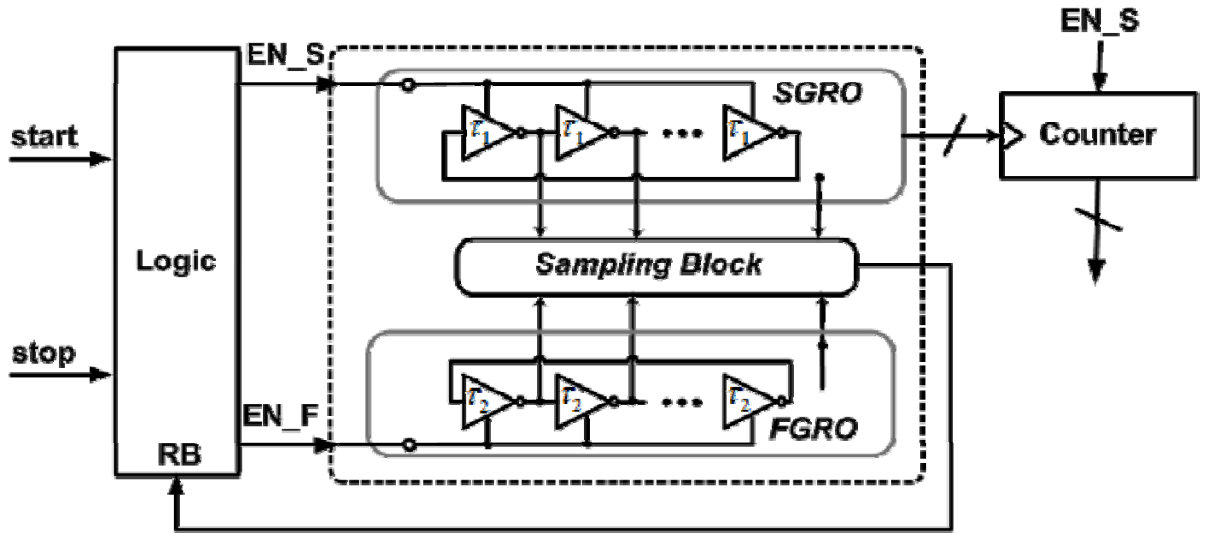
Gated-Ring-Oscillator TDC

(B.M. Helal, et al. JSSC, Apr. 2008)

However, coarse resolution still limited by an inverter delay

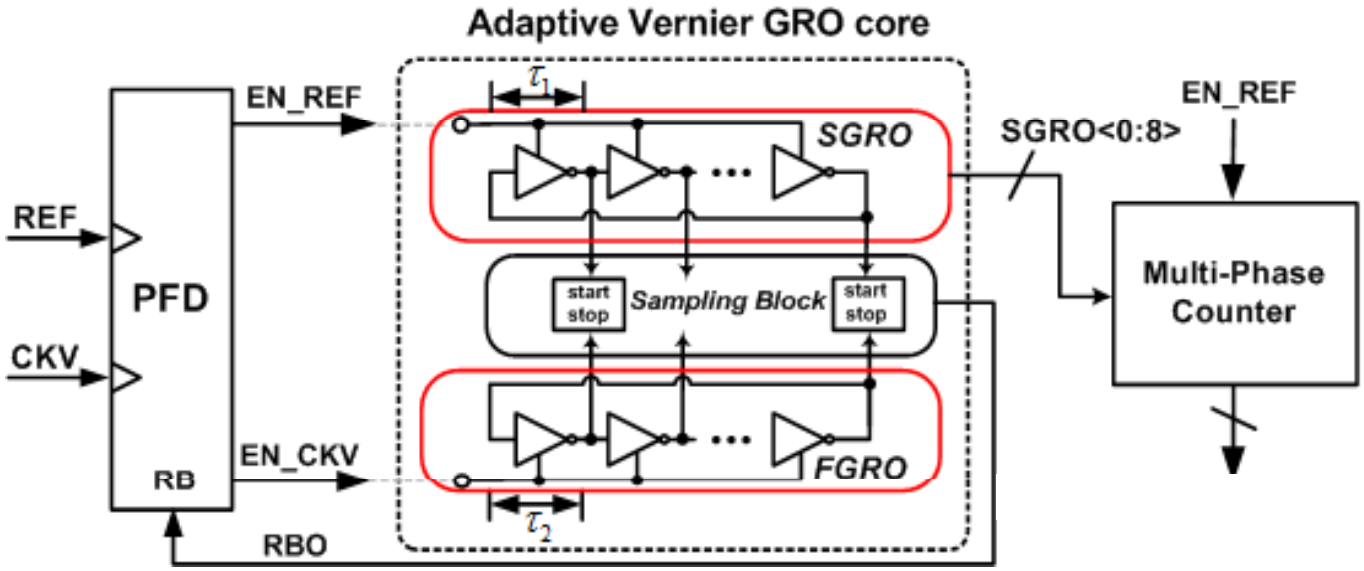
Vernier + gated ring oscillator

- **New TDC → combines Vernier + GRO**

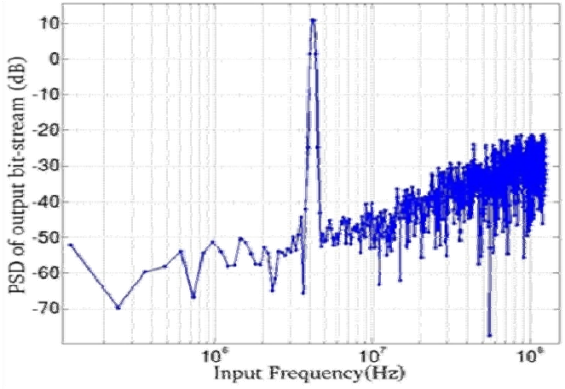


High Vernier time resolution + First-order noise shaping

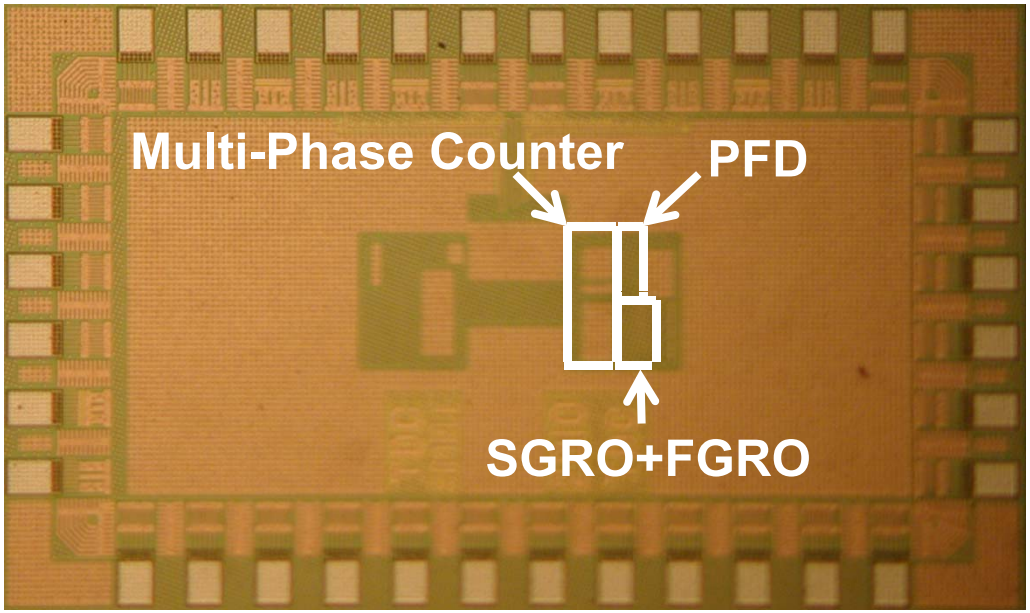
Noise shaping



1st-order noise shaping



Chip photograph

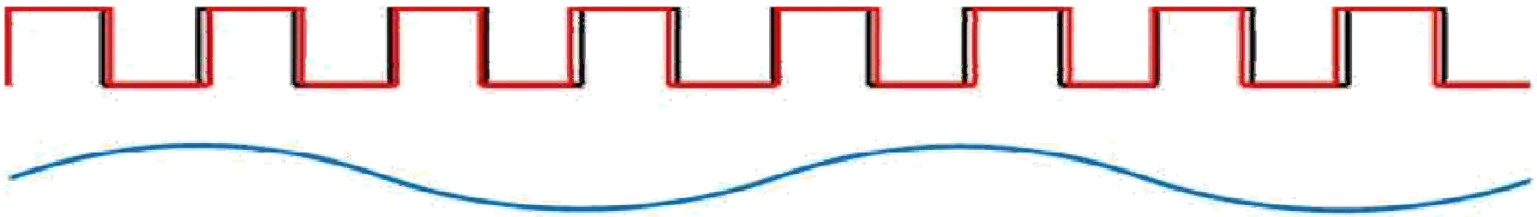


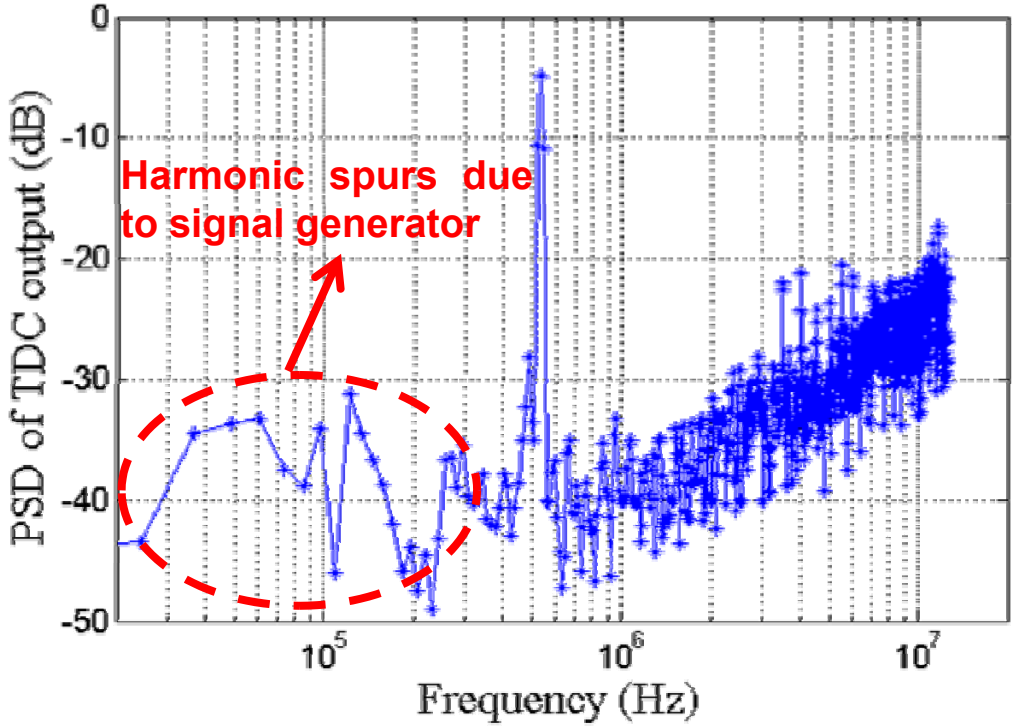
Presented at ESSCIRC 2011

3rd highest ranked paper in the RF sub-committee! (only 0.03 from top!)

Area	**0.027mm^2**
Process	**90nm CMOS**
Current (Supply)	**3mA (1.2V)**
Vernier resolution	**~5ps**
Effective in-band resolution (OSR= 16)	**~3ps**

Measurement results – sinusoidal input





TDC output PSD with sinusoidal delay input (500KHz)

SCANDINAVIAN EXCELLENCE DEFINED IN LUND

LUND UNIVERSITY