



LUND
UNIVERSITY



Welcome to the



Lund Circuit Design Workshop
2011



Welcome and Introduction

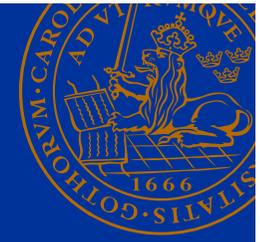
Viktor Öwall

Dept. of Electrical and Information Technology

Lund University, Sweden

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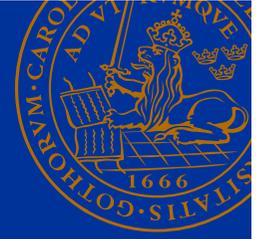
Welcome to two exiting days



- A Lund University perspective by senior researchers and PhD students



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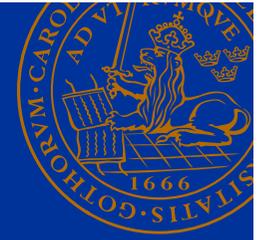


Invited speakers from academia:

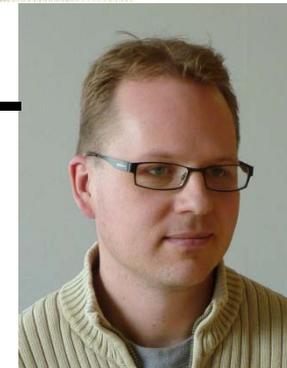
- Bram Nauta, University of Twente
- Jan Rabaey, UC Berkeley



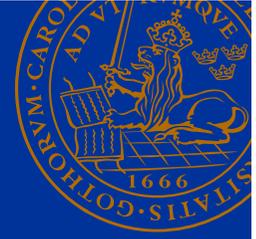
Welcome to two exiting days



- A Lund University perspective by senior researchers and PhD students
- Invited speakers from academia:
 - Bram Nauta, University of Twente
 - Jan Rabaey, UC Berkeley
- **An industrial perspective:**
 - Matthias Passlack, TSMC
 - Baudouin Martineau, STMicroelektronics
 - Thomas Olsson, Ericsson Research

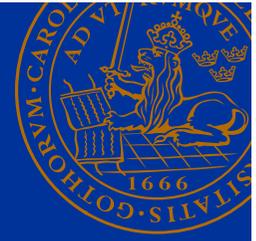


Welcome to two exiting days



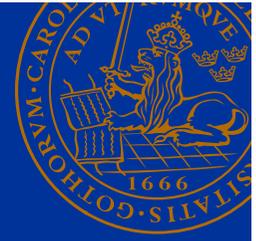
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- Invited speakers from academia:
 - Bram Nauta, University of Twente
 - Jan Rabaey, UC Berkeley
- An industrial perspective:
 - Dag T. Wisland, Novelda AS
 - Lars Risbo, TI Denmark
 - Sami Vilhonen, ST Ericsson Finland
- **Social activities including: The Dinner**

Some Logistics!



- Today's program is at Grand Hotel including Lunch.
- Dinner in the Main Building of Lund University.
- Tomorrow's programs is at the Faculty of Engineering, Lund University.

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Dinner : Main Building of Lund University



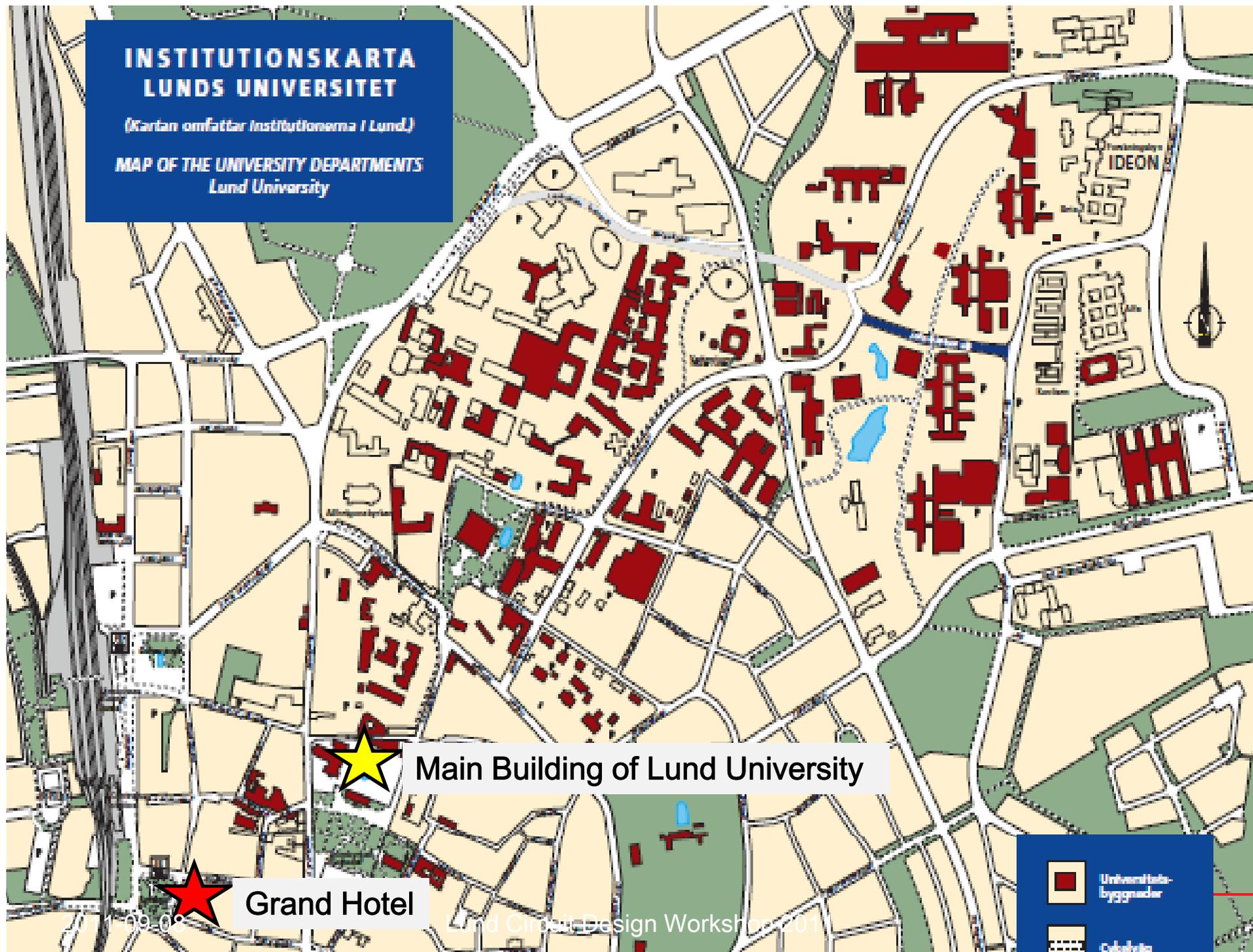
2011-09-08

Lund Circuit Design Workshop 2011

INSTITUTIONSKARTA LUNDS UNIVERSITET

(Kartan omfattar institutionerna i Lund.)

MAP OF THE UNIVERSITY DEPARTMENTS
Lund University

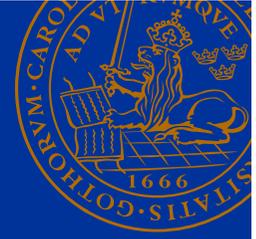


★ Main Building of Lund University

★ Grand Hotel

- Universitetsbyggnader
- Cykelväg

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- Today's program is at Grand Hotel including Lunch.
- Dinner in the Main Building of Lund University.
- Tomorrow's programs is at the Faculty of Engineering, Lund University.
Approximately 20-25min walk from Grand Hotel.

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MAP OF THE UNIVERSITY DEPARTMENTS
Lund University



E-building, Faculty of Engineering



Grand Hotel



Universitets-
byggnader



Cykelföring

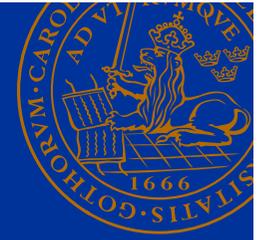
E-building: faculty of Engineering



2011-09-08

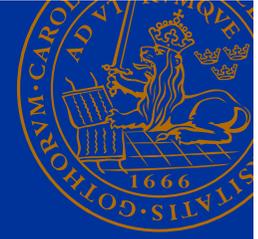
Lund Circuit Design Workshop 2011

The Hosts



From VINNOVA's evaluation 2011: "SoS builds on strong long-term relations with top industry partners in the international arena in the Center's strategic area which is **highly relevant to the Swedish economy**. The SoS team represents an **impressive range of research talent and experience**, including many staff with international records of achievement and clearly shows that **they can compete on an international level**. "

People in



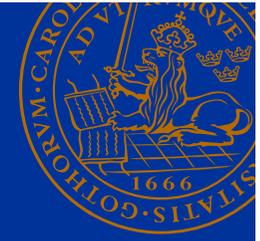
Director: Viktor Öwall, Co-director: Pietro Andreani
Chairman of the Board: Sven Mattisson, Ericsson AB



International Advisory Board

- Professor Jan Rabaey, BWRC, UC Berkeley, USA
- Professor Mike Faulkner, Victoria University, Australia
- Professor Qiuting Huang, ETH, Zürich, Switzerland

The Hosts



WWW

Wireless with Wires

UPD



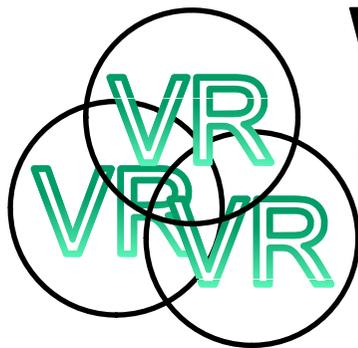
**Wireless Communication for
Ultra Portable Devices**

Research Grants



New projects:

- DARE
- Distant
- HIPEC

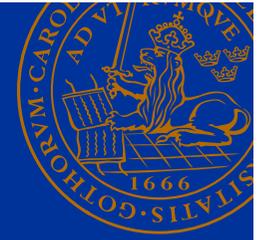


WWW

UPD



New this year at the workshop

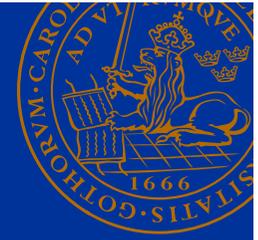


Instead of presenting different research grants we have put together a slide show on



...and one with introductions to tomorrow's poster sessions.

Grand Slam at SSF!



We have been very successful this year and attracted three large SSF Grants:



- DARE – Digitally Assisted Radio Evolution
PI Pietro Andreani
- Distrant - Distributed Antenna Systems
PI Fredrik Tufvesson
- HiPEC - High Performance Embedded Computing
PI Kris Kuchcinski

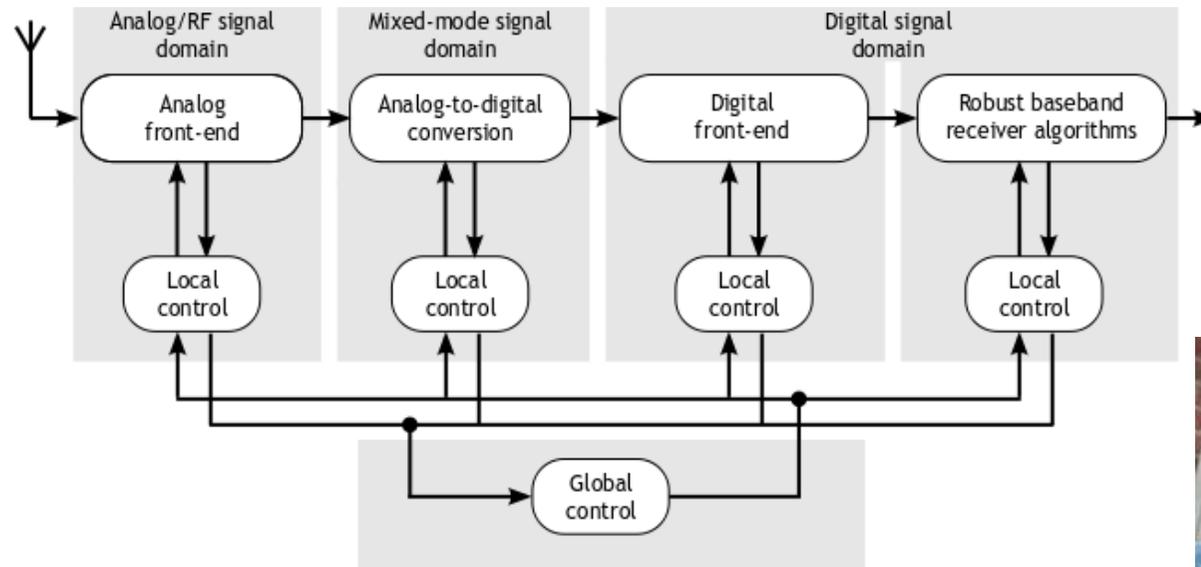


” – Vi bedömer strategiskt relevans och vetenskaplig kvalitet på ansökningarna och där låg Lund bäst till i denna utlysning. ”, Joakim Amorin, SSF

DARE – Digitally Assisted Radio Evolution



SSF grant, 29 MSEK over 5 years, starts Sept. 2011 with 6 PhD students

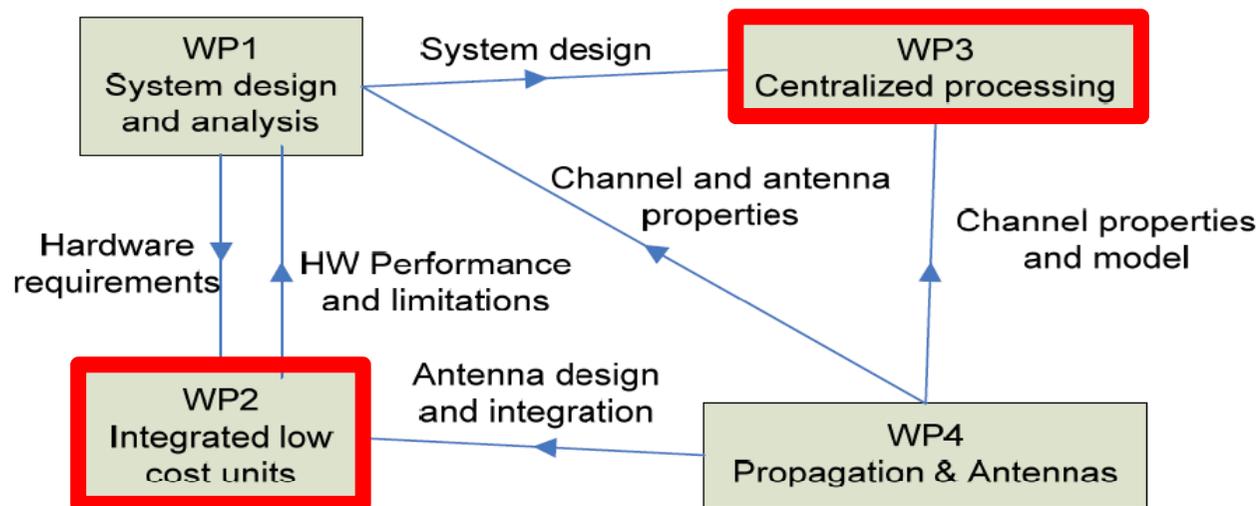


- *Target: LTE – rel. 10*
- Key radio blocks in nm CMOS
- Digital control and adaptation of analog, mixed-signal, and digital blocks
- Improved trade-off between performance and power consumption

Distrant - Distributed Antenna Systems



SSF grant, 27.2 MSEK over 5 years, starts Sept. 2011 with 5 PhD students

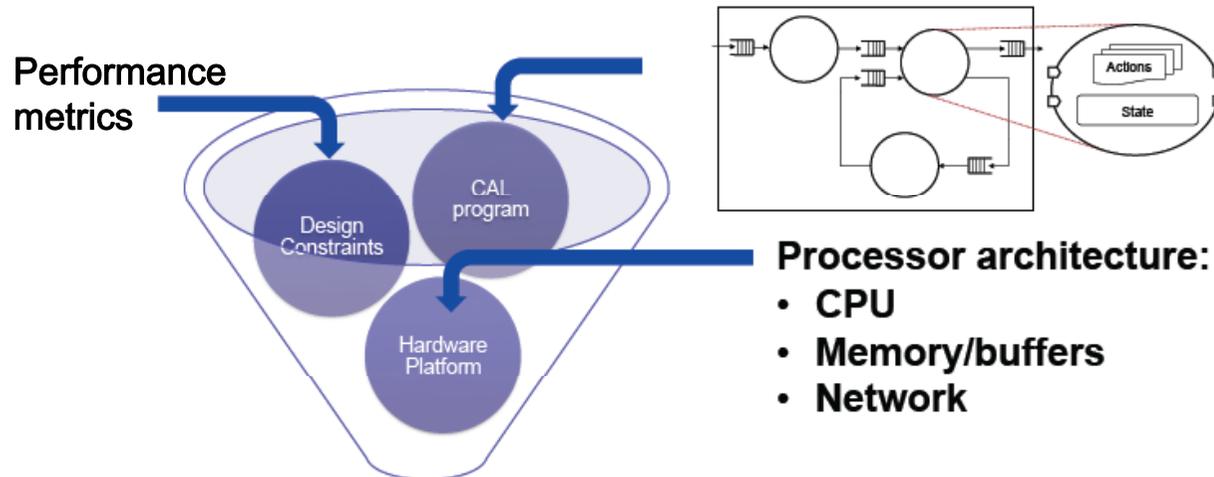


- *Large antenna arrays (~100) to be grouped together to form large arrays or distributed in the environment as a sparse array .*
- To achieve: increased capacity, improved coverage, reduced energy dissipation

HiPEC - High Performance Embedded Computing



SSF grant, 25.9 MSEK over 5 years, starts Sept. 2011 with 5 PhD students

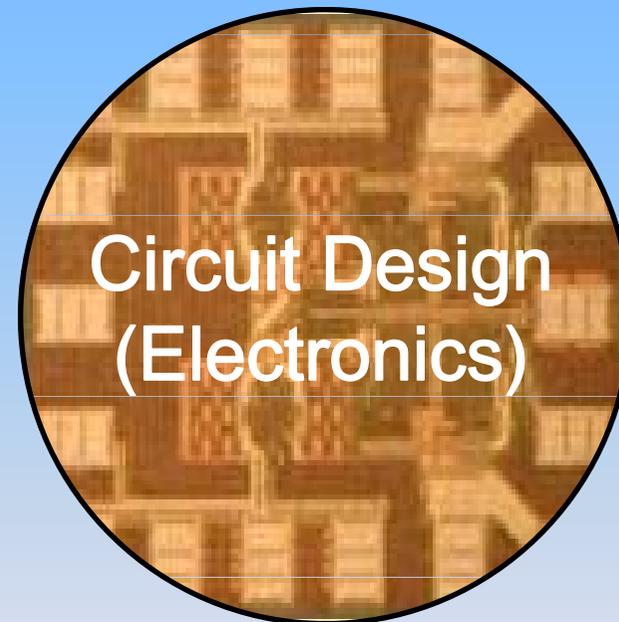
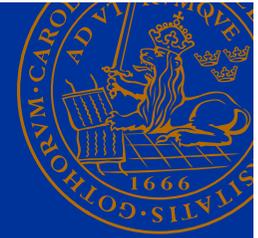


Utilizing the Reconfigurable Array developed within SoS

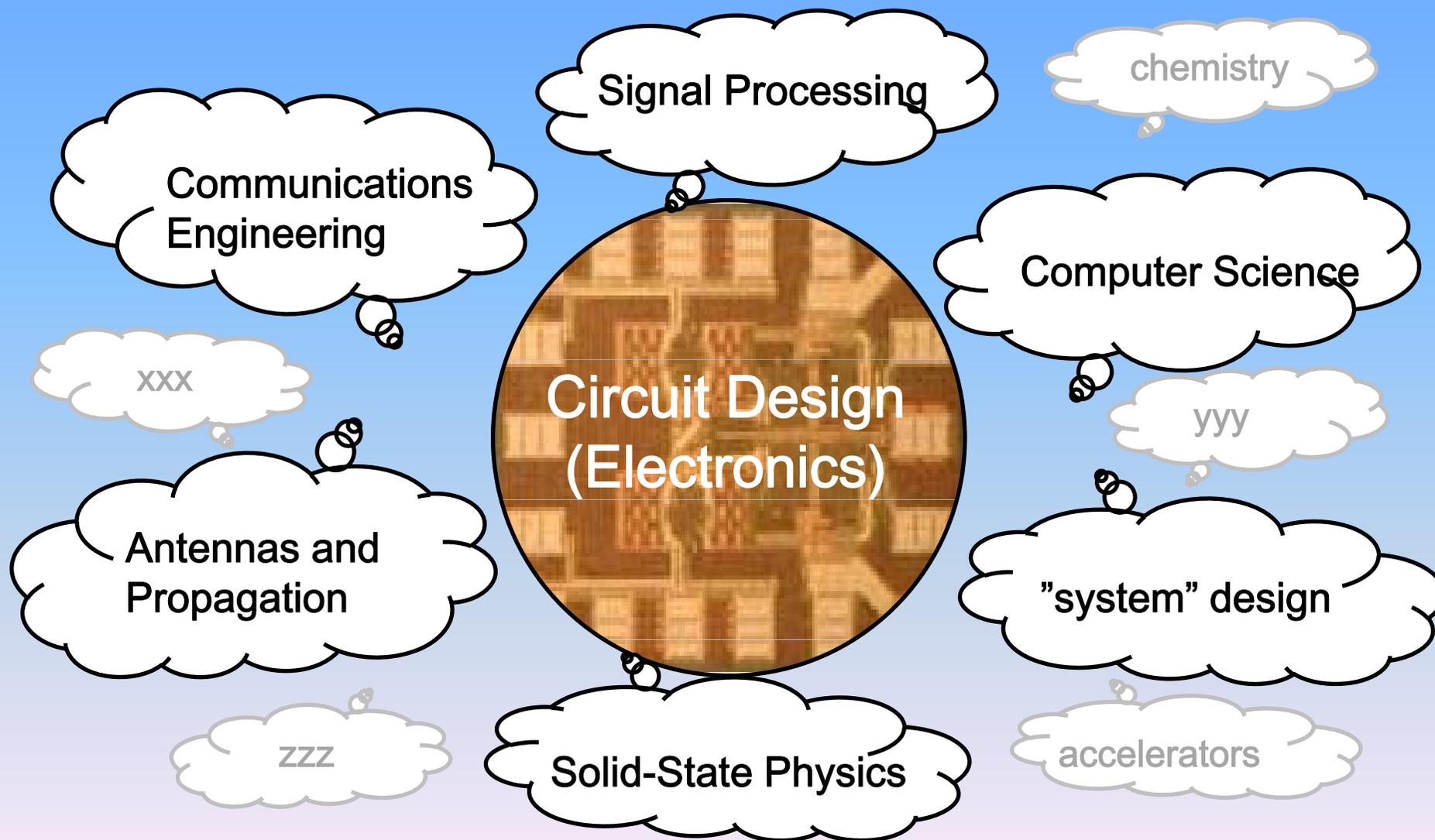


- *Develop reconfigurable embedded execution platform.*
- *Automatic translation, mapping and scheduling based on the CAL dataflow language*

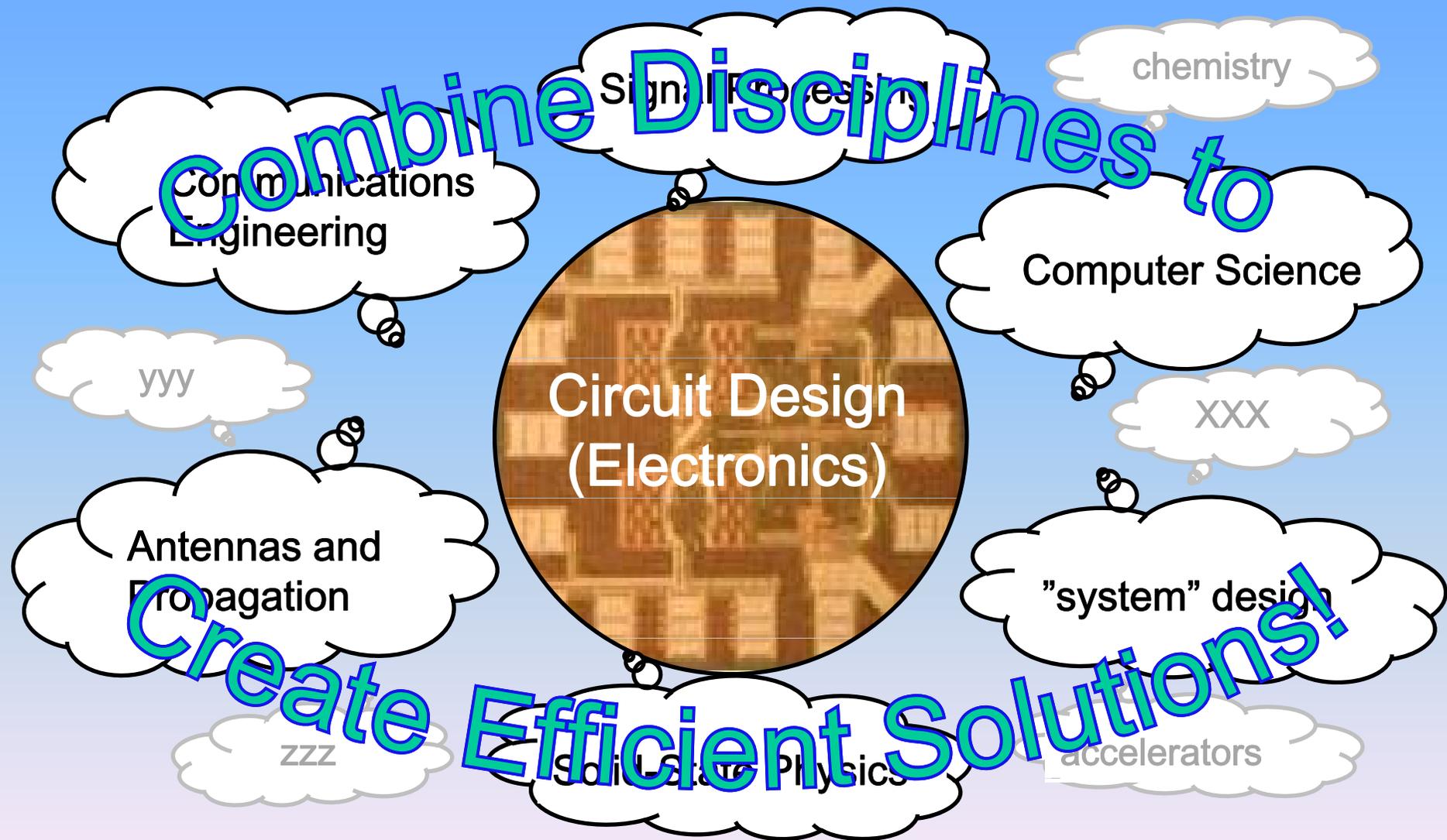
Research Environment – from both academic and industrial networks



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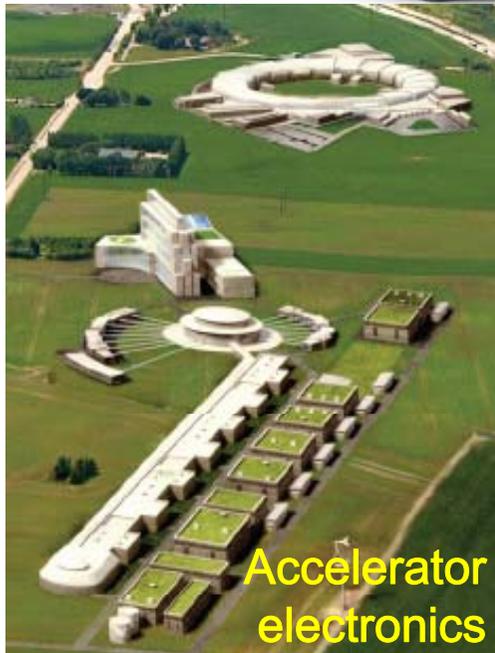
Research Environment – from both academic and industrial networks



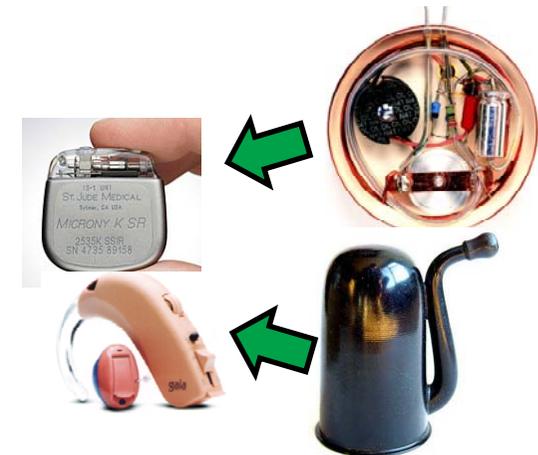
Application areas



Main Focus:



Wireless/cellular systems

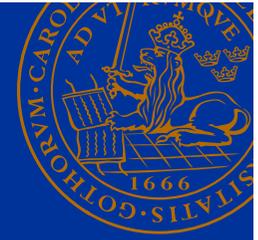


Medical applications, including wireless

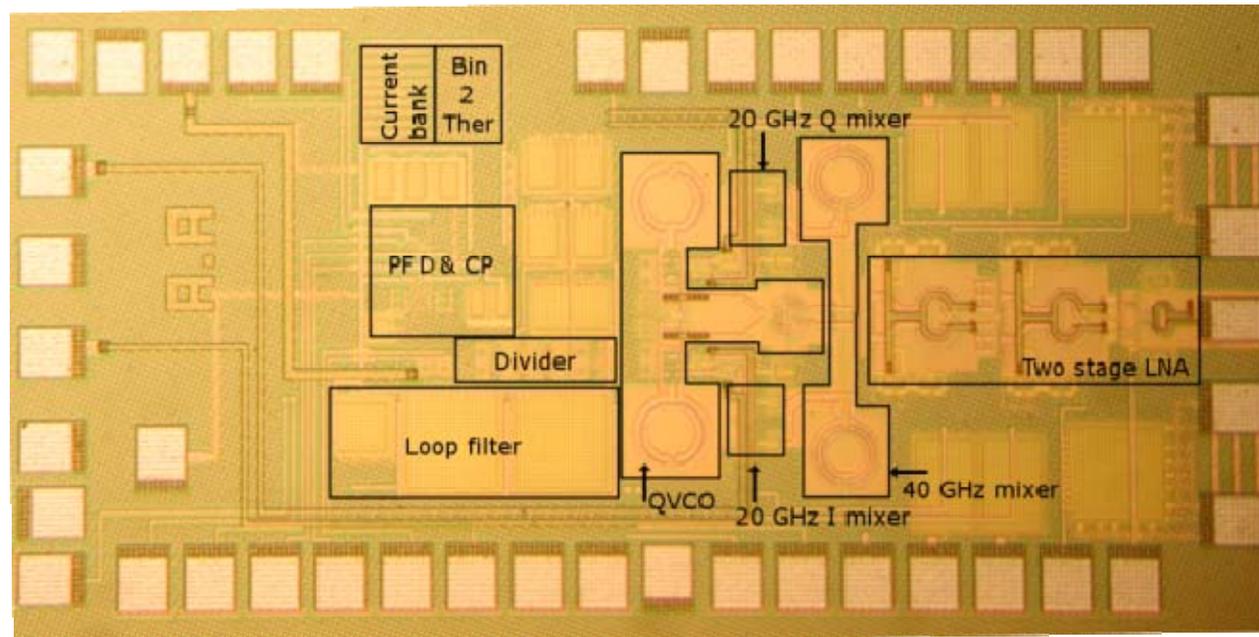


...and some research highlights!

mmWave Beamforming circuits



Andreas Axholt defended his PhD thesis September 7!

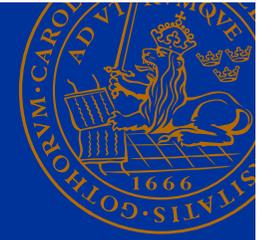


Measured and working

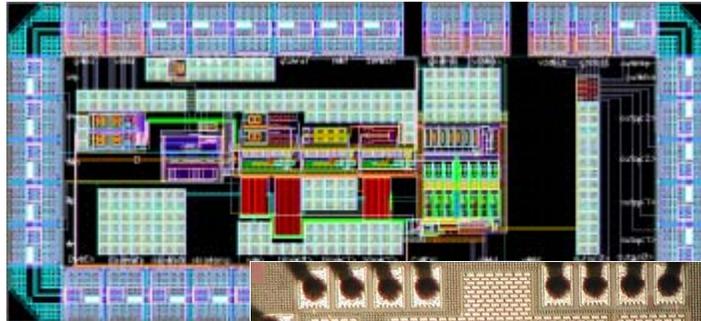
60 GHz, 20 GHz PLL, Transformers, Balun, Mixers, LNAs, QVCO, Binary-to-Thermometer decoder



Continuous-Time $\Delta \Sigma$ -ADC

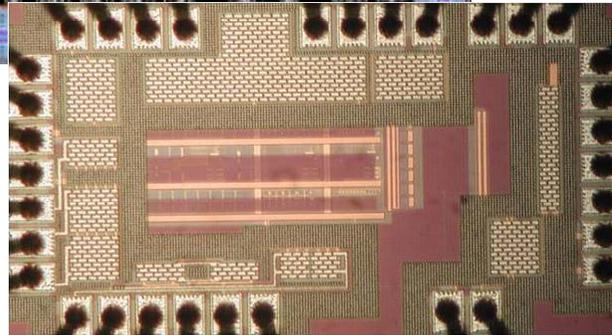


- LTE

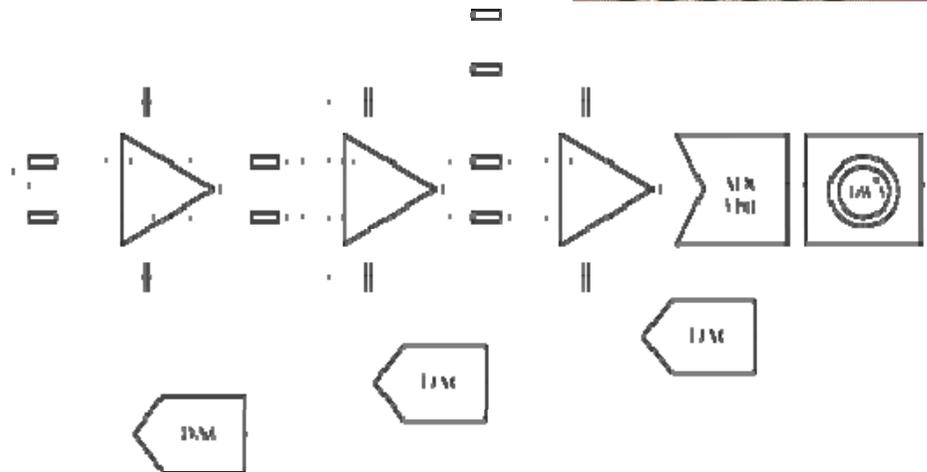


by Mattias Andersson

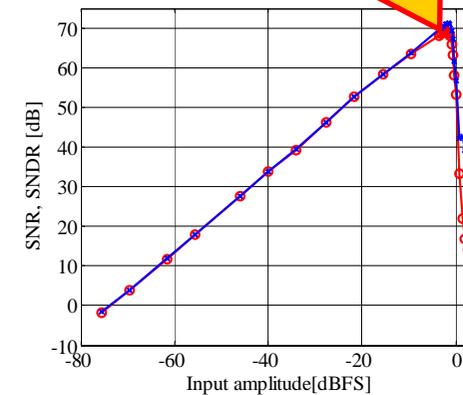
- Low Power Radios



by Dejan Radjen

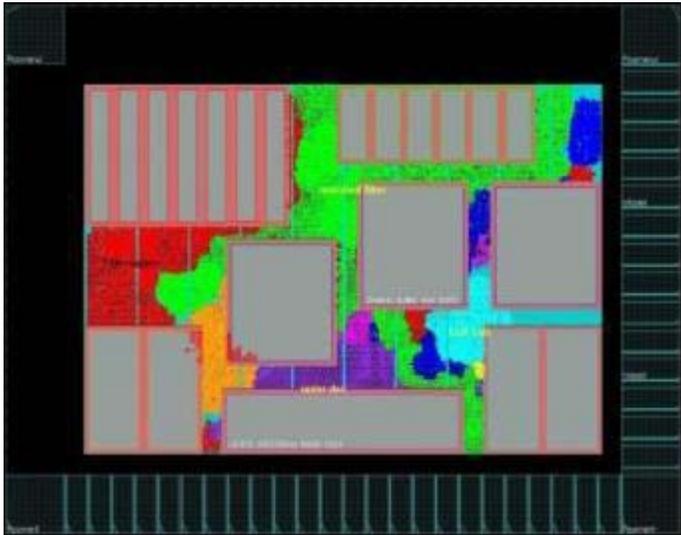
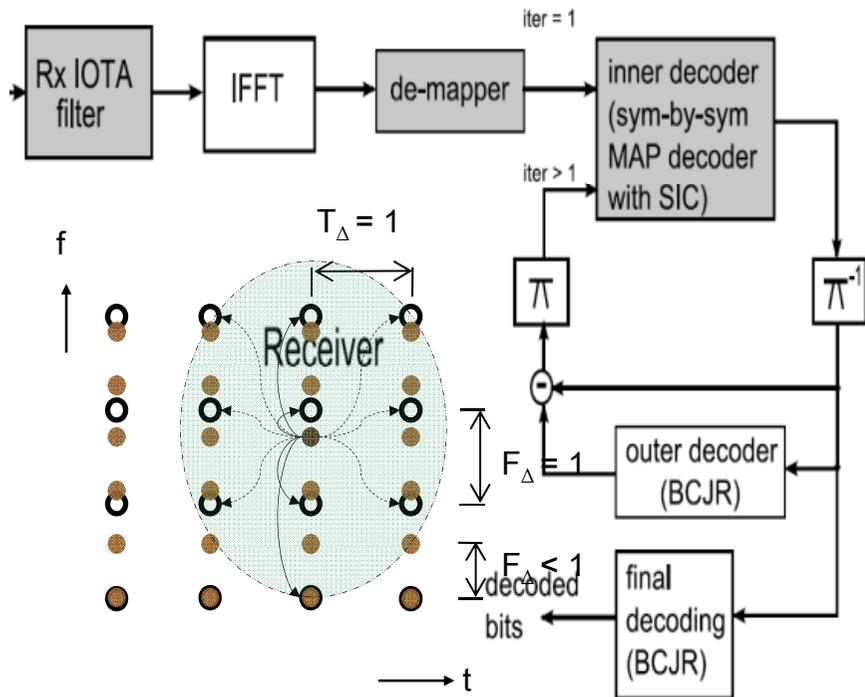


Peak SNDR 69dB
Peak SNR 71dB



Faster-than-Nyquist (FTN) receiver

FTN iterative receiver



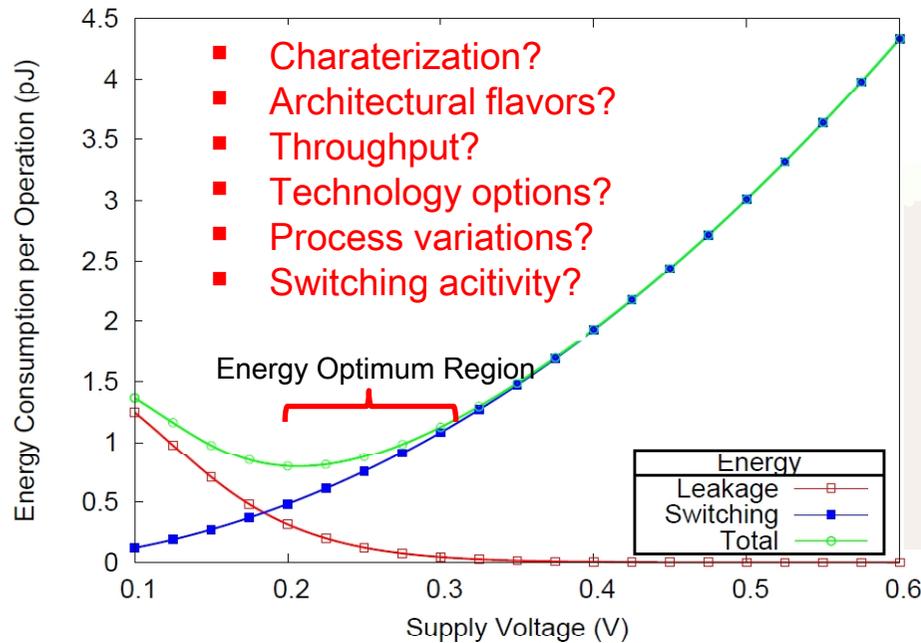
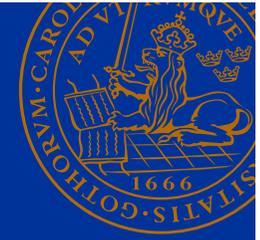
Fabricated in ST65nm CMOS
Measured.
Demo tomorrow.

Motivation:

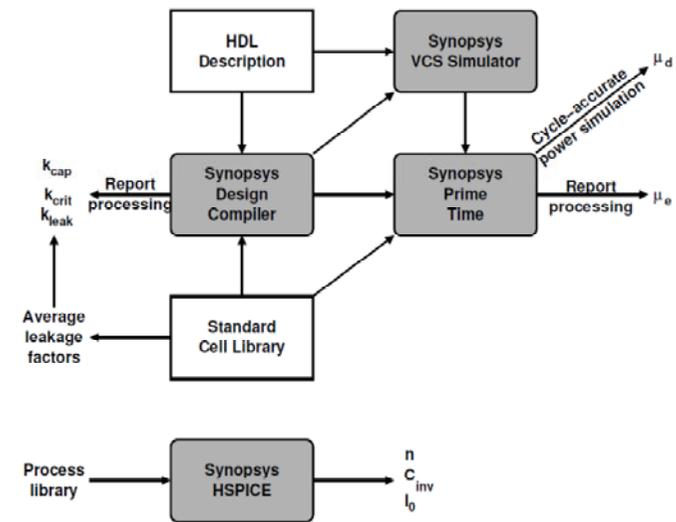
- increased bandwidth efficiency
- is FTN hardware feasible?

Deepak Dasalukunte to defend PhD thesis December/January.

Digital Circuits in Weak Inversion



High-level Modeling in the Sub- V_T Domain



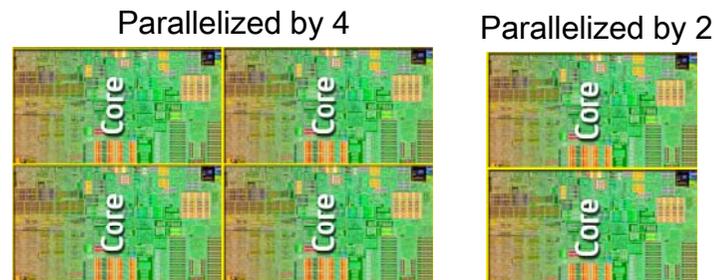
Applied to a decimation chain filter in the UPD-project

Decimate data from 8-Msamples/s to 0.25-Msamples/s.

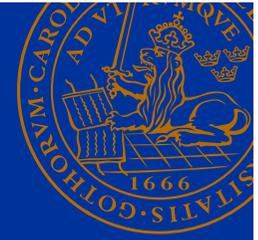
Different throughputs



Different Architectures



InAs Nanowire Mixer Circuit Integration

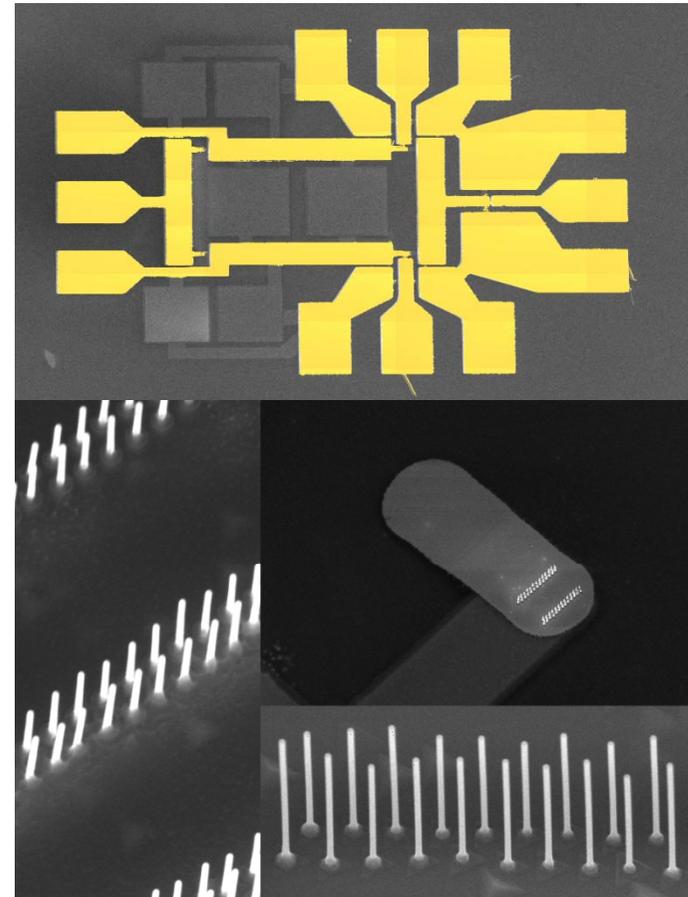


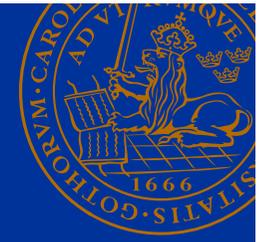
Goal

- Integration of InAs NW single balanced differential mixer circuit
- Demonstrating performance advantageous compared to similar Si technology

Results

- Single and Array Vertical NW Transistor Performance
 - g_m - 1 S/mm
 - f_t - 20 GHz
 - f_{max} - 30 GHz





**Thank You
and
Enjoy!**