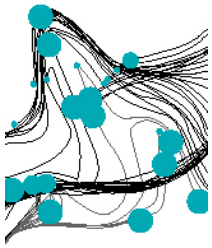

Interferer Robust Wide-band Receiver Techniques

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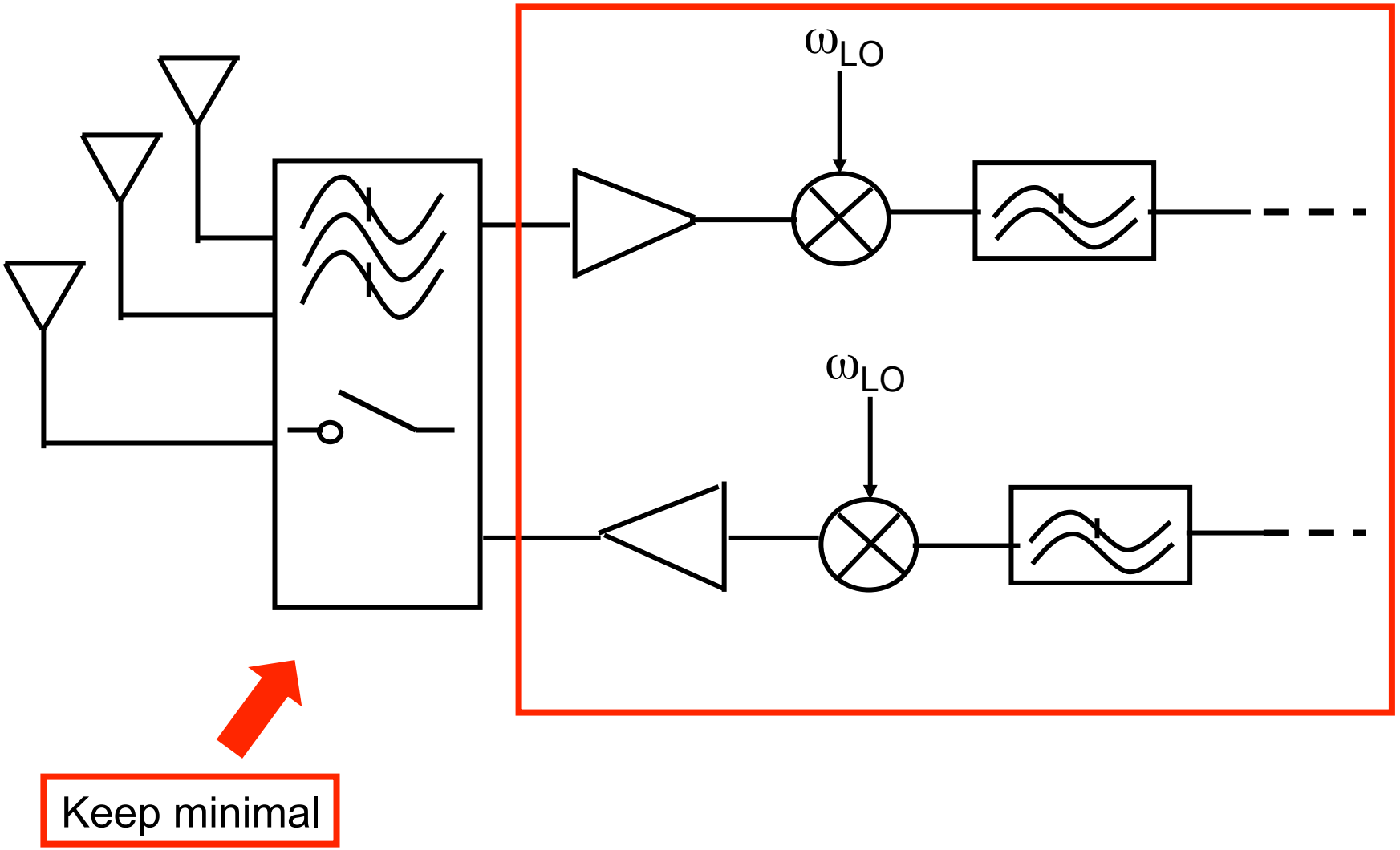
UNIVERSITY OF TWENTE.

Outline

- Introduction
- Interferer robust SDR RX – analog part
- Interferer robust SDR RX – digital part
- Mixer-first RX
- N-path RF filter
- Interferer scrambler for Software Radio

Preferred: one wide band frontend IC:
Software Defined



RF system trend (I)

- Challenges **wide band** circuits:

Minimal pre-filtering: → high linearity

No high Q tanks: → low noise

- Bandwidth will be ok for low GHz

- Towards Software Defined Radio

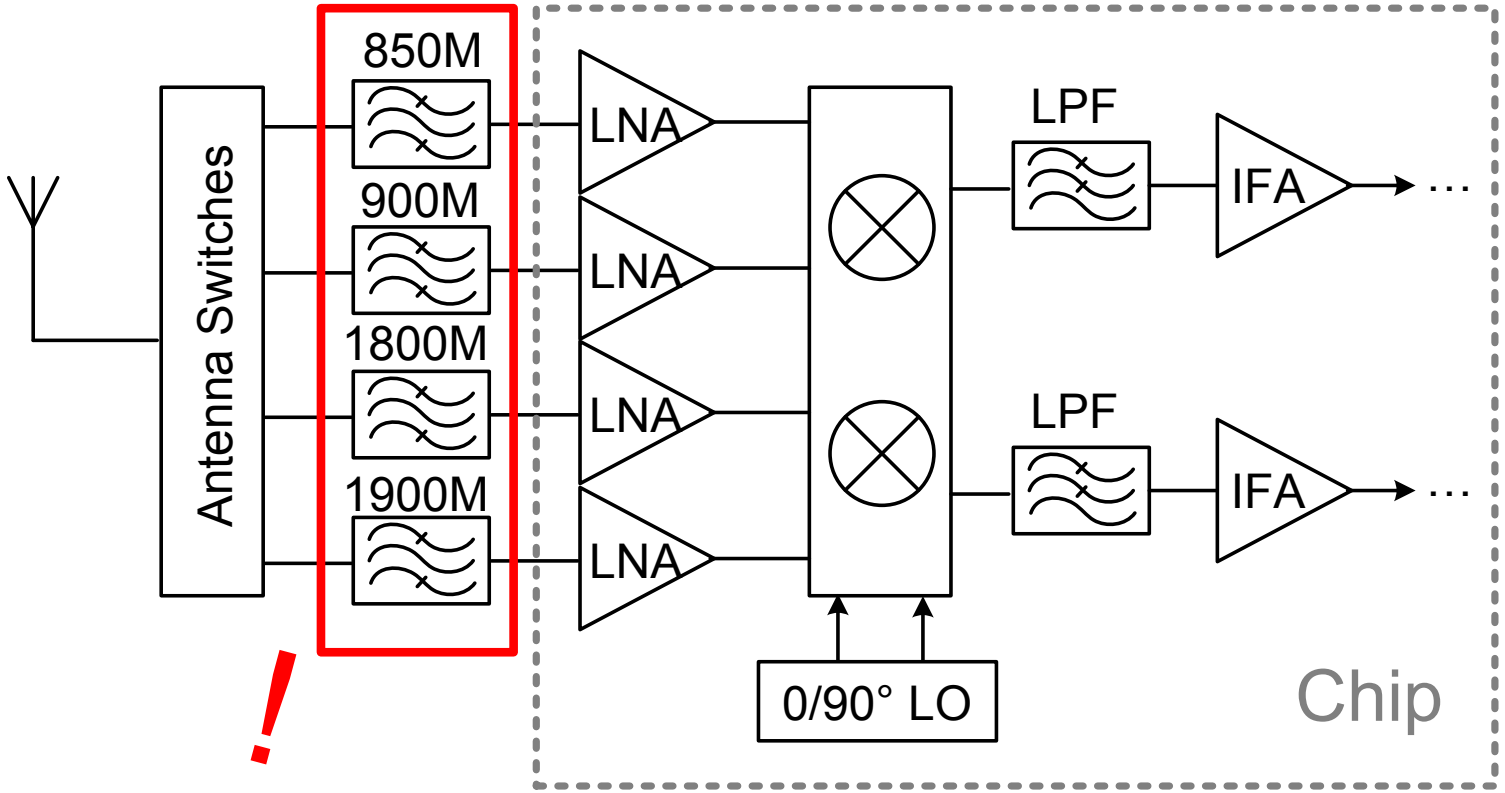
Outline

- Introduction
- **Interferer robust SDR RX – analog part**
- Interferer robust SDR RX – digital part
- Mixer-first RX
- N-path RF filter
- Interferer scrambler for Software Radio

A Software-Defined Radio Receiver Architecture Robust to Out-of-Band Interference

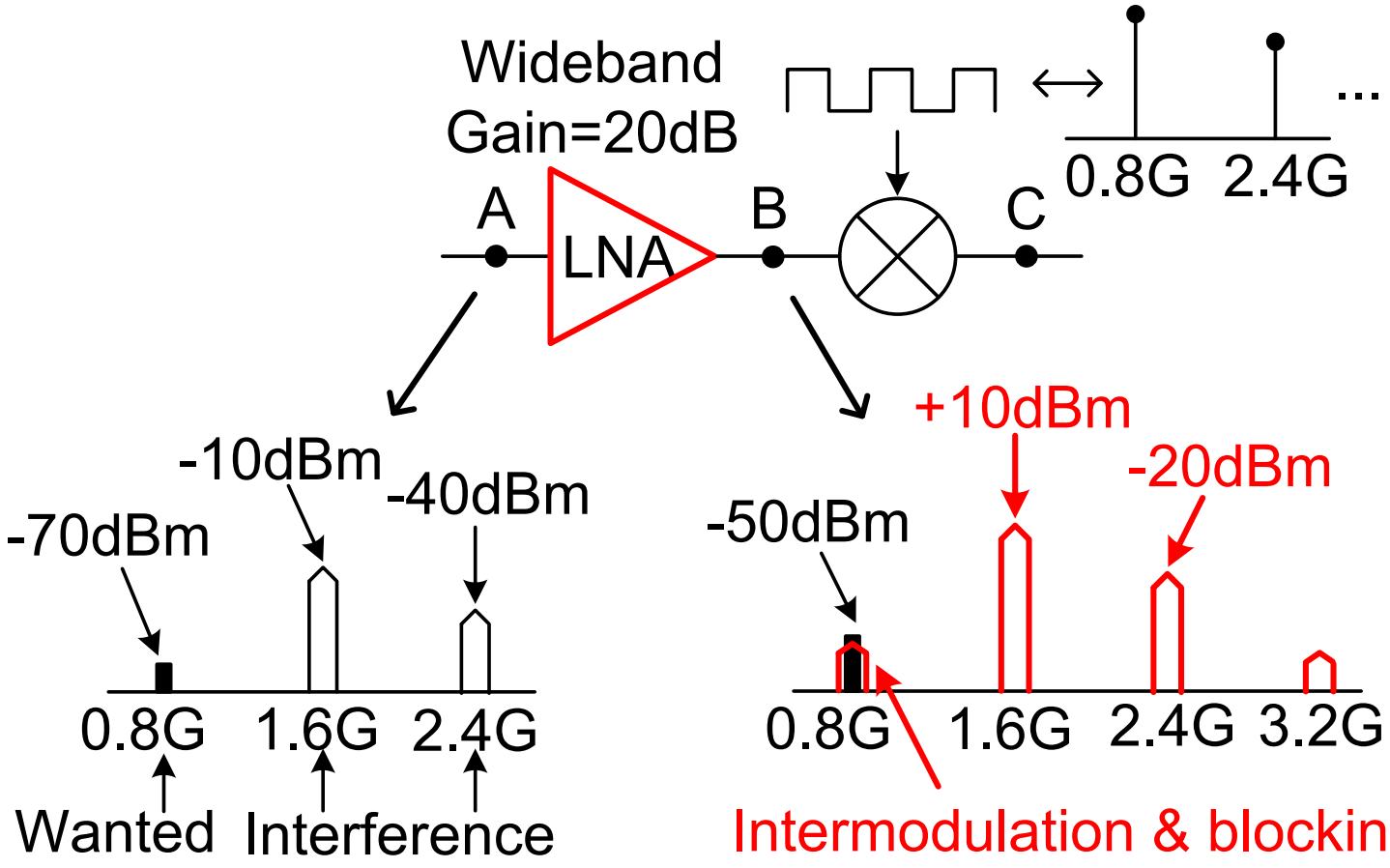
[Ru, ISSCC 2009]

Conventional Multi-Band Receiver



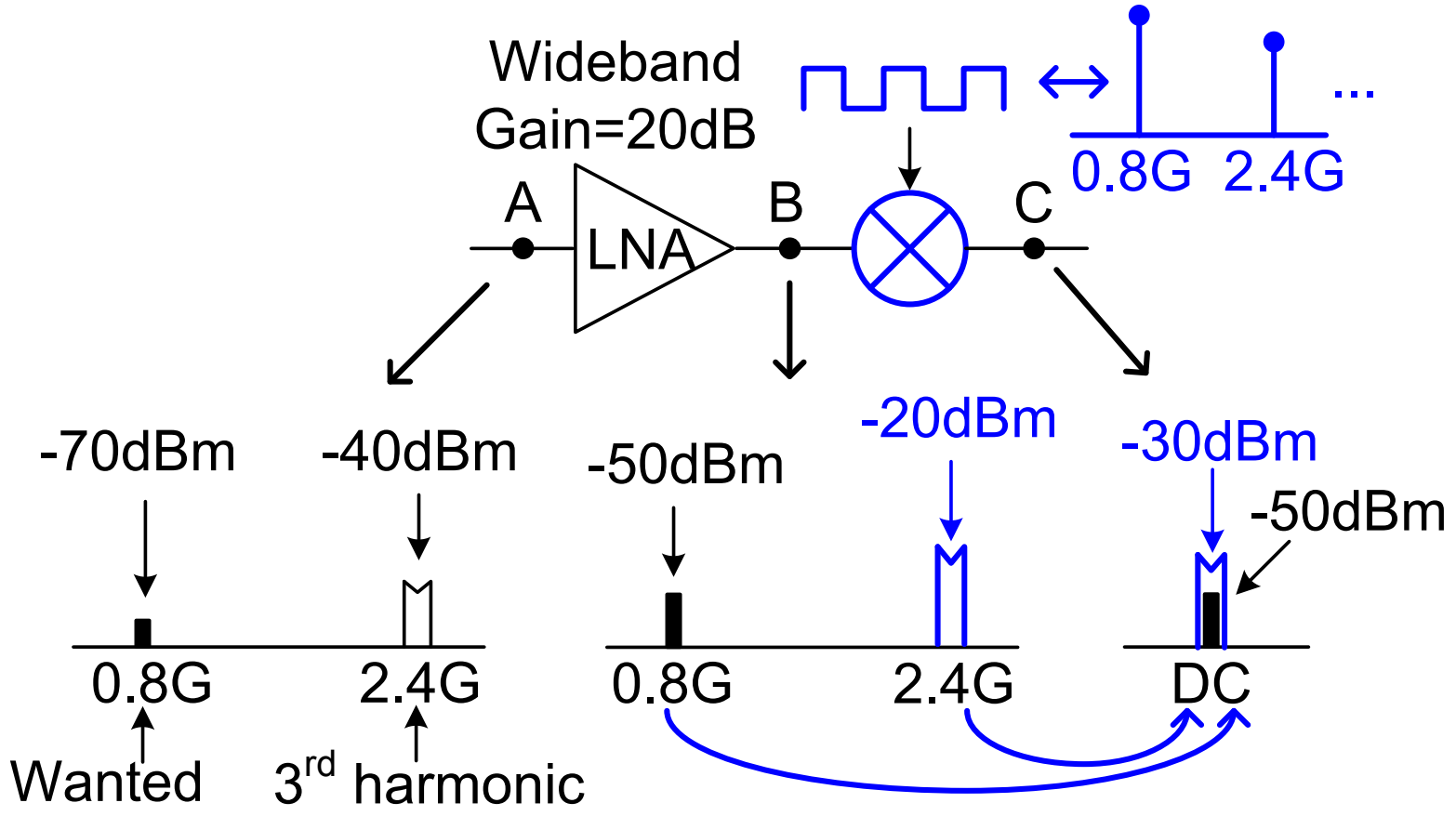
- RF filters for out-of-band interference, but bulky, costly, lossy, inflexible…
- **Our goal: Software Defined Radio with relaxed RF filtering**

Wideband Interfering: Nonlinearity



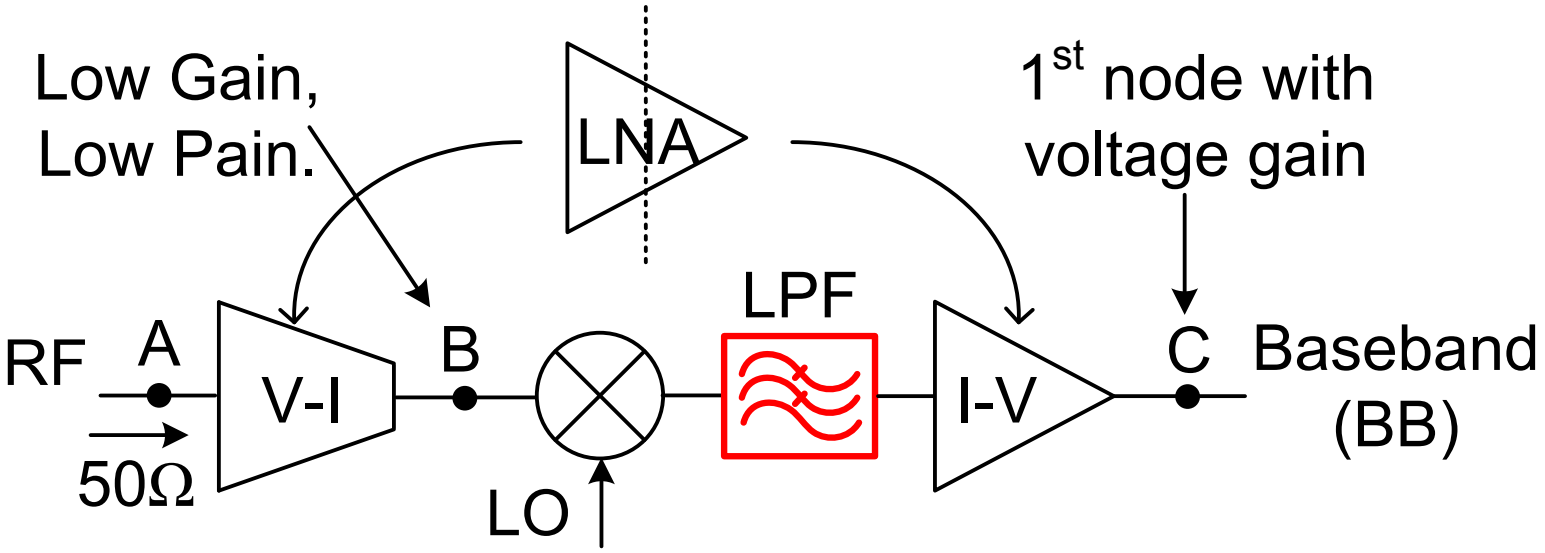
- Wideband LNA: also amplifies interference → nonlinearity

Wideband Interfering: Harmonic Mixing



- Switching mixer: square-wave LO → harmonic mixing

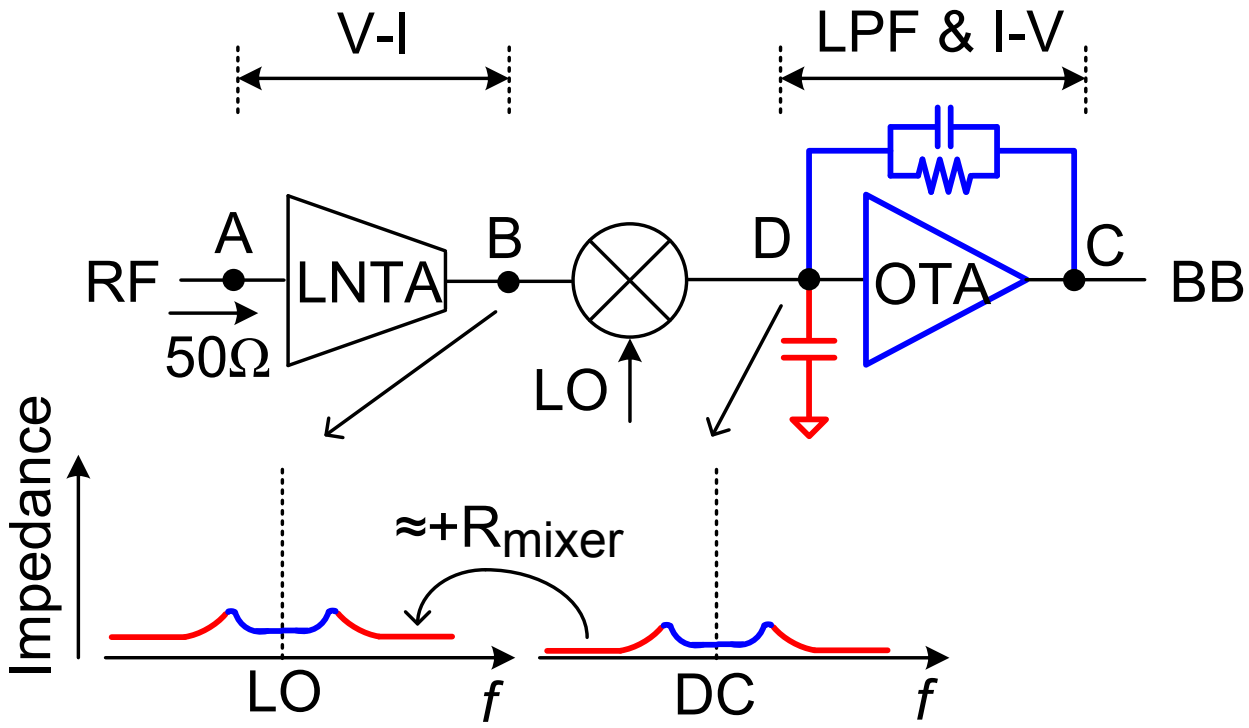
Concept: Use LP Filtering for Selectivity



- Voltage gain only at BB after **low-pass filter (LPF)** to filter blockers

→ Keep low impedance over a wide band at node B

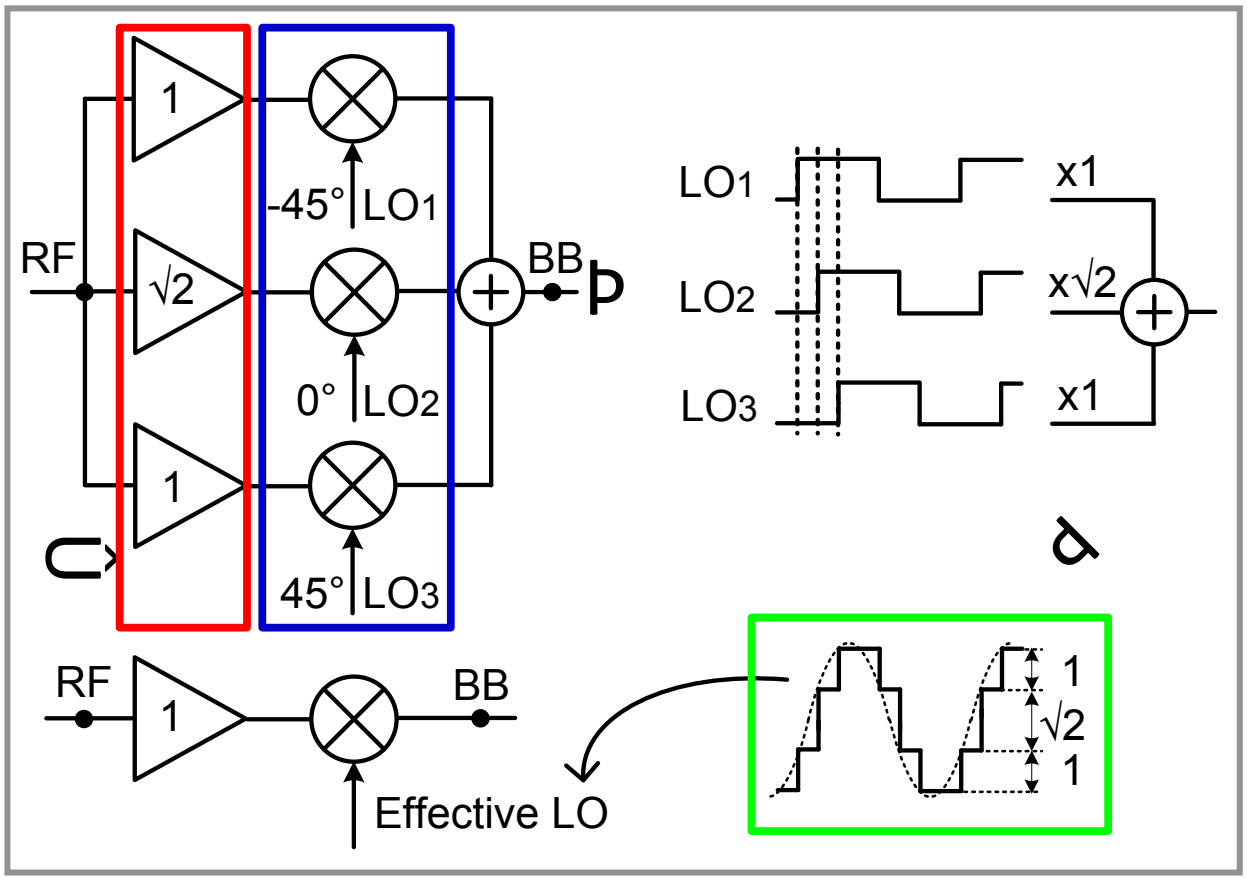
Realization: Wideband LNTA + Mixer + TIA

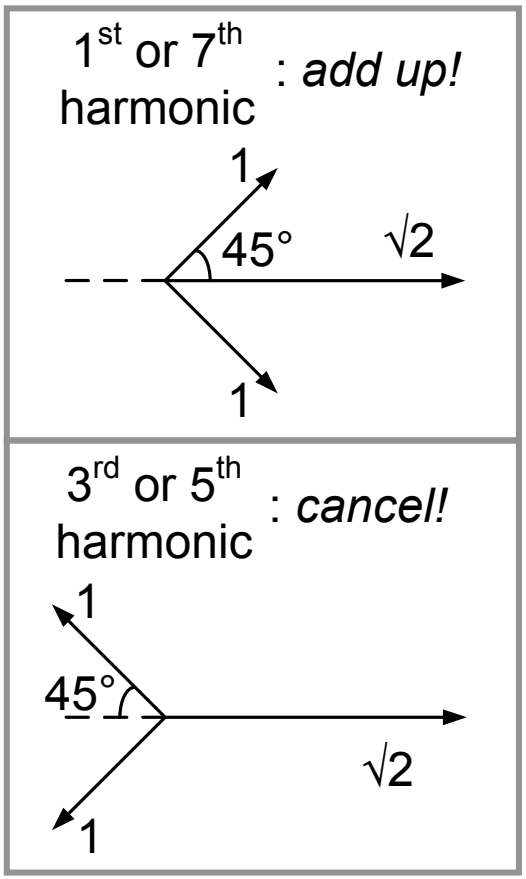


- LNTA: high G_m & high R_{out} → low noise
  small voltage swing at node B → good linearity
- Similar to [1], but now wideband and with blocker filtering

[1] Redman-White & Leenaerts, ESSCIRC07

Harmonic Rejection (HR) Mixer: Remove 3LO and 5LO



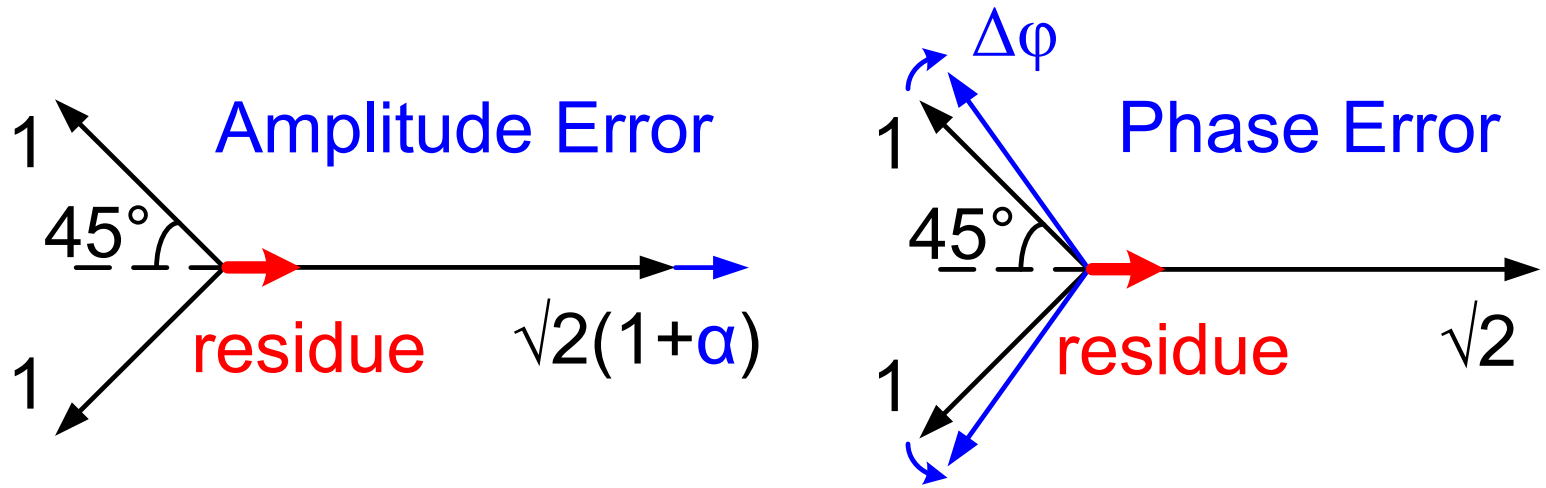


- Amplitude weighting + phase shifting → emulate sine-LO

[2] Weldon et. al., ISSCC01

Problem: Amplitude and Phase Errors

3rd or 5th harmonic vector diagram

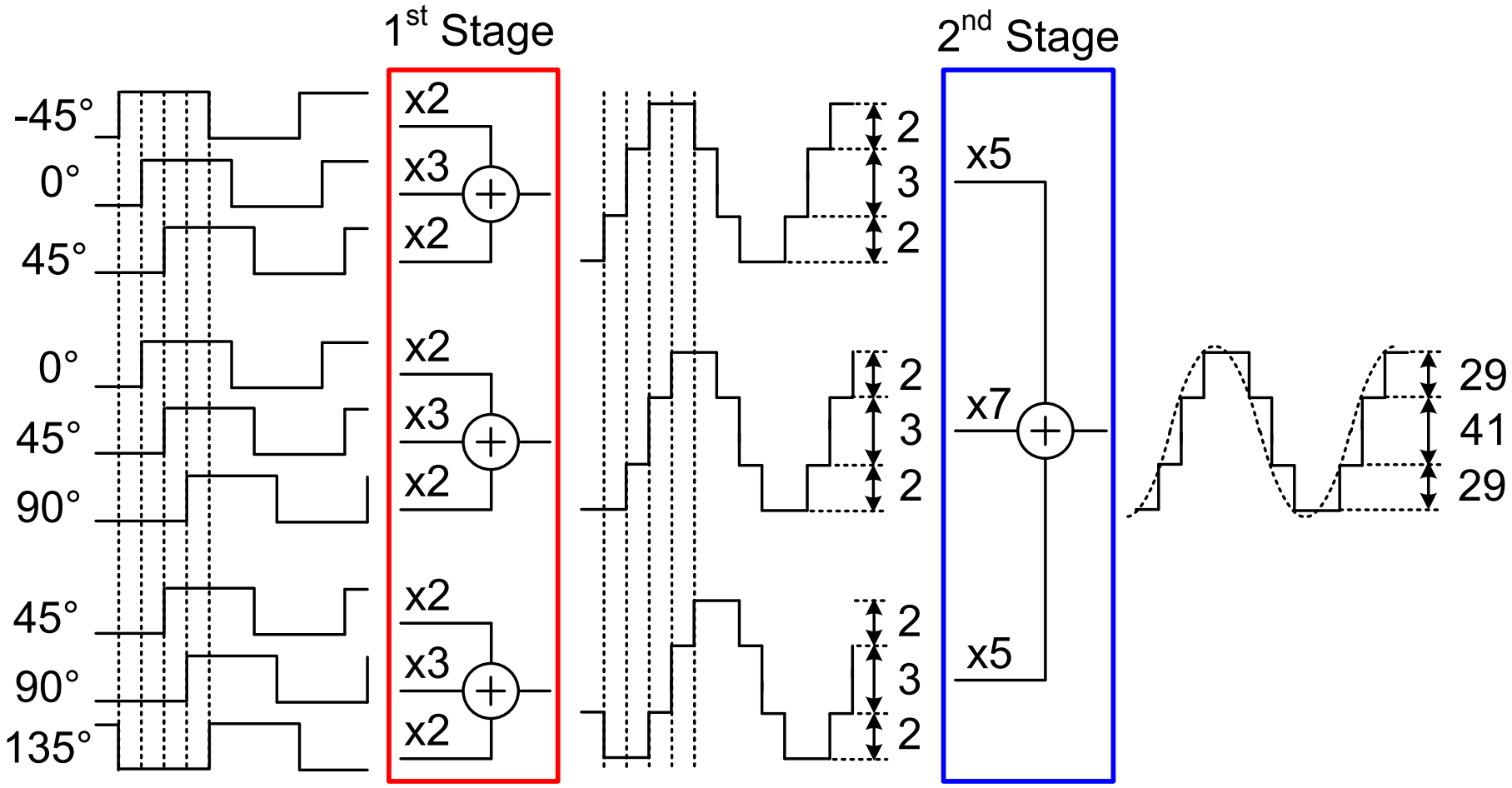


- Amplitude and phase errors

→ unwanted harmonic residue → degrade HR ratio

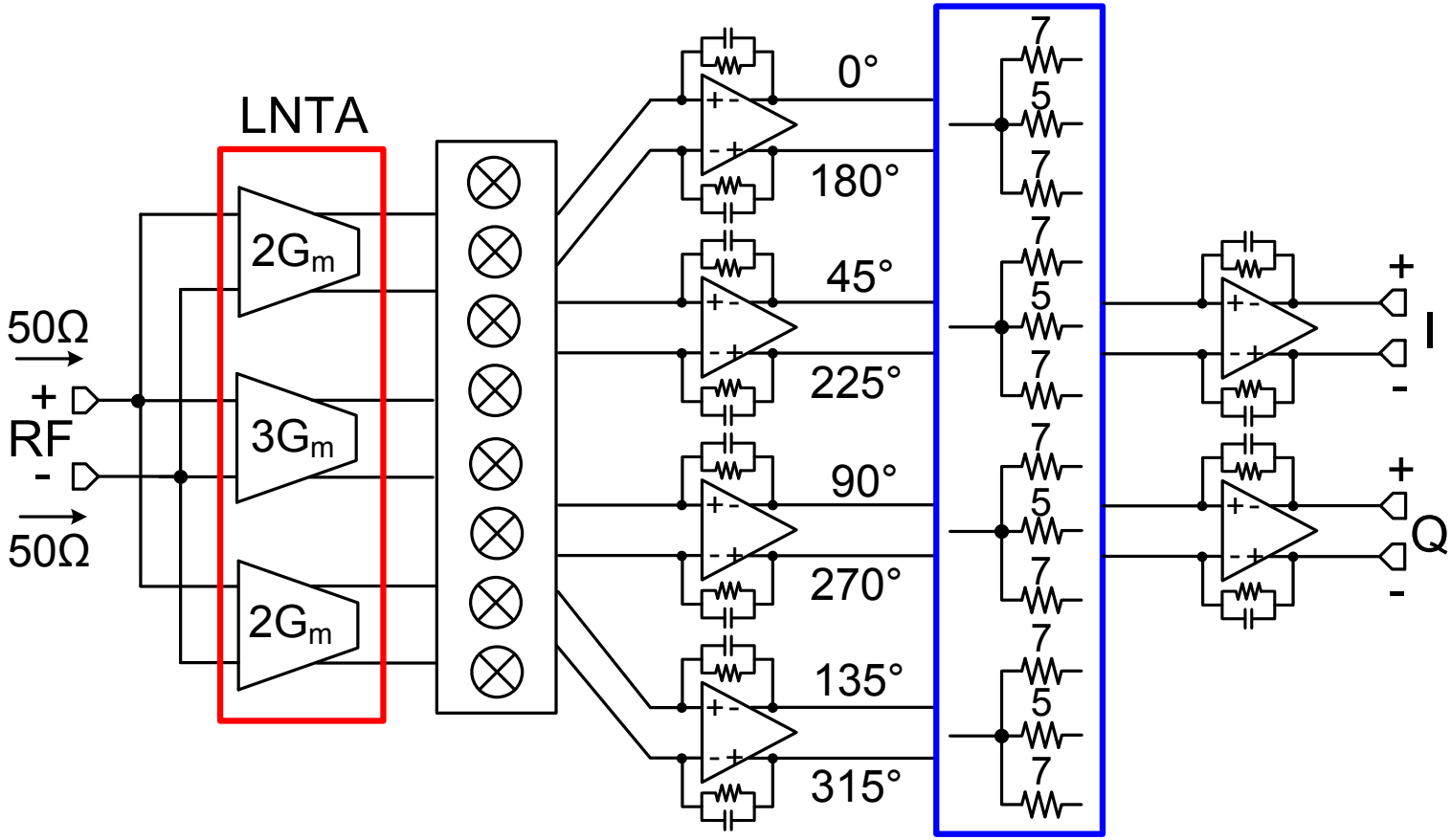
- How to make irrational ratio, e.g. √2, on chip?

2-Stage Polyphase HR: Concept



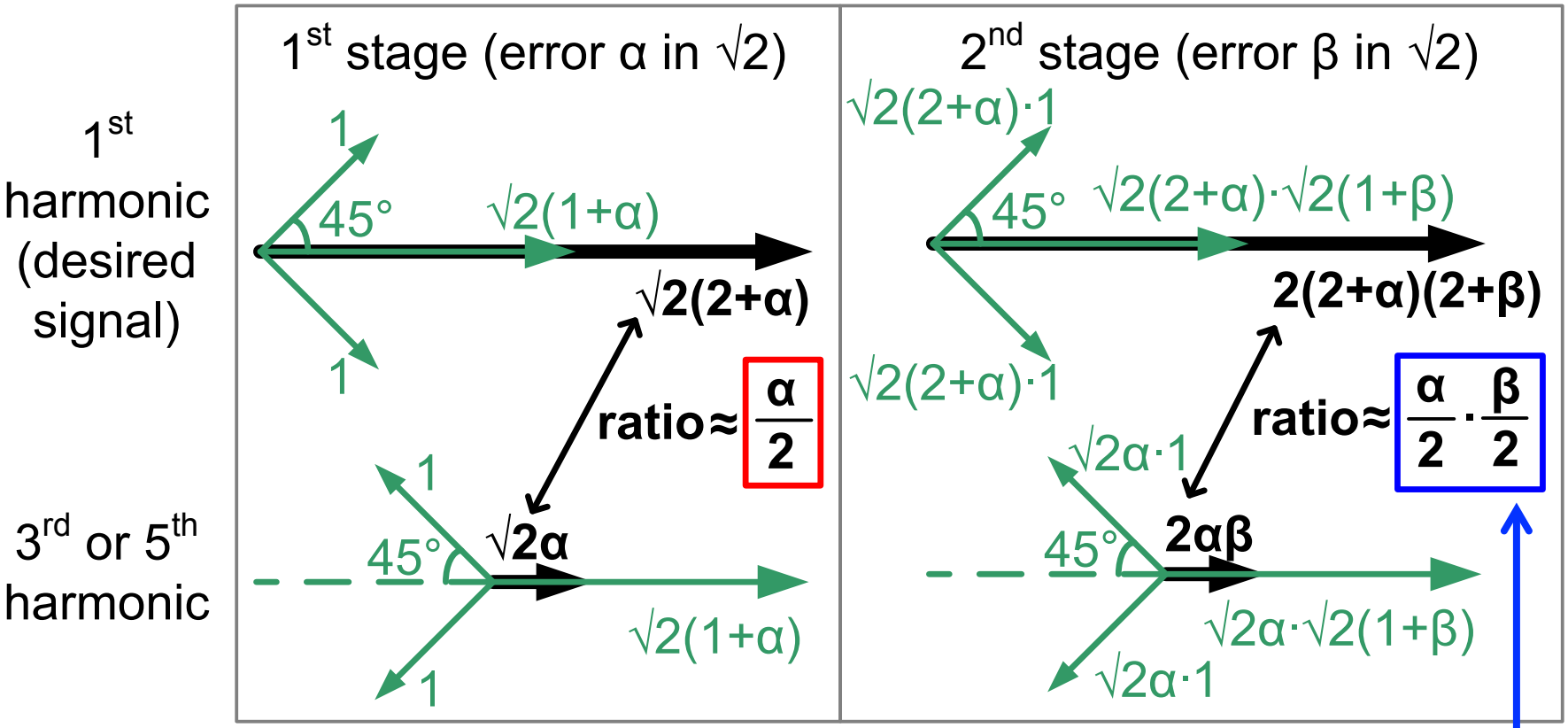
- 41/29=1.4138, √2=1.4142 → **ε=0.03%**

2-Stage Polyphase HR: Realization



- RF LNTA for 1st-stage weighting (2:3:2)
- BB resistor for 2nd-stage weighting (5:7:5)
- Nominally √2, what about influence of mismatch?

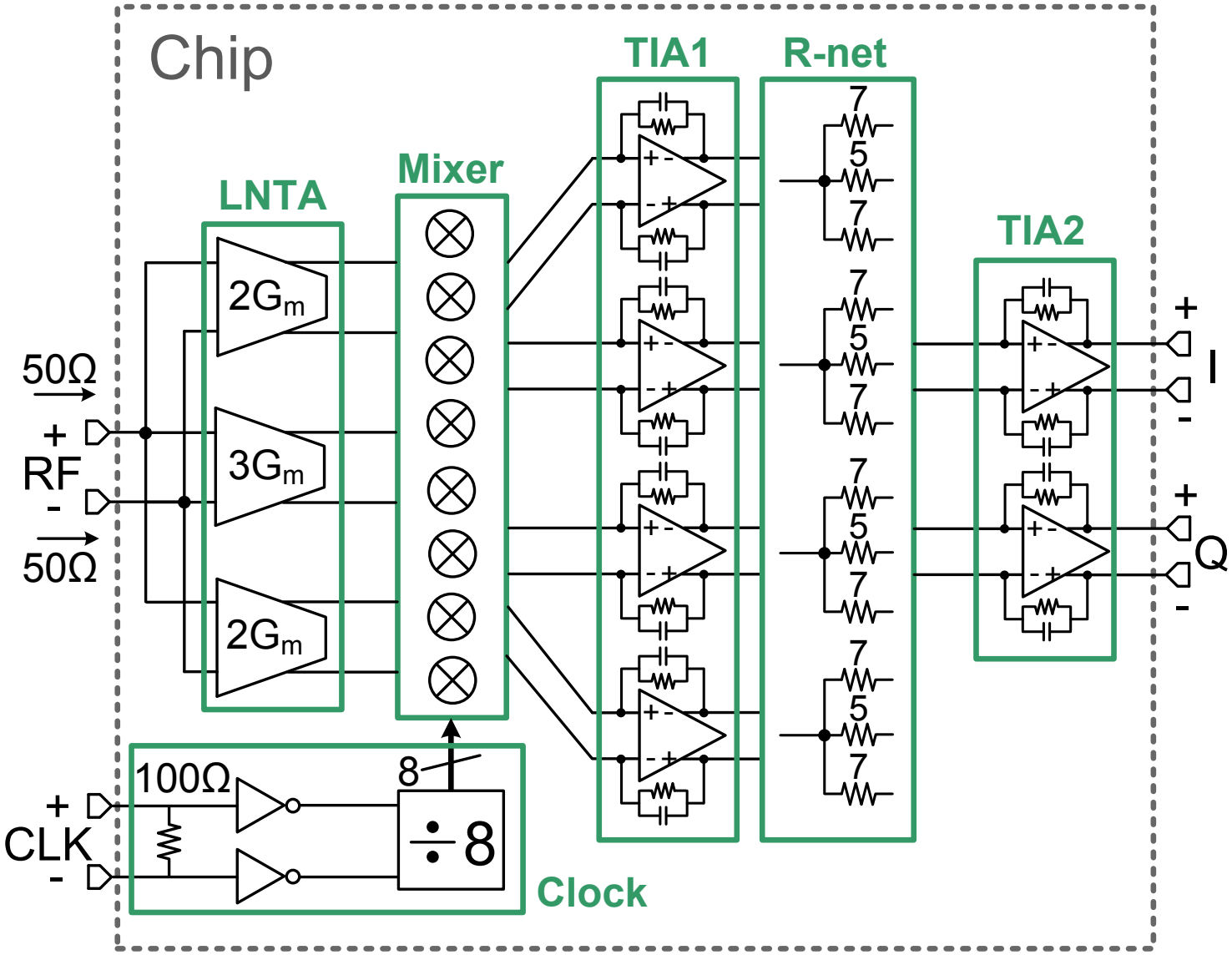
Reduced Effect of Amplitude Mismatch



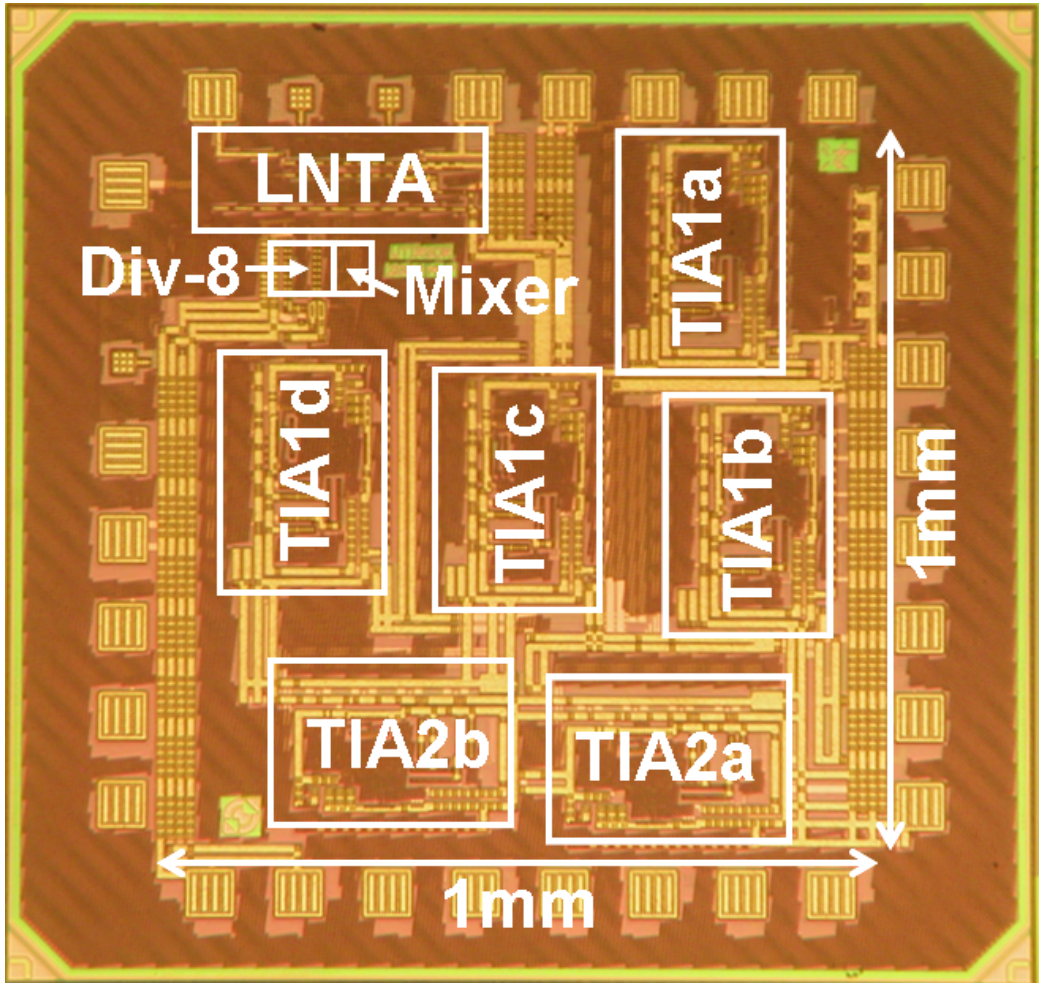
- 2-stage polyphase → product of relative errors
- E.g. 2:3:2 → α=6% → 1st-stage only: HR3=40dB

  5:7:5 → β=1% → 2-stage total: HR3=86dB

Zero-IF Receiver Prototype

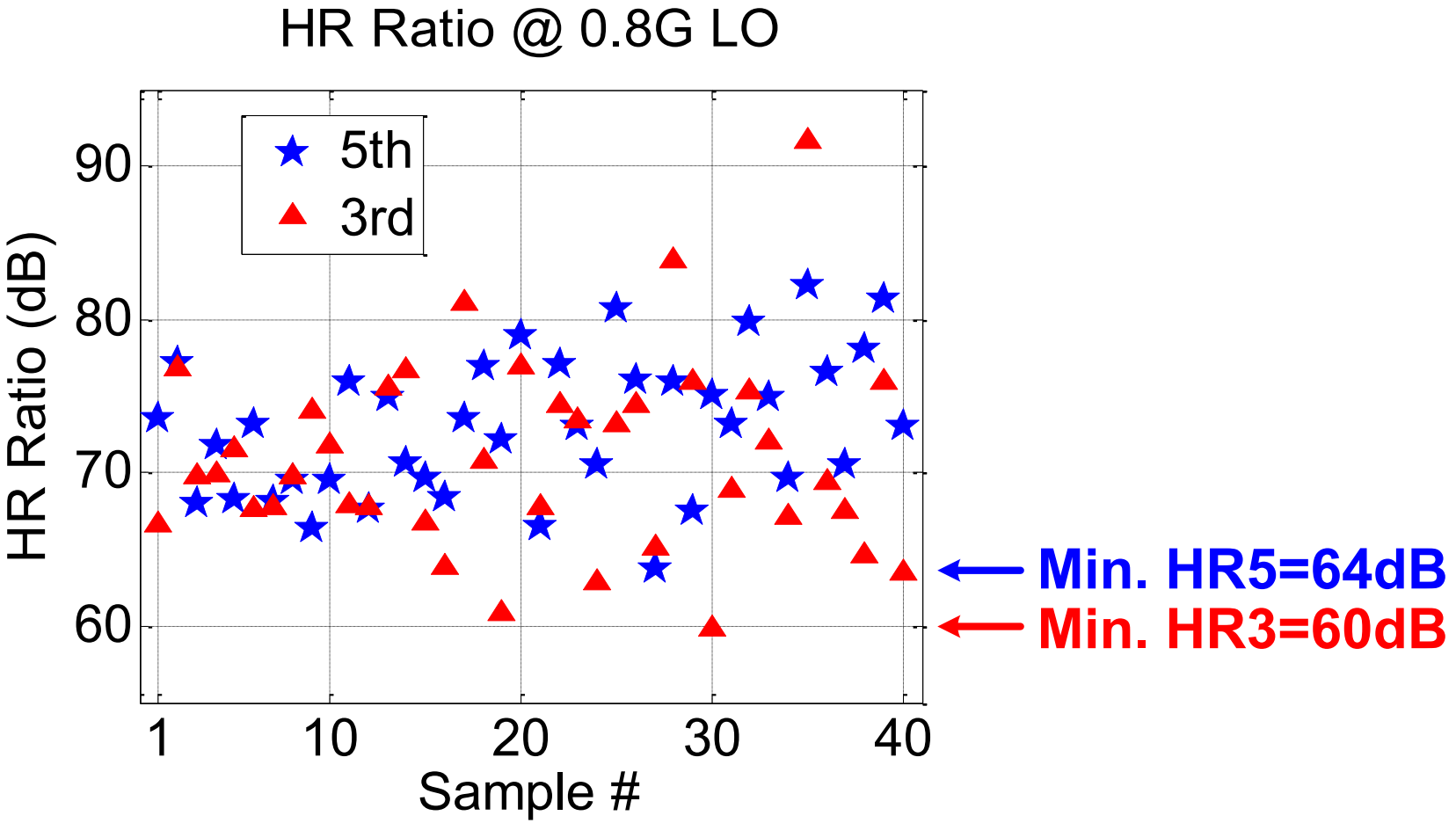


Chip Photo



- $1mm^2$ in 65nm CMOS
- VDD: 1.2V
- Current consumption:
  - Analog 33mA
  - Digital 17mA

Measured HR: 40 Chips



- **No trimming & calibration, no RF filtering**

Measured Performance Summary

LO Frequency	0.4~0.9GHz
Gain	34.4±0.2dB
DSB NF	4dB±0.5dB
S_{11} < -10dB	80M~5.5GHz
In/Out-of-band IIP3[1]	**+3dBm / +18dBm**
In/Out-of-band IIP2[2]	+46dBm / +51dBm
IF Bandwidth	12MHz
1/*f* noise	**30kHz** corner

VDD	1.2V
Current Consumption	Analog: 33mA
	Digital (clock): 8mA @ 0.4GHz 17mA @ 0.9GHz

Harmonic Rejection Ratio @ 0.8GHz LO	
3rd-order	**> 60dB (40 chips)**
5th-order	**> 64dB (40 chips)**
2nd, 4th, 6th	**> 62dB (20 chips)**

[1] Out-of-band IIP3: two tones = 1.61G & 2.40GHz, LO = 819MHz

[2] Out-of-band IIP2: two tones = 1.80G & 2.40GHz, LO = 601MHz

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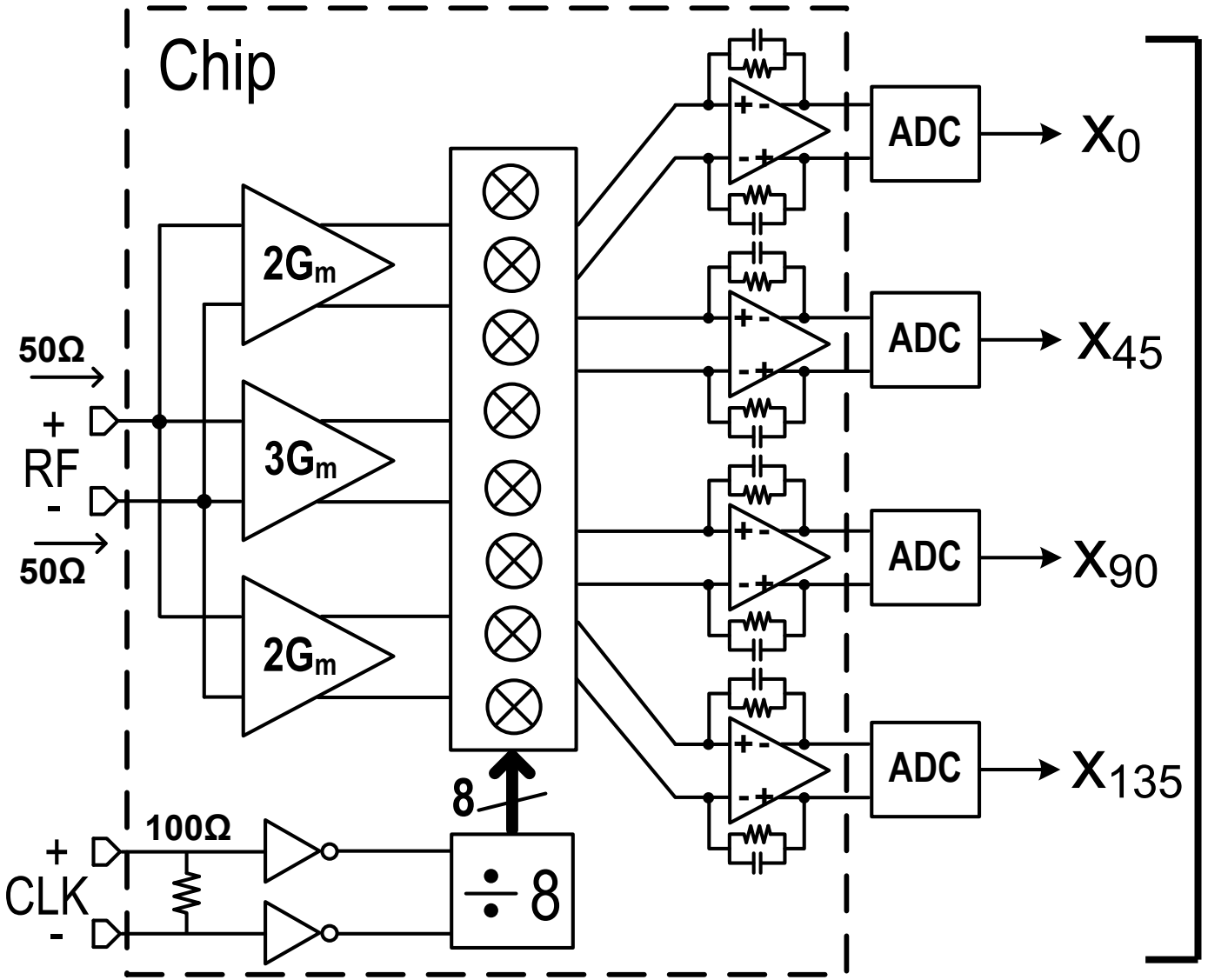
The Digital approach:

Harmonic Rejection Exploiting Adaptive Interference Cancellation

[Moseley, ISSCC 2009]

Harmonic Rejection RX: This work



To Digital Harmonic Rejection Algorithm

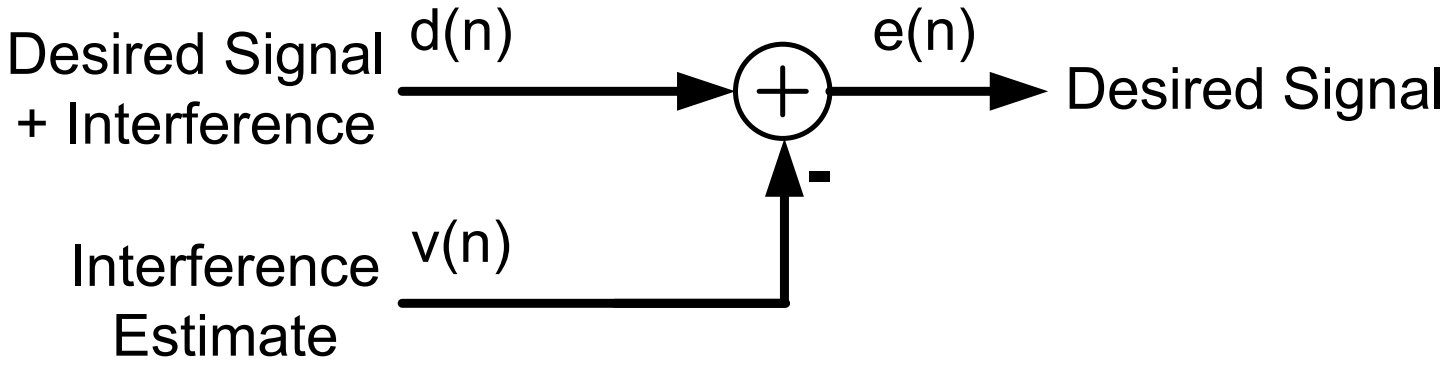
(Baseband processor)

The Basic Idea

Subtract interference

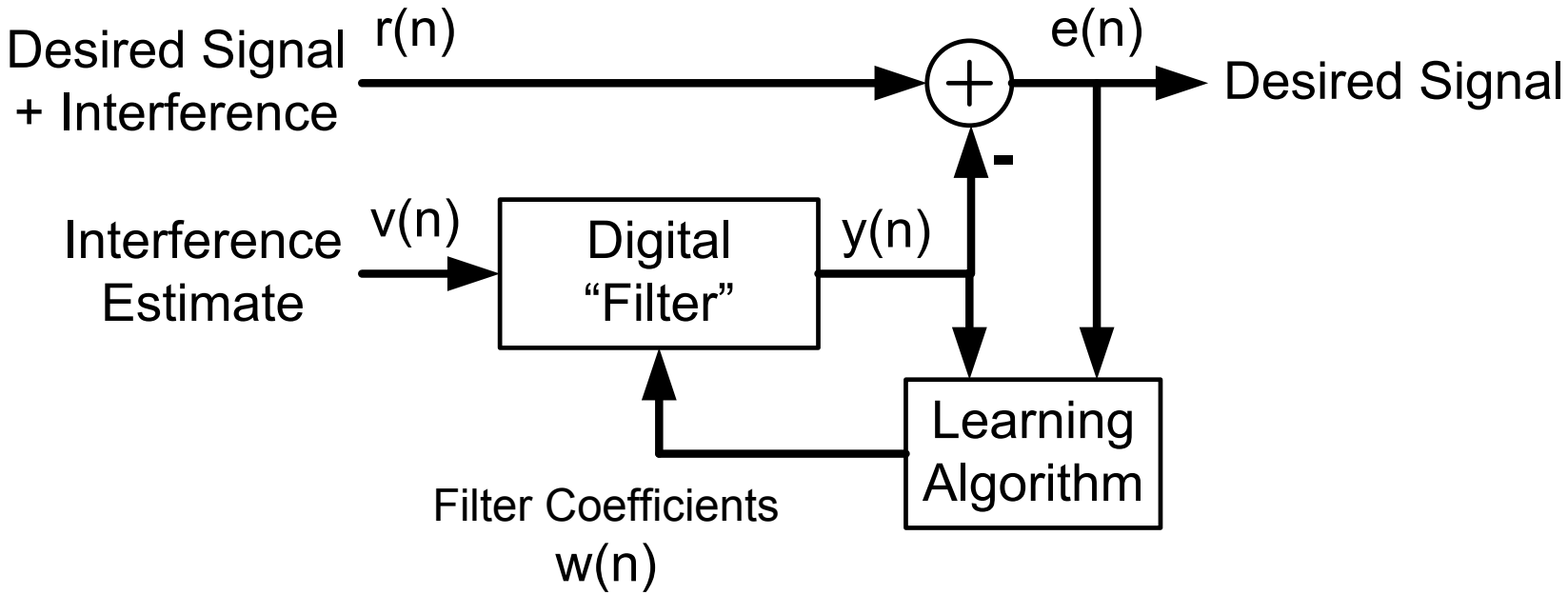
(residual harmonic image responses)

from received signal.



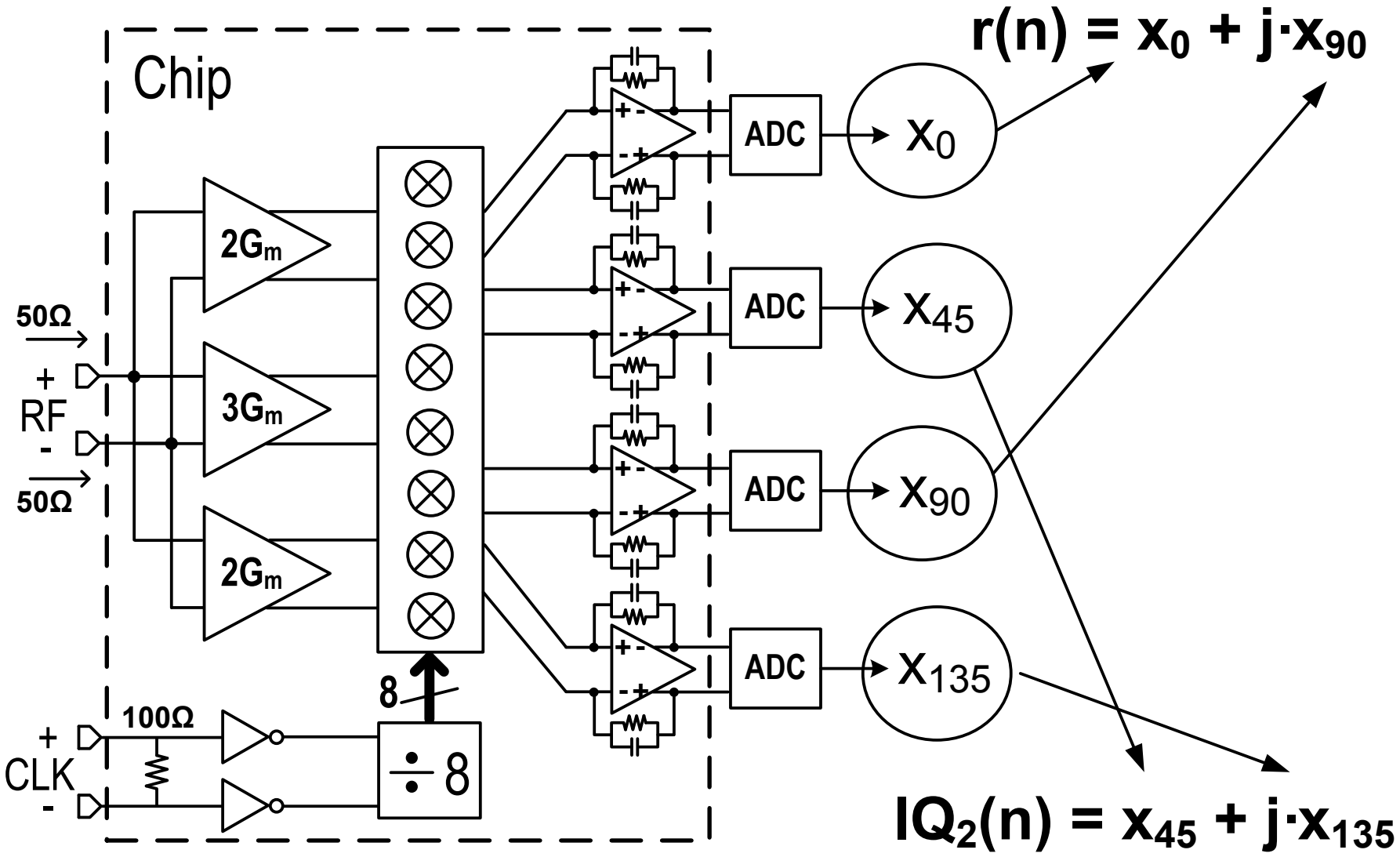
- **Need *interference estimate signal*.**

Adaptive Interference Cancelling (AIC)

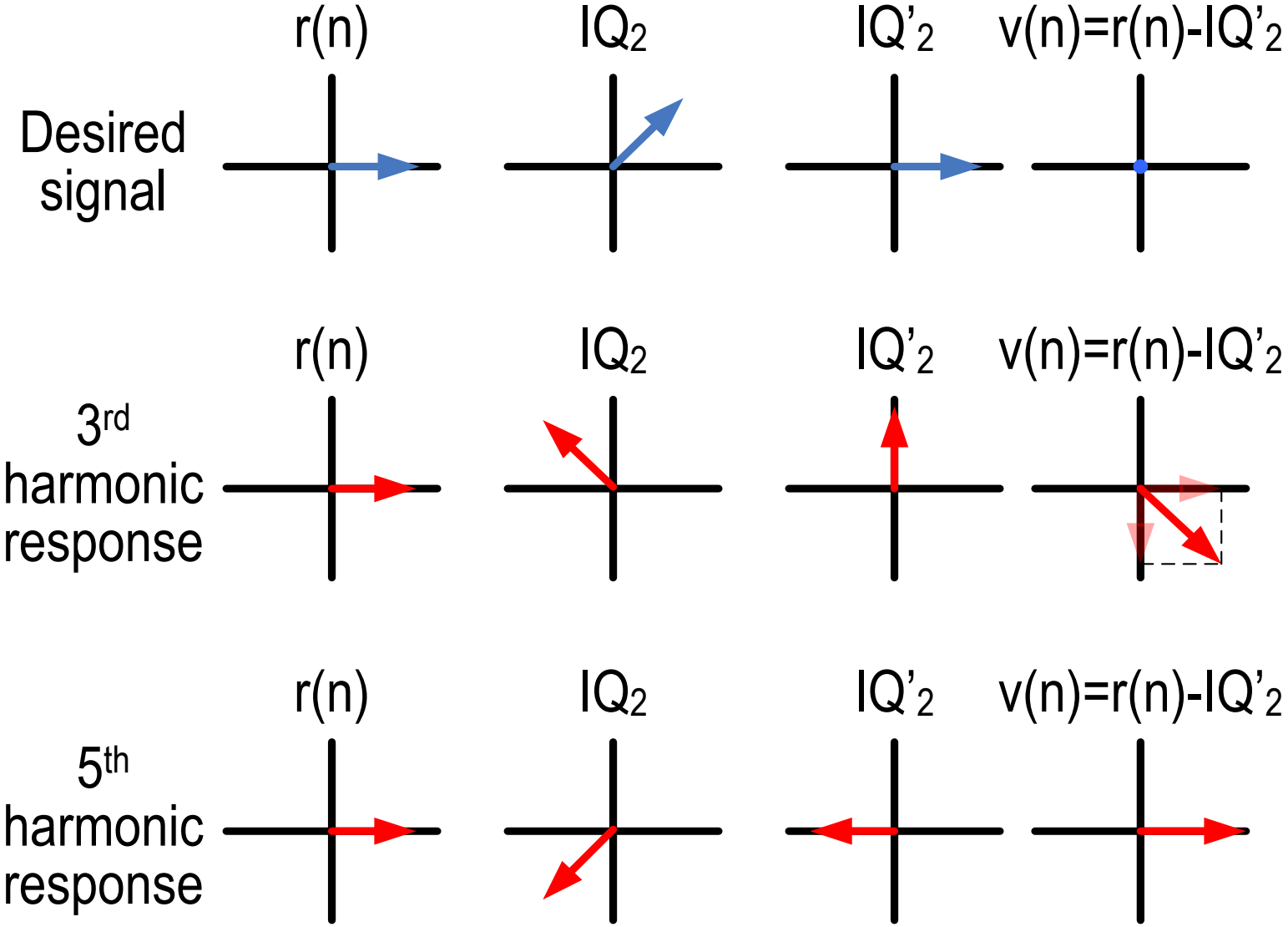


- Adaptive "filter" aligns phase & amplitude.
- Minimizes cross-correlation v(n) and e(n).

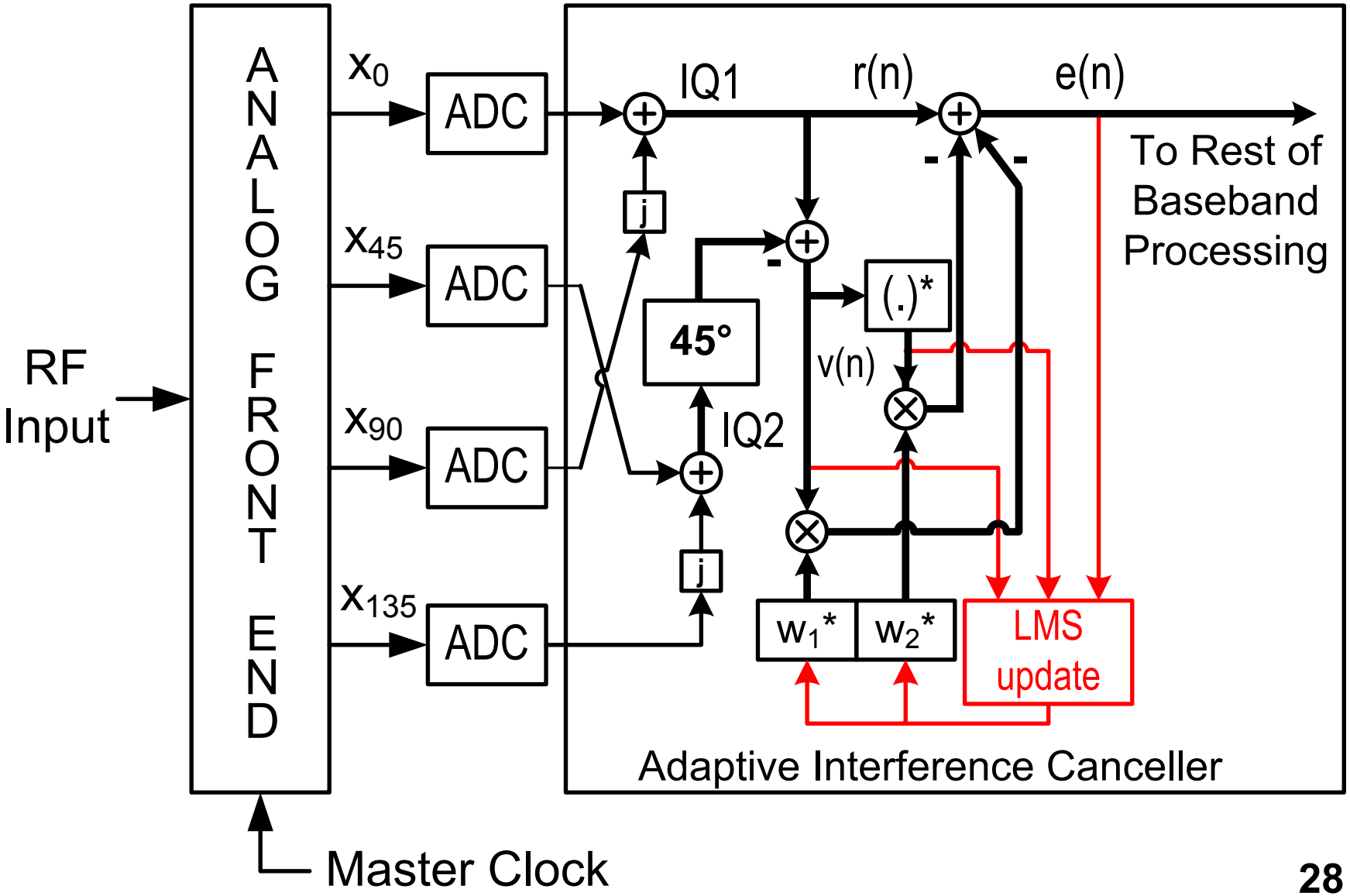
Two I/Q signals



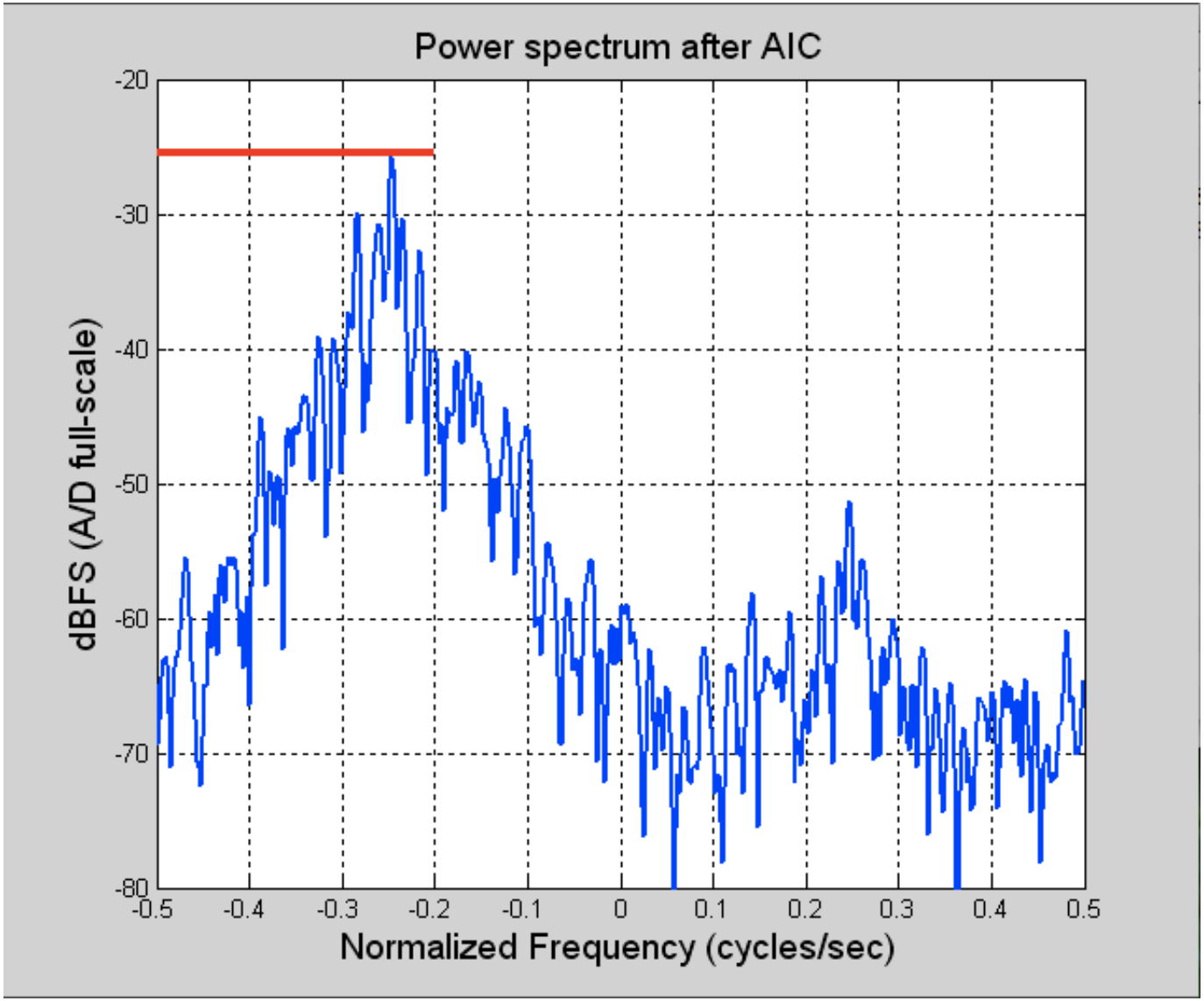
Interference estimate



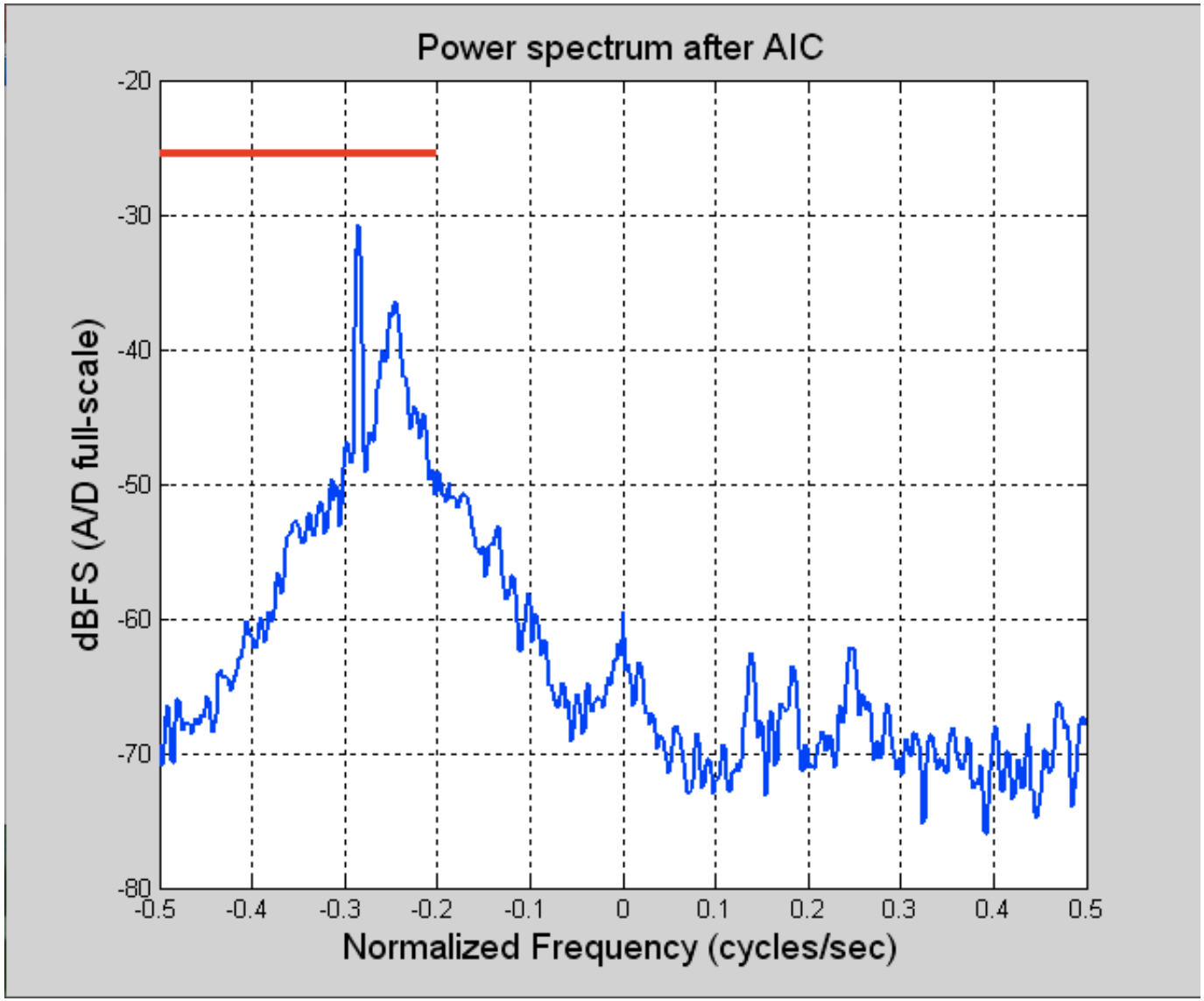
AIC Algorithm 5/5



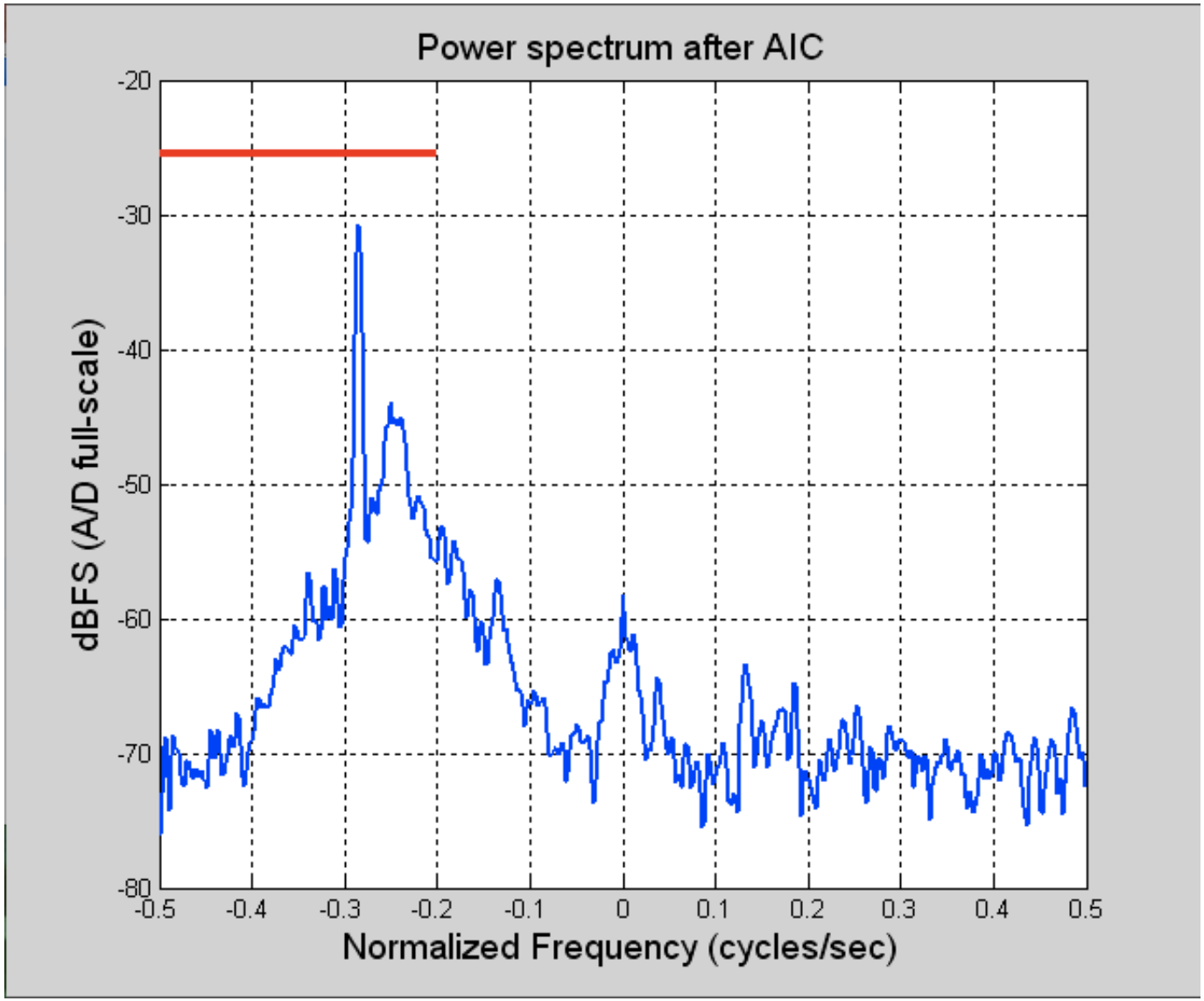
Demonstration



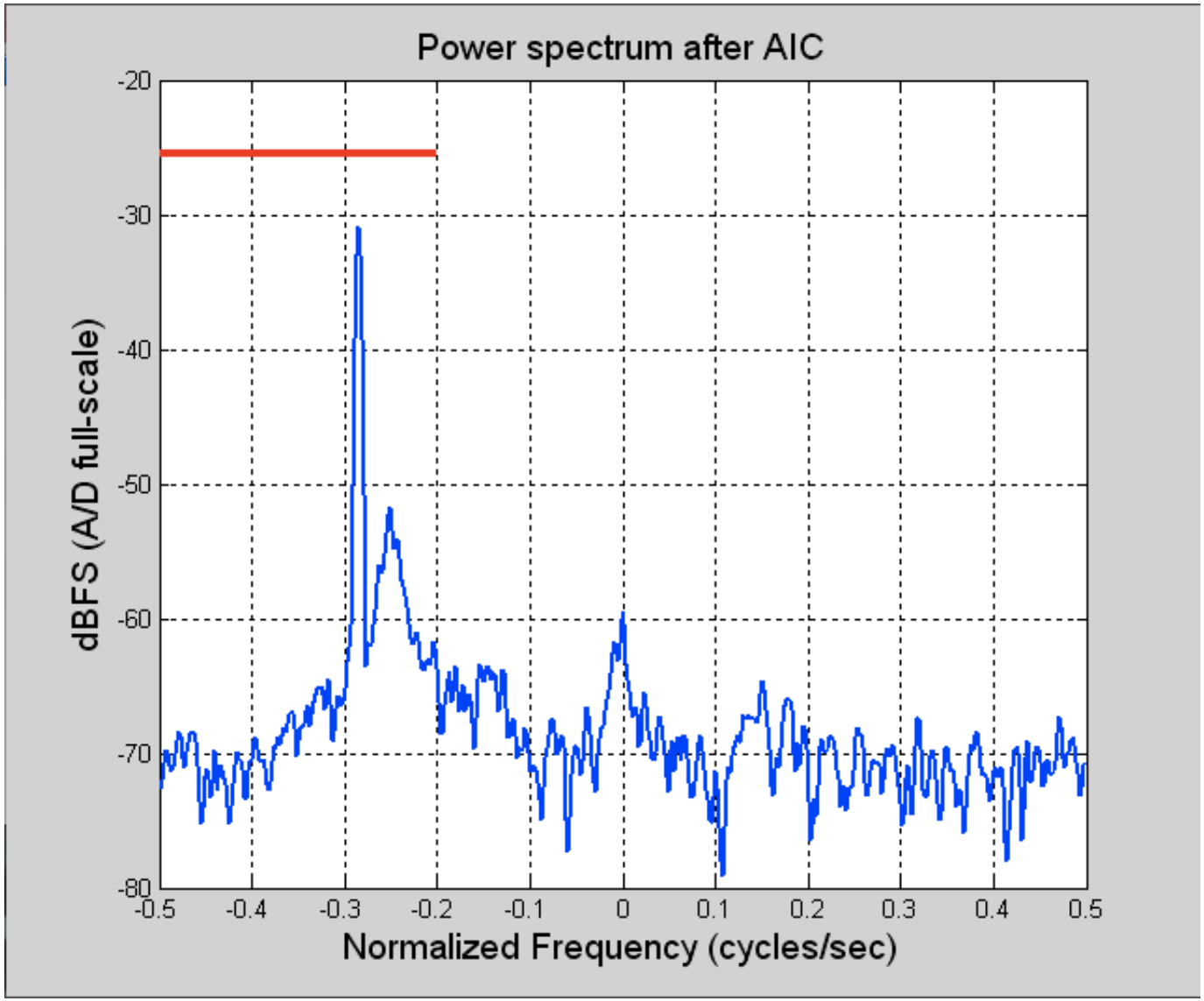
Demonstration



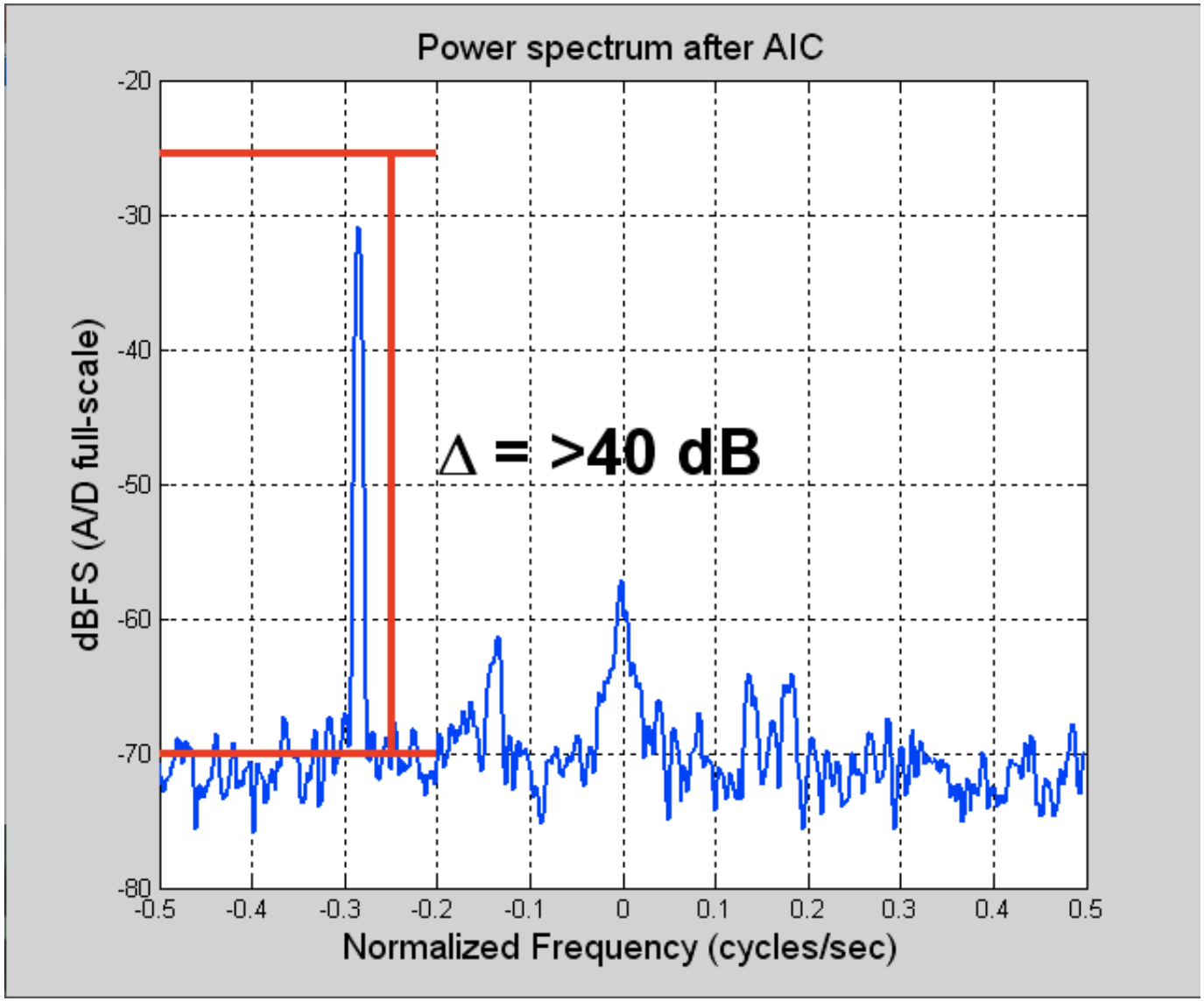
Demonstration



Demonstration



Demonstration



Comparison

	This work	Z. Ru ISSCC 2009 12.8
Rej. strongest	**>80 dB** (1)	>60 dB
Rej. other odd	>36 dB	>60 dB
Rej. even	>64 dB	>62 dB
Power frontend	45 mA @ 1.2 V (excl. ADCs)	50 mA @ 1.2 V (excl. ADCs)
Power DSP (100 Msps)	<8.5 mA @ 1.2 V (simulated)	N/A
# ADCs	4 / 2 if AIC off	2

(1) If one harmonic interference image band is dominating.

Outline

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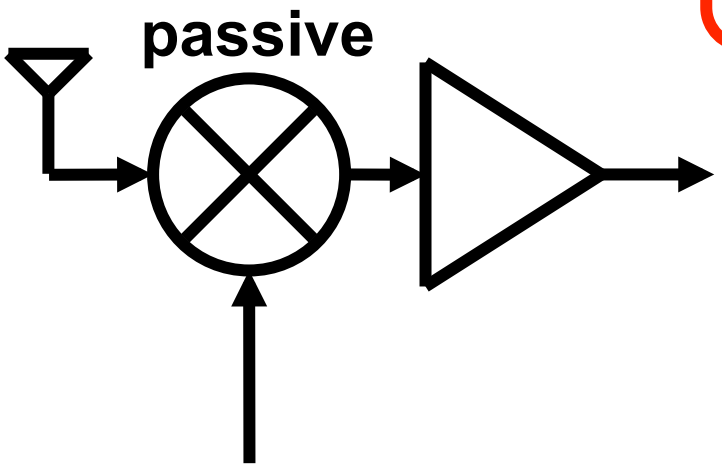
Mixer-first receiver:

A 0.2-to-2.0GHz 65nm CMOS Receiver Without LNA Achieving >11dBm IIP3 and <6.5dB NF

[Soer, ISSCC2009]

Proposed Architecture



Use passive mixer:

- High linearity

✓

No voltage gain before mixer:

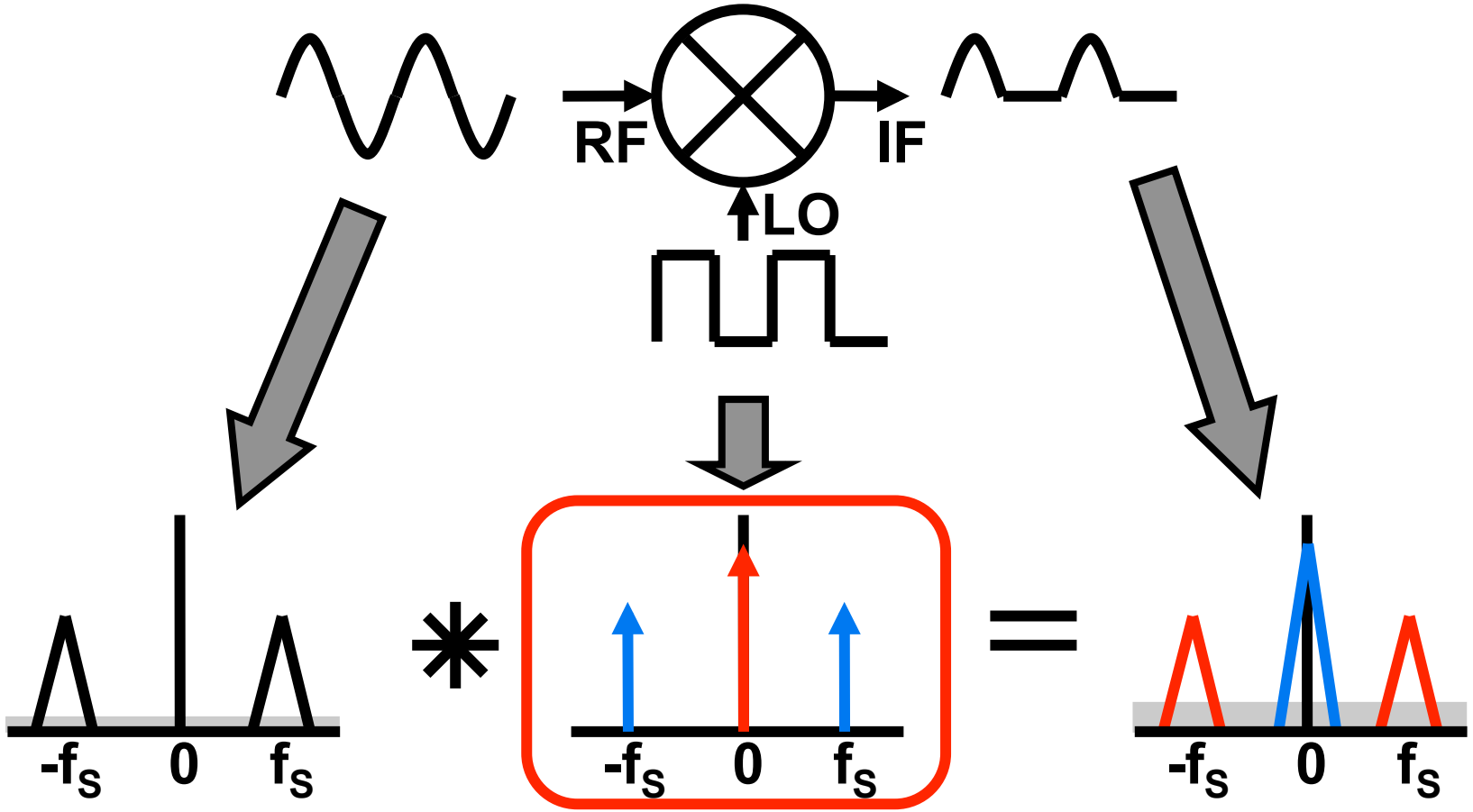
- Noise folding?
- Conversion loss?

Solve with:

- Harmonic cancellation
- Optimized mixer duty cycle

✓

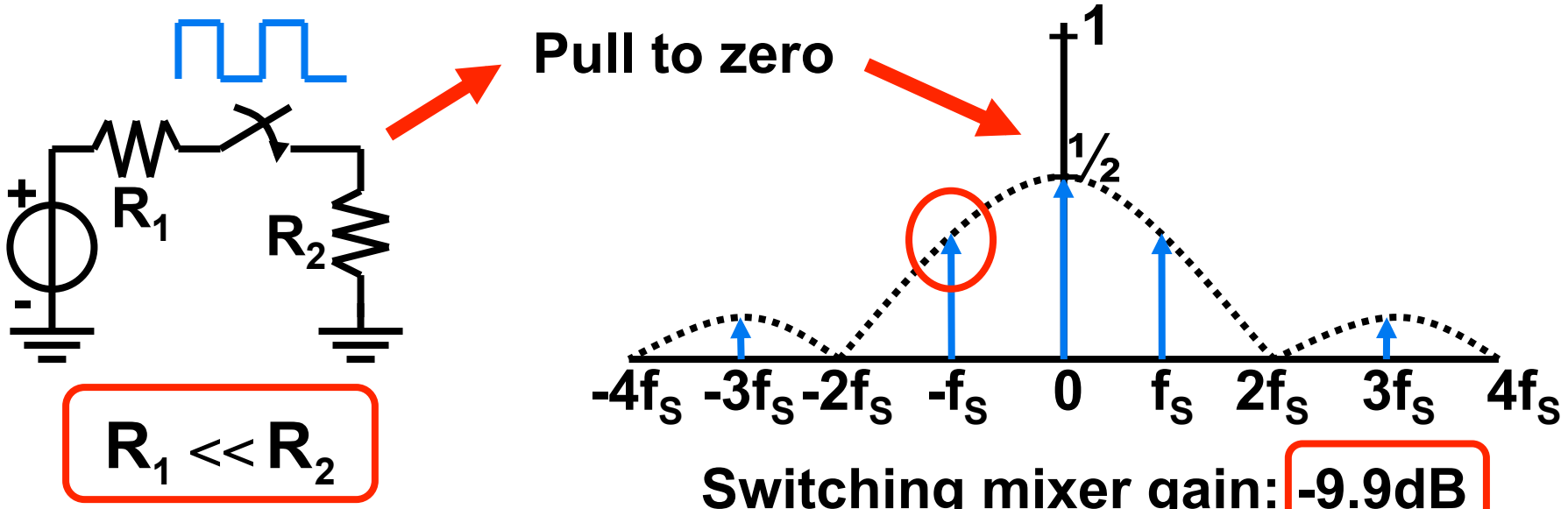
Mixer Operation

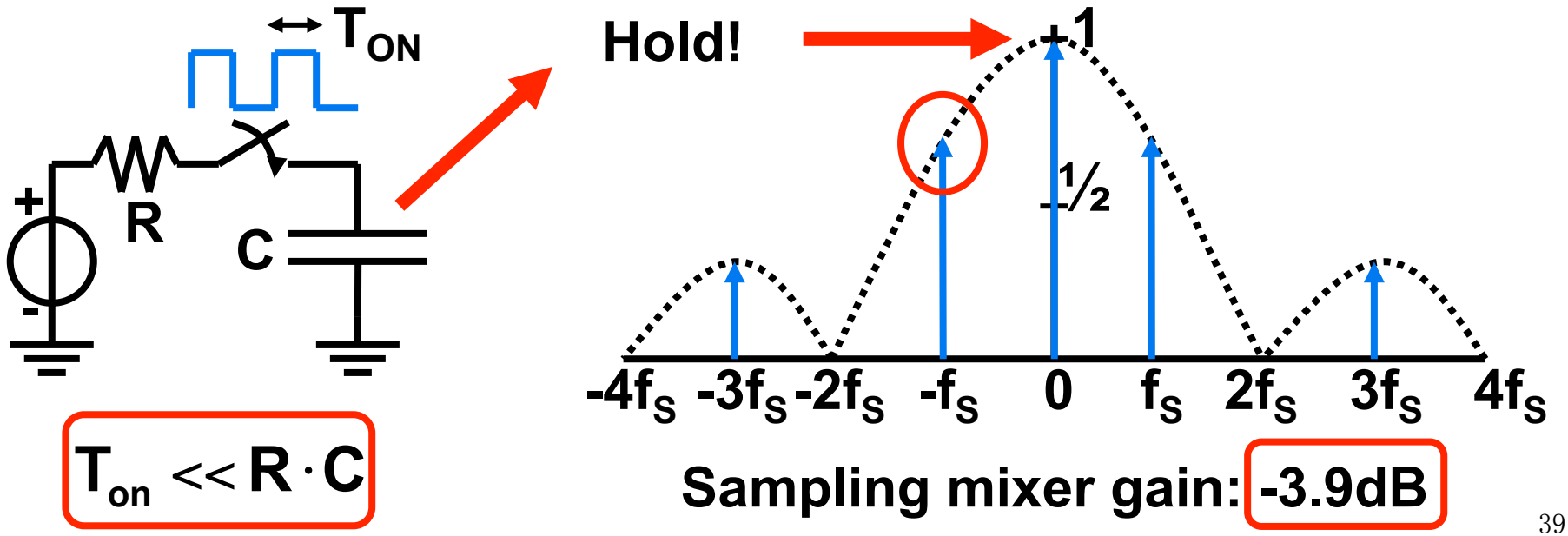


Linear Periodically Time Variant:

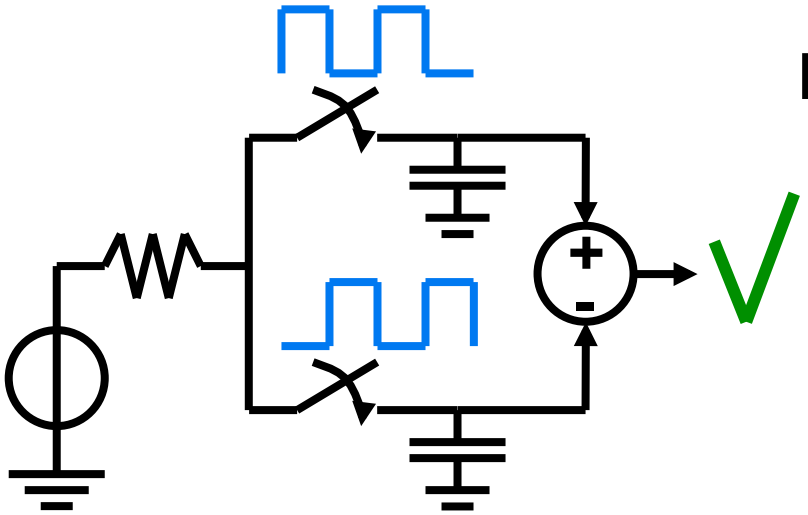
- **LO frequency f_S**
- **Convolution with harmonics (not all shown)**
- **Noise folding ⇨ increases NF**

Switching vs. Sampling Mixer



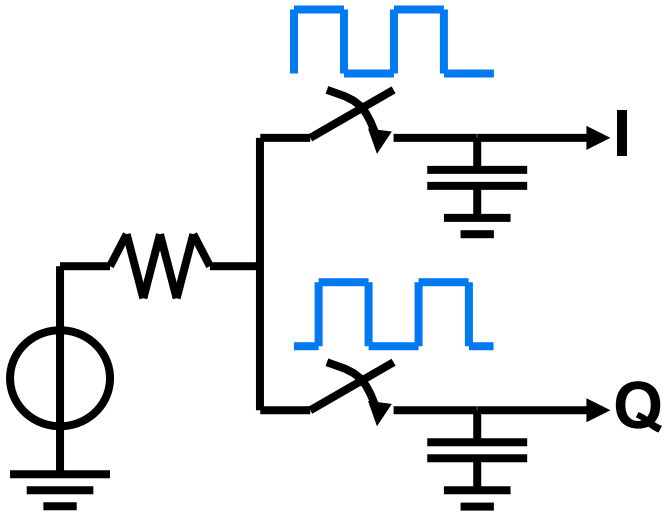


Multiphase



Balanced:

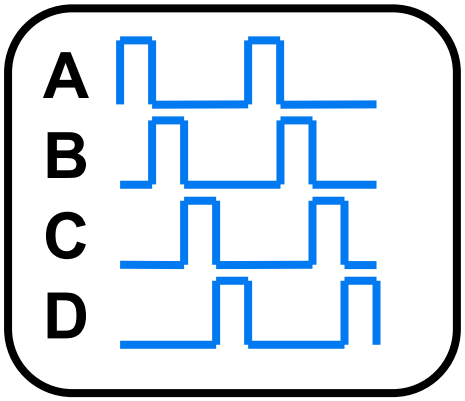
- 180° clock phase difference
- No feed-through
- Cancel even-order harmonics

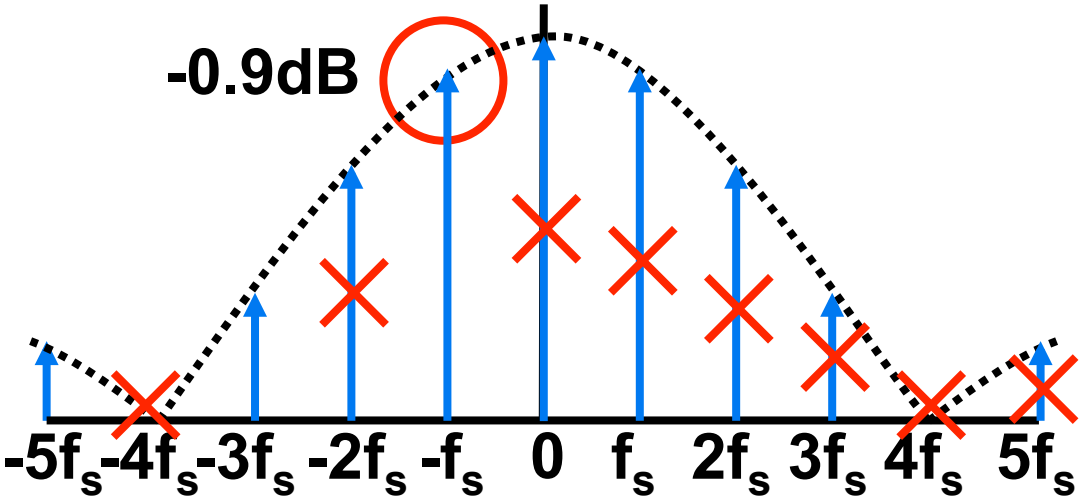


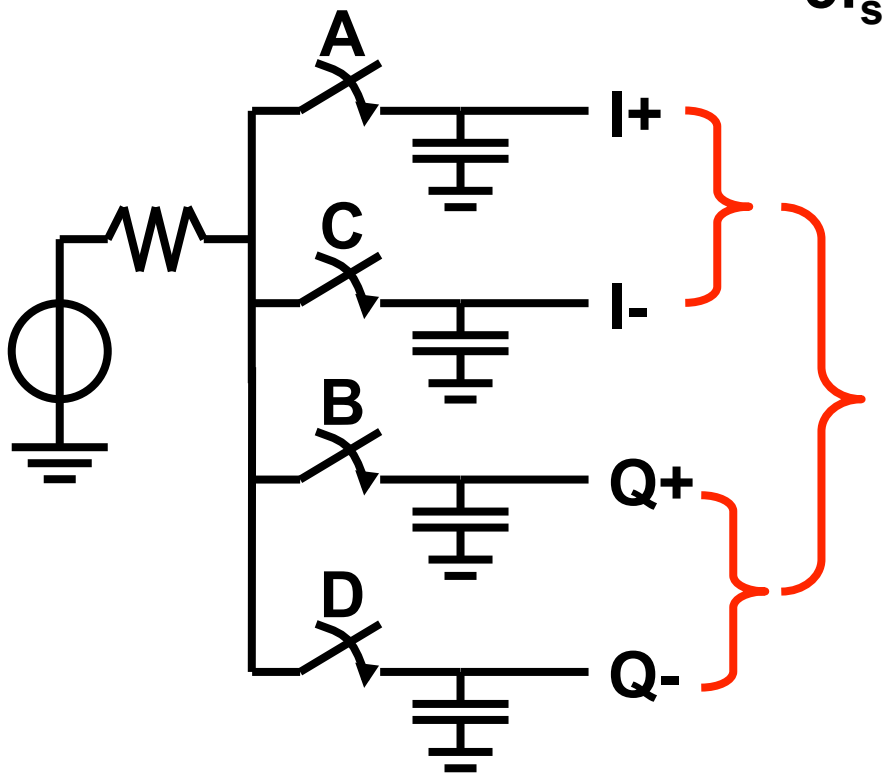
In-phase / Quadrature:

- 90° clock phase difference
- Image rejection?
- Clocks overlap!

25% Quadrature Sampling Mixer





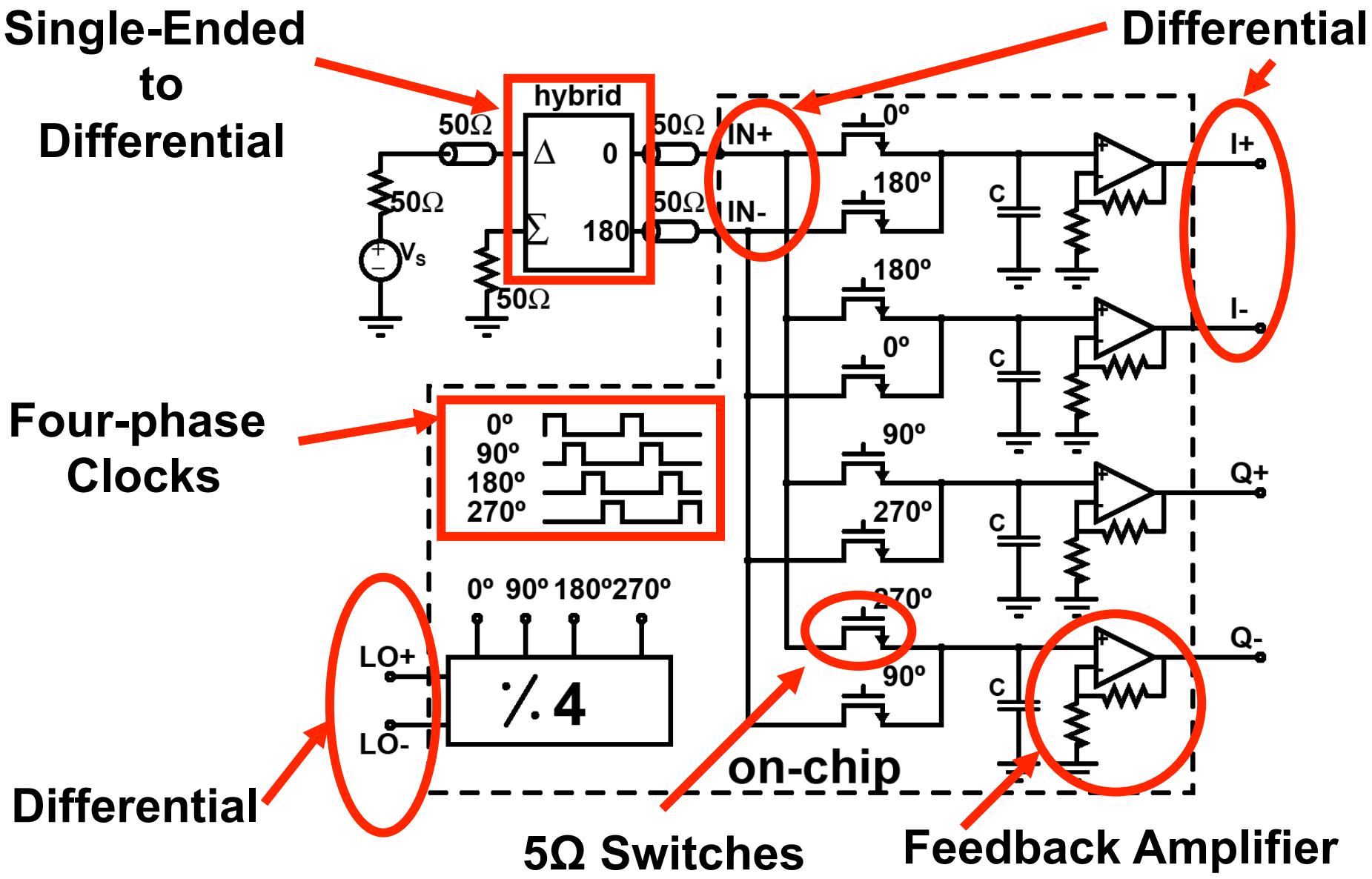


Balanced ✓

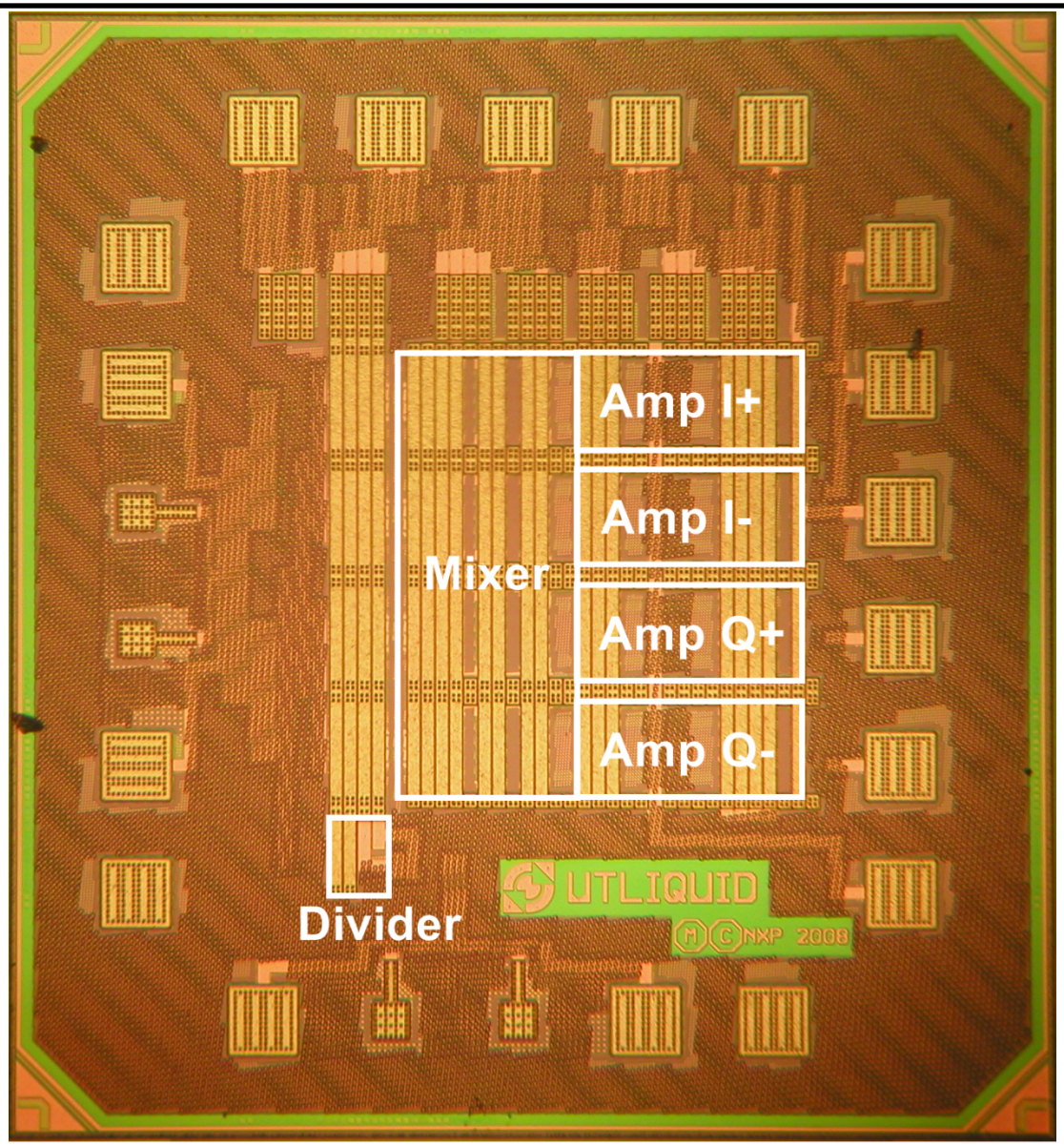
I/Q image rejection ✓

-0.9dB conversion gain
0.9dB NF

Total Design



Chip Micrograph



65nm CMOS, active area 0.13mm^2

Results & Benchmark

	This Work	[Bagheri, ISSCC 2006]	[van de Beek, ISSCC 2008]	Tektronix RSA2200A	
RF Frequency	0.2 - 2.0	0.8 - 6	0.6 - 10	0 - 3	GHz
IF -3dB Bandwidth	25	20	264	~10	MHz
Gain	19	20	14		dB
DSB NF	6.5	5	7	24	dB
IIP2	+65	+60	+20		dBm
IIP3	+11	-4	0	+30	dBm
SFDR in 1MHz BW	79	70	71	80	dB
Power Dissipation	67	60	90		mW
Supply Voltage	1.2	2.5	1.2		V
Active Area	< 0.13	3.8	< 0.2		mm^2
Technology	65nm	90nm	45nm		CMOS

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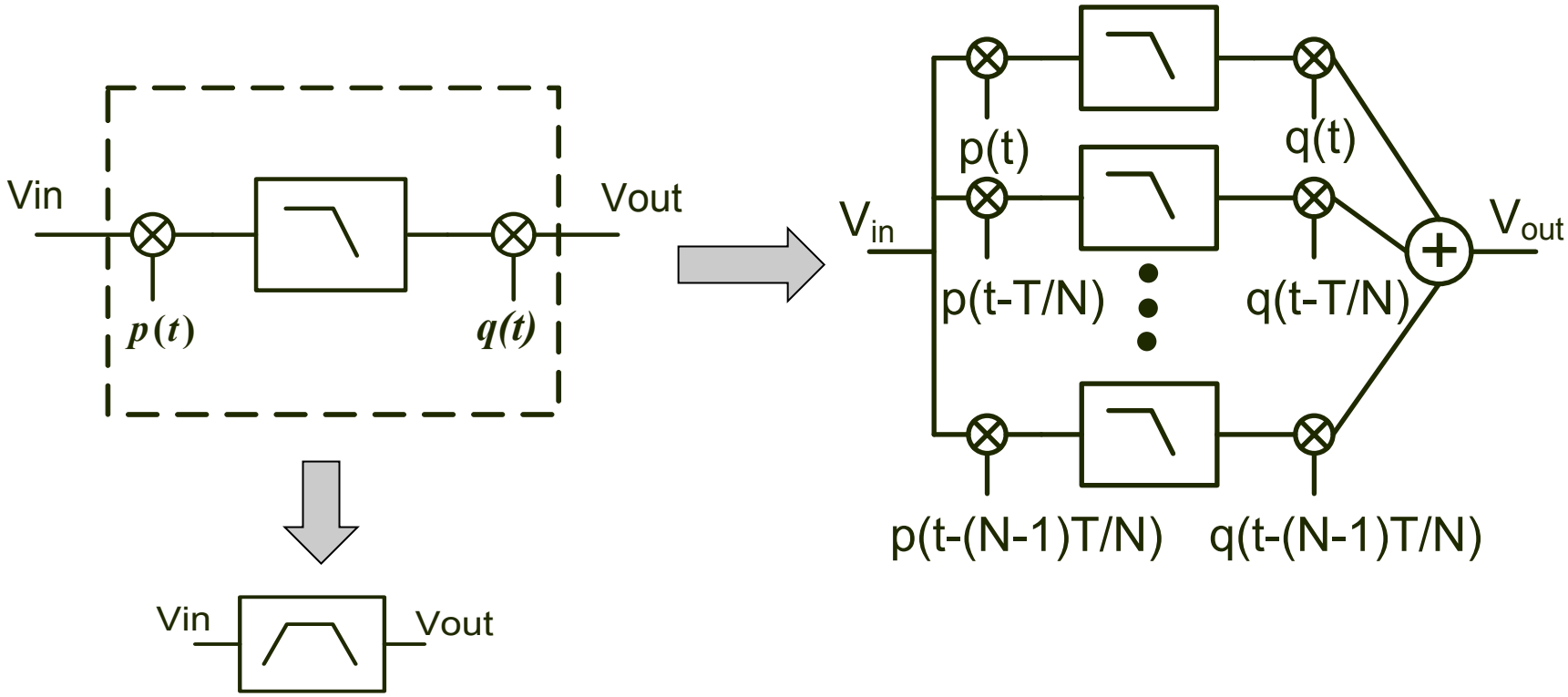
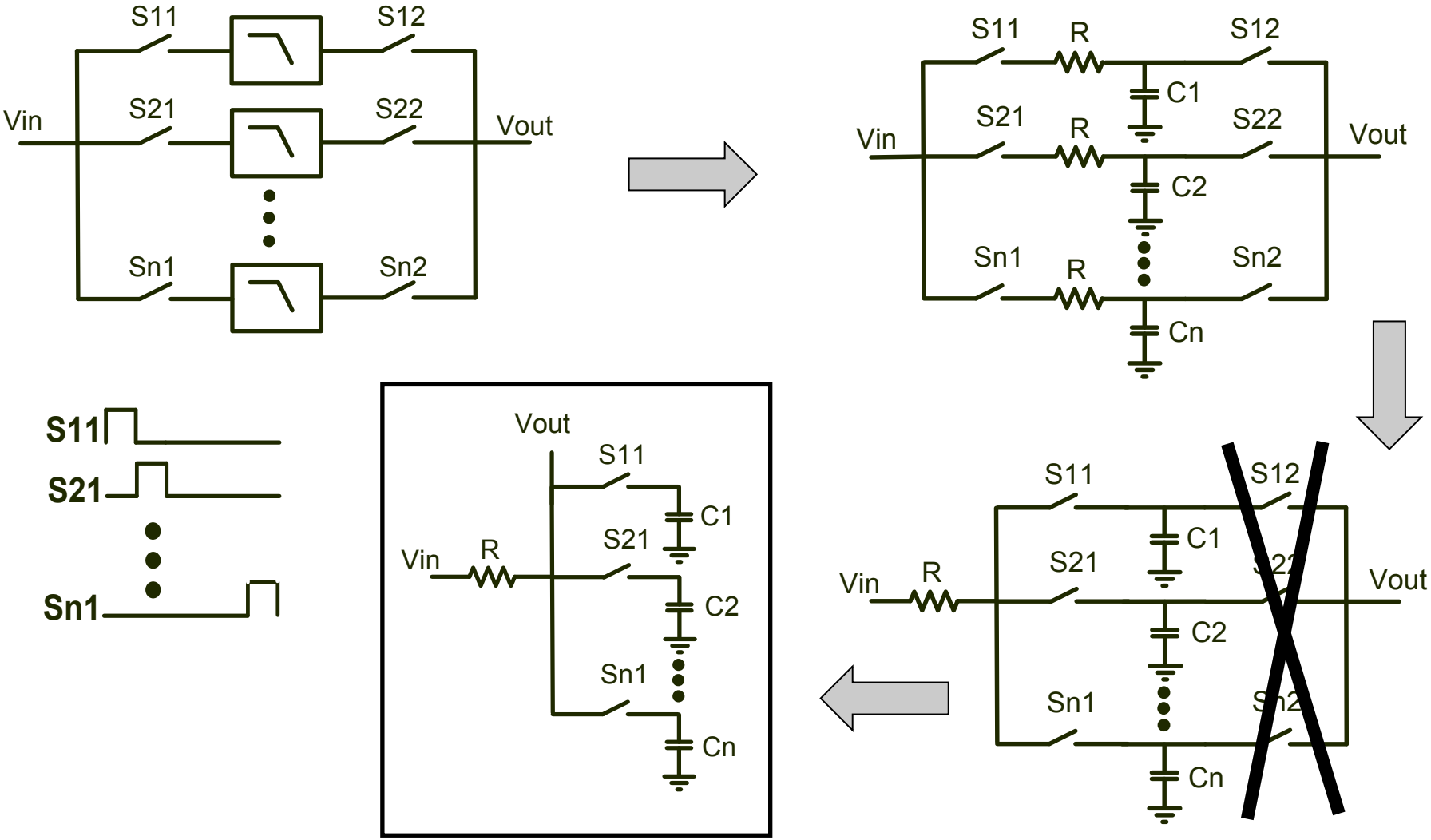
Idea from 1960: N-Path Filters

- Downconvert & LPF & Upconvert = BPF
- Square-wave clock, harmonic mix problem
  - Cancel using multiple paths!



[Franks, ISSCC1960]

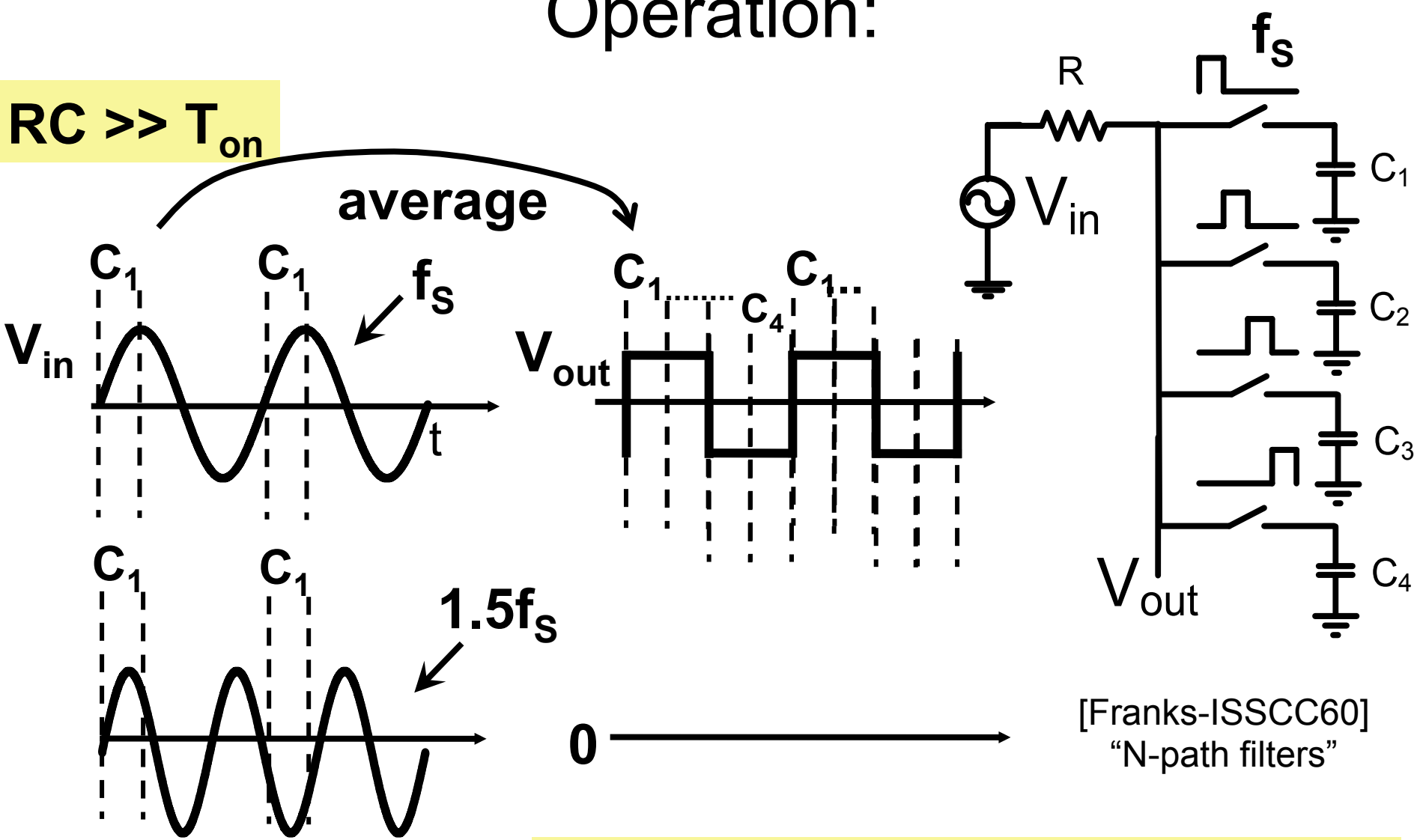
Simple Implementation



[Ghaffari, RFIC 2010 & JSSC May 2011]

Operation:

RC >> T_{on}

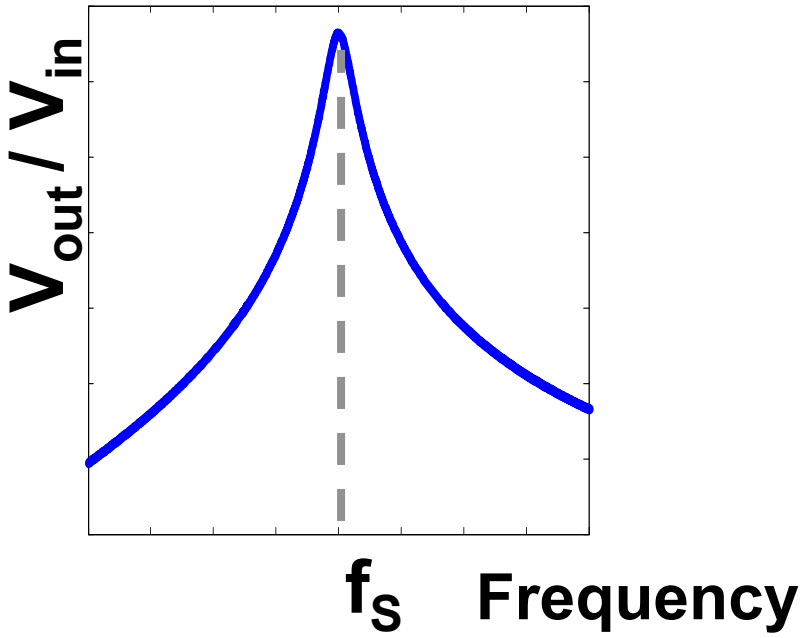


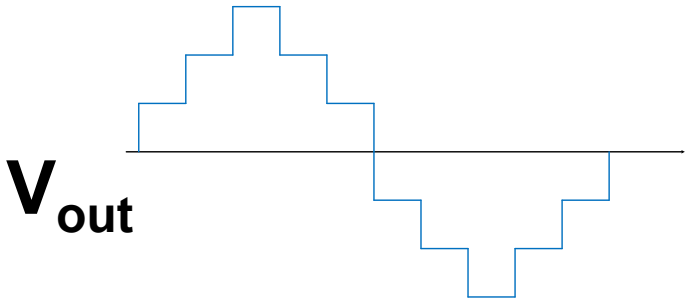
[Franks-ISSCC60]
"N-path filters"

- **High ohmic @ switching frequency**
- **Short circuit @ other frequencies**

Filter Properties

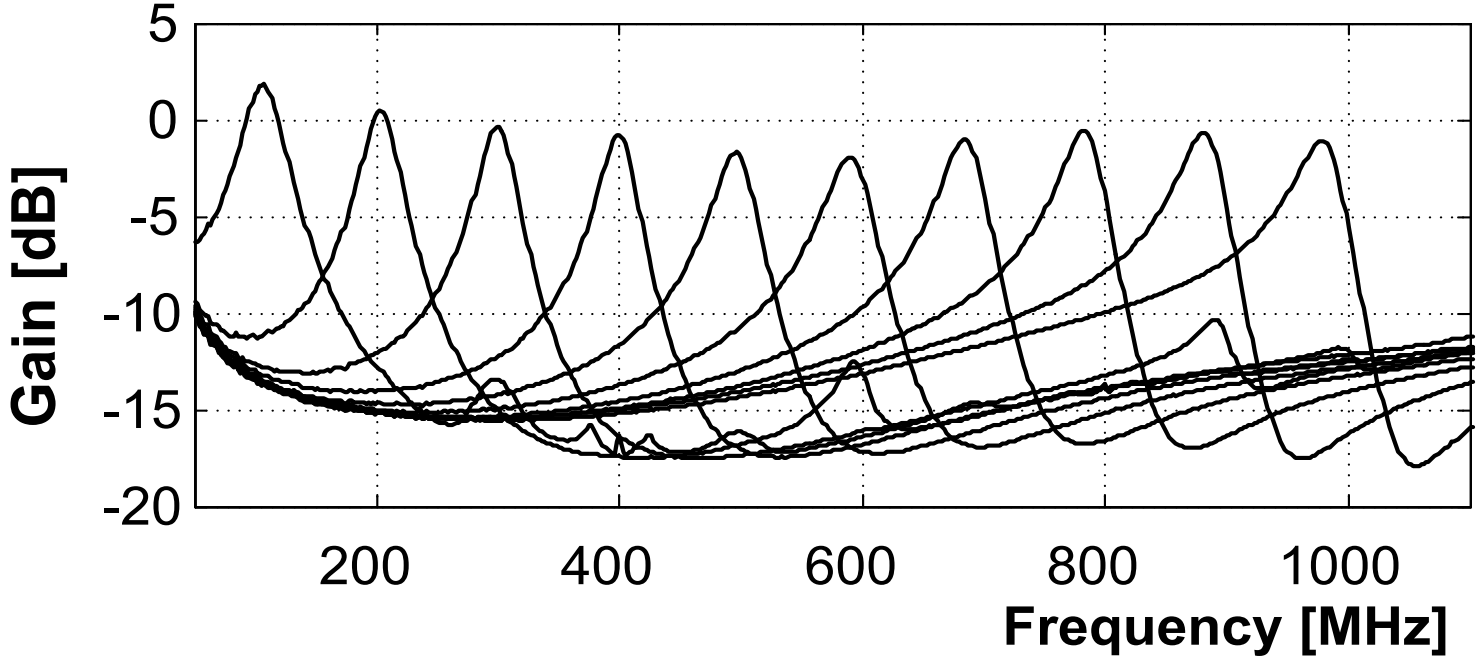
- Band-pass around f_s
- Tunable (clock f_s)
- High Q for high $RC \cdot f_s$
- Good linearity & noise
- Unwanted harmonics





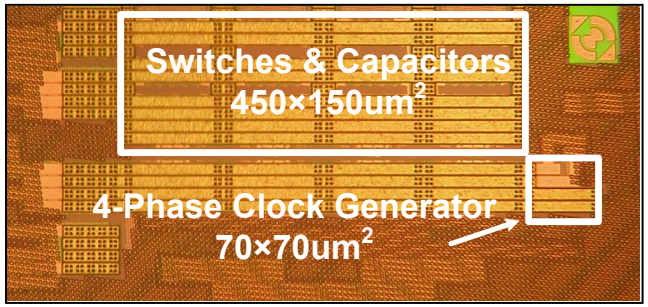
More paths ⇔ Less Distortion

Filter Properties: flexibly tunable



Selectivity (Q)	3 to 29
Compression (P_{1dB})	+2dBm
Linearity (IIP3)	+19dBm
Noise Figure	<5.5dB
Power	2-16 mW

65nm CMOS chip*



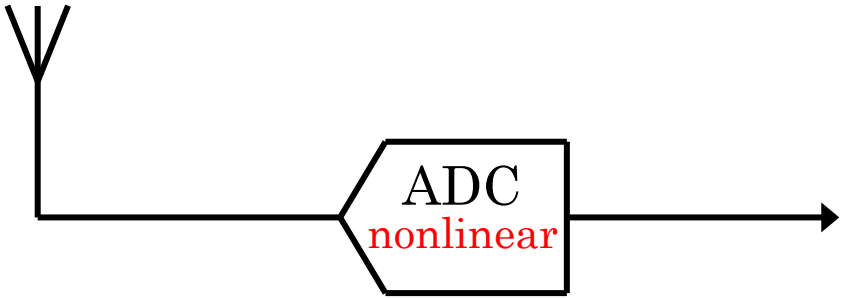
[Ghaffari,Klumperink,Nauta-RFIC10-JSSC5-2011]

Outline

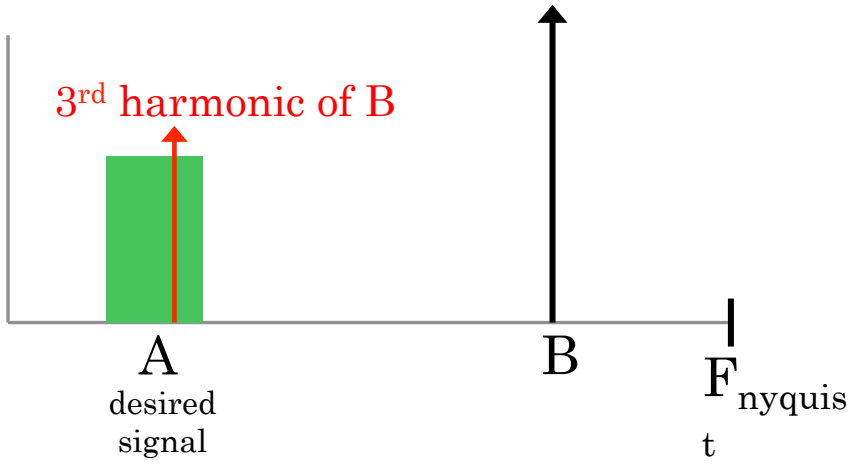
- Introduction
- Interferer robust SDR RX – analog part
- Interferer robust SDR RX – digital part
- Mixer-first RX
- N-path RF filter
- **Interferer scrambler for Software Radio**

Interferer scrambling for Software Radio

- Software defined radio
- Problem: linearity ADC

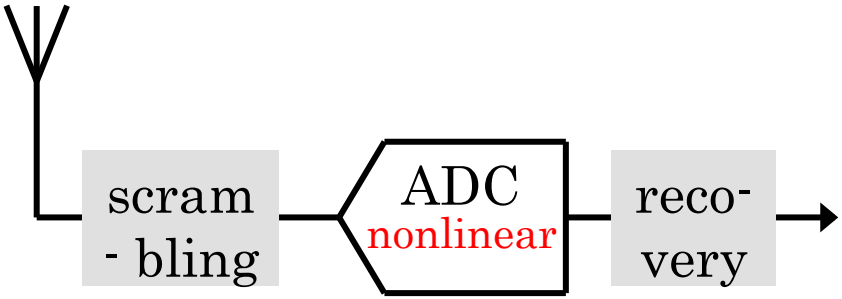


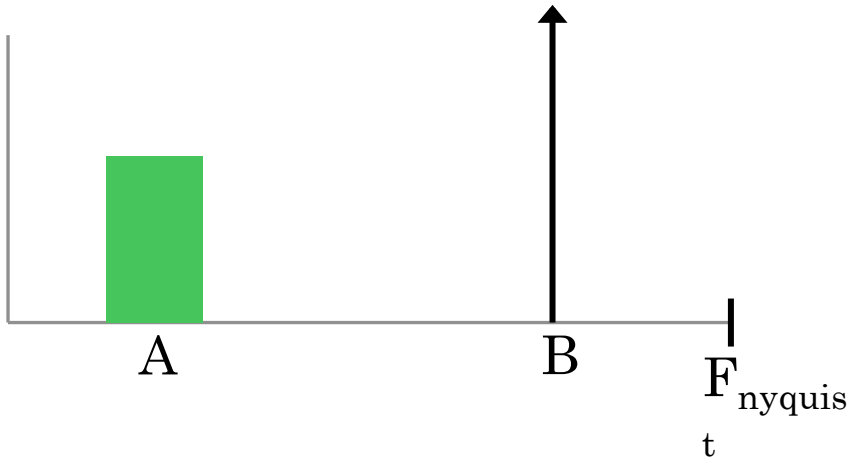
→ in-band harmonic: SNDR ↓



Introduction

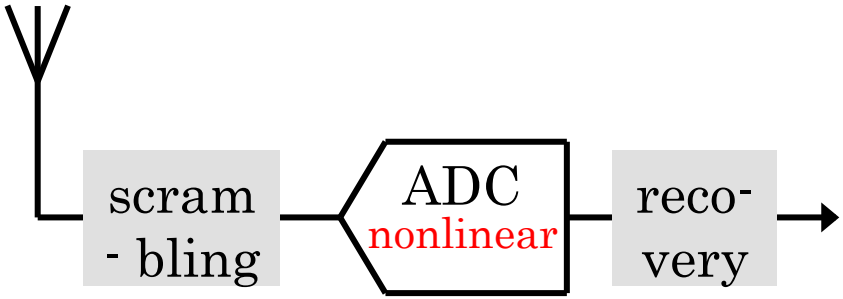
- proposed solution: scrambling

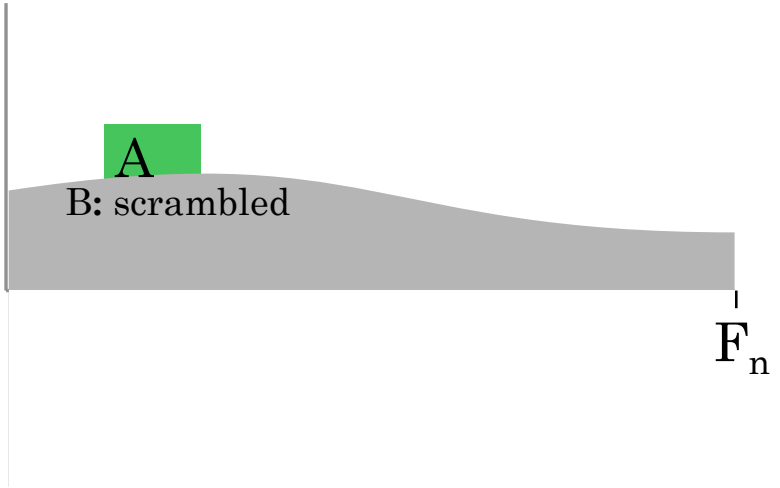




Scrambling Concept

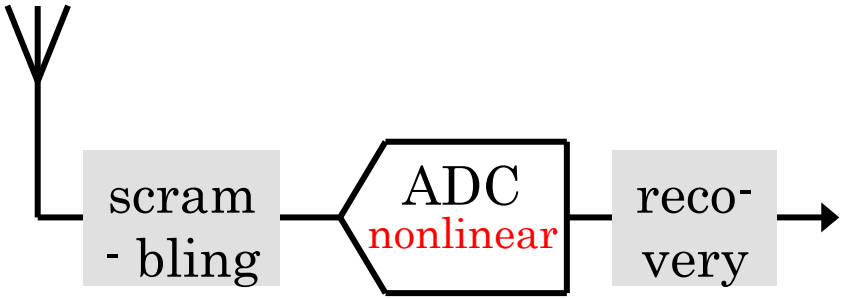
- proposed solution: scrambling

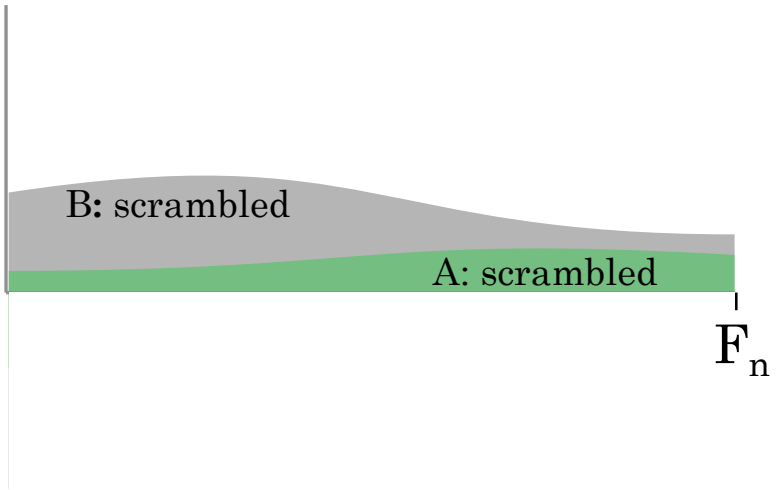




Scrambling Concept

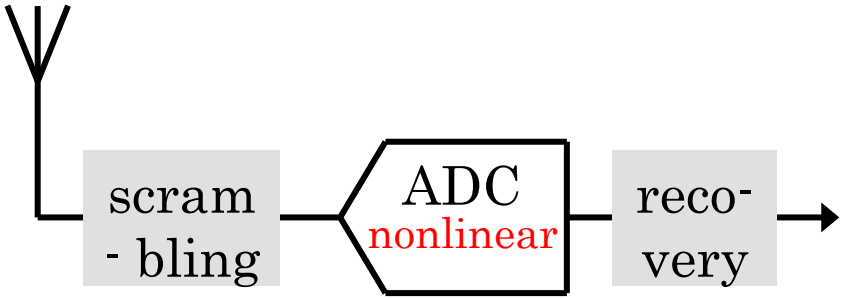
- proposed solution: scrambling

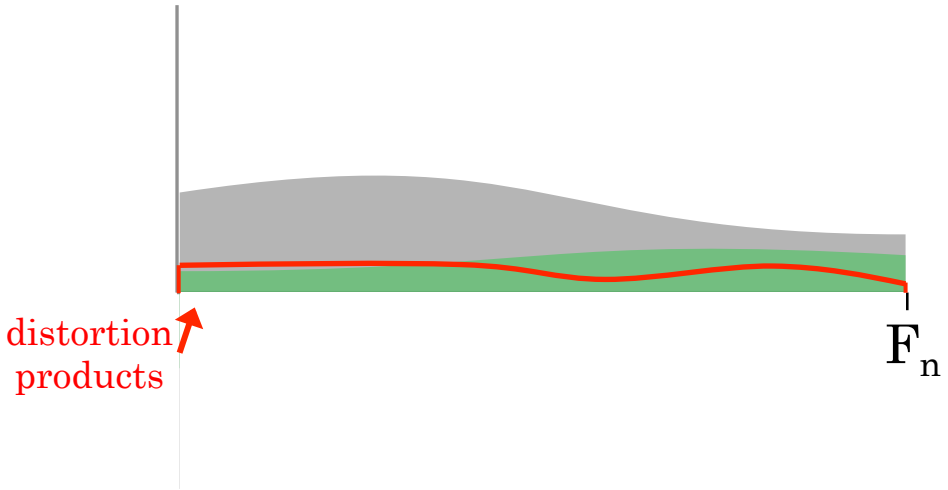




Scrambling Concept

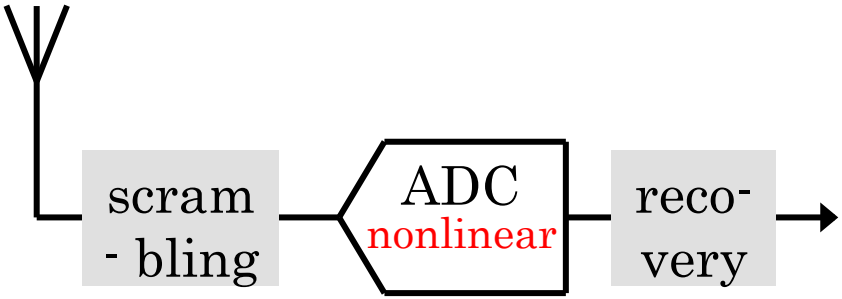
- proposed solution: scrambling



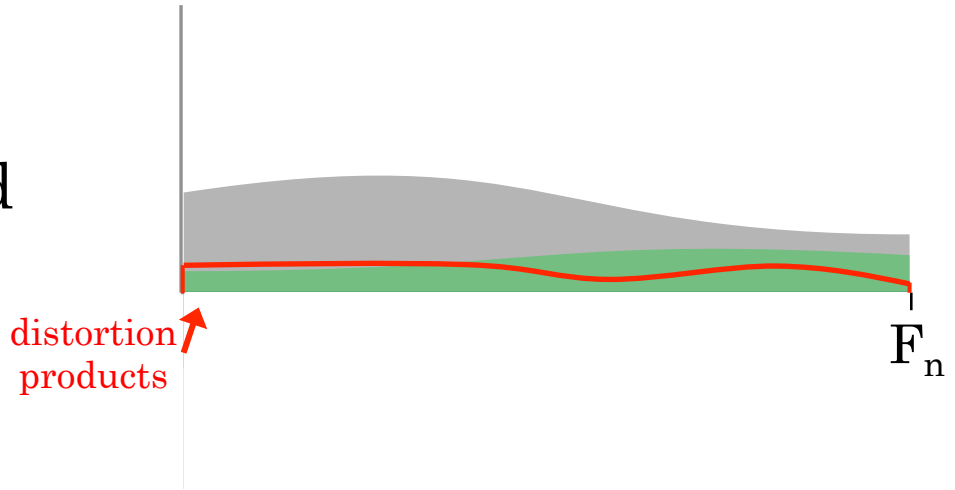


Scrambling Concept

- proposed solution: scrambling

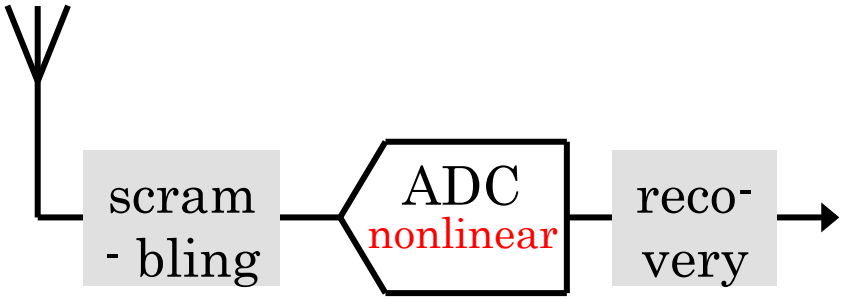


→distortion now wideband



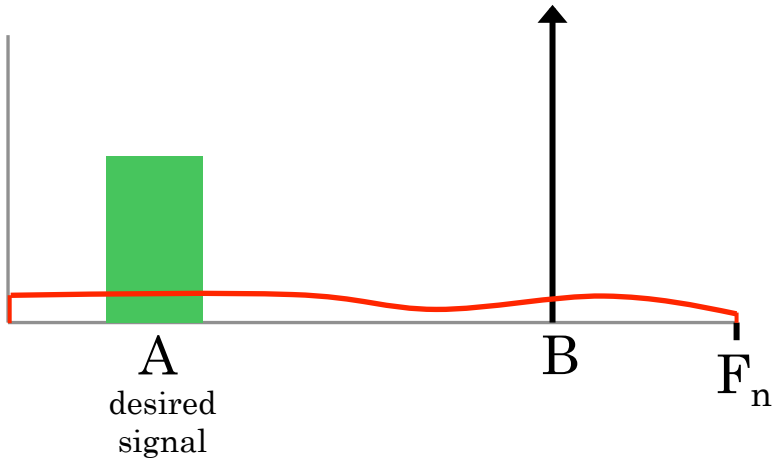
Scrambling Concept

- proposed solution: scrambling

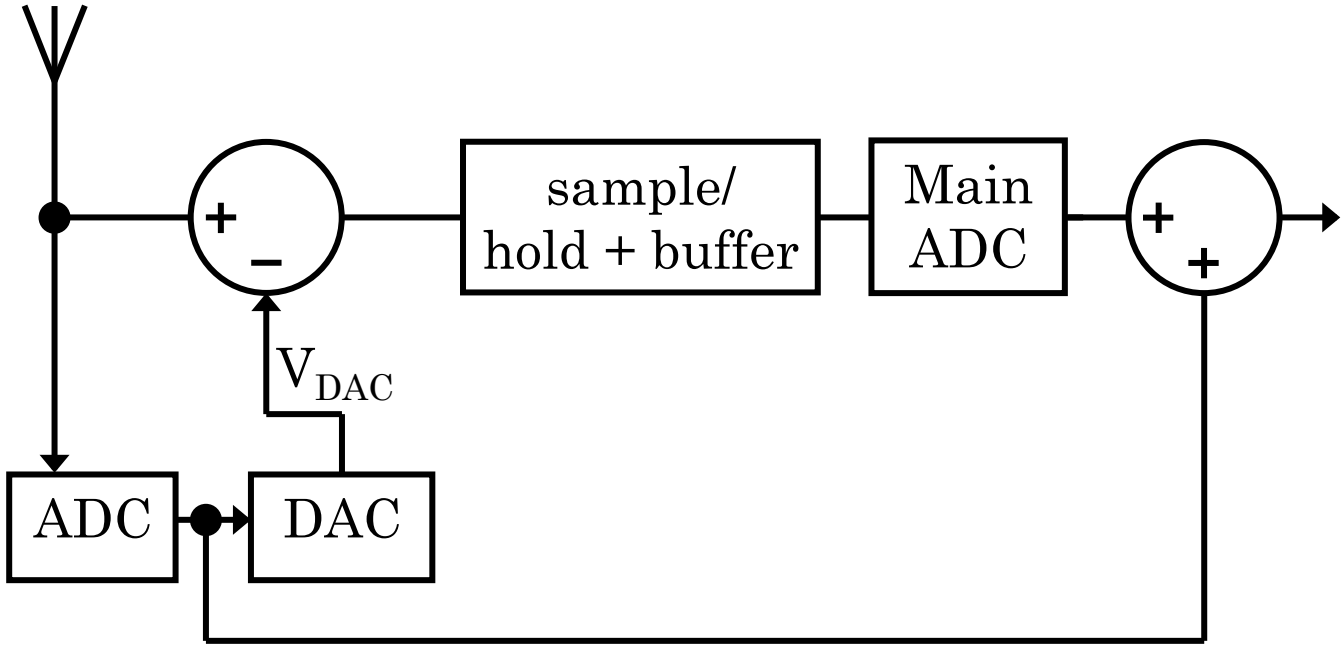


- After recovery

→ In-band SNDR improved



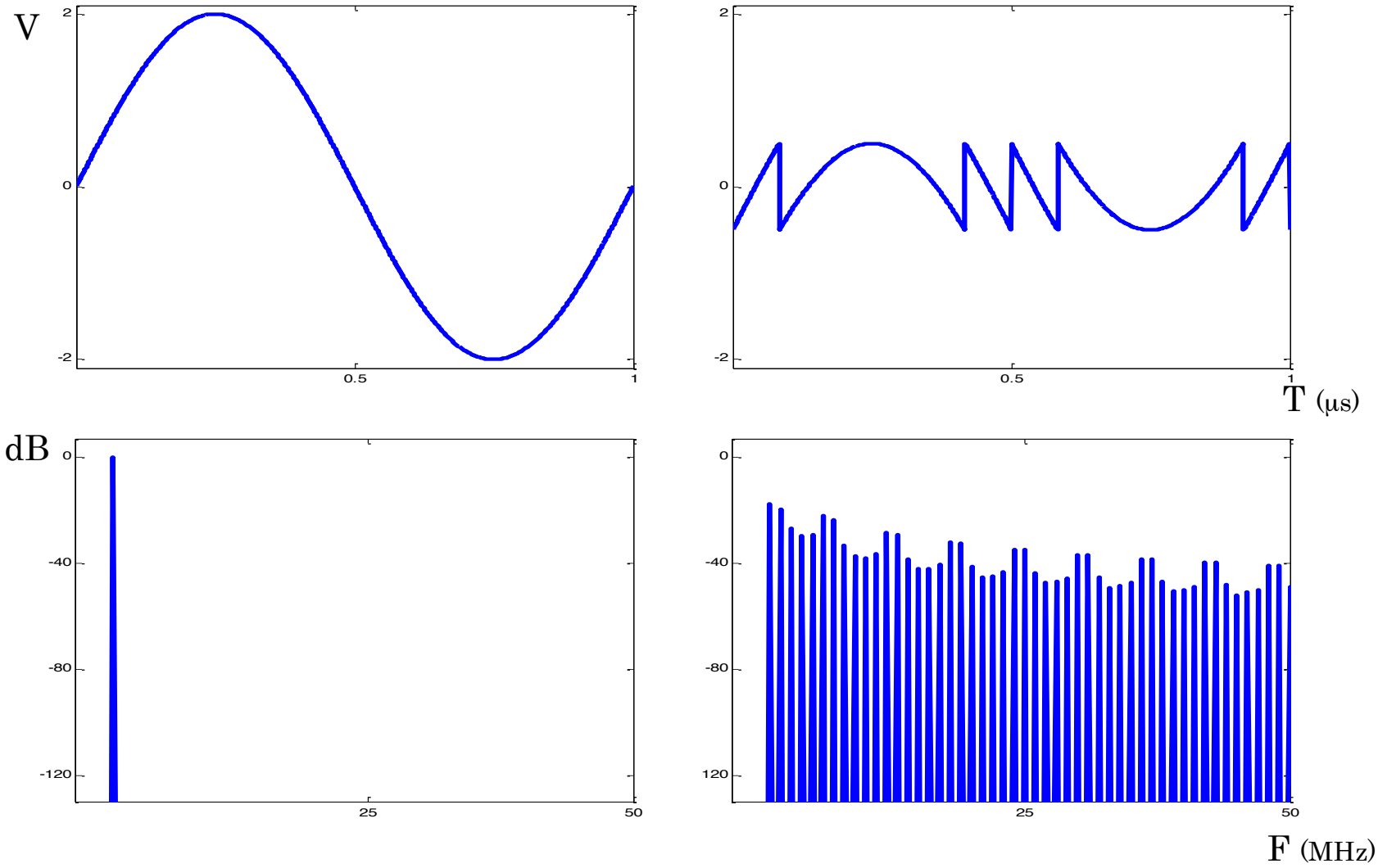
Scrambling Concept



- Challenges:
  - DAC performance
  - Subtractor performance
  - phase alignment
- Solutions presented at ESSCIRC 2011

Matlab example; 1 Gs/s main ADC, 1 MHz input sine

$$y(t) \approx x(t) + 0.01x^3(t)$$



Matlab example; 1 Gs/s main ADC, 1 MHz input sine

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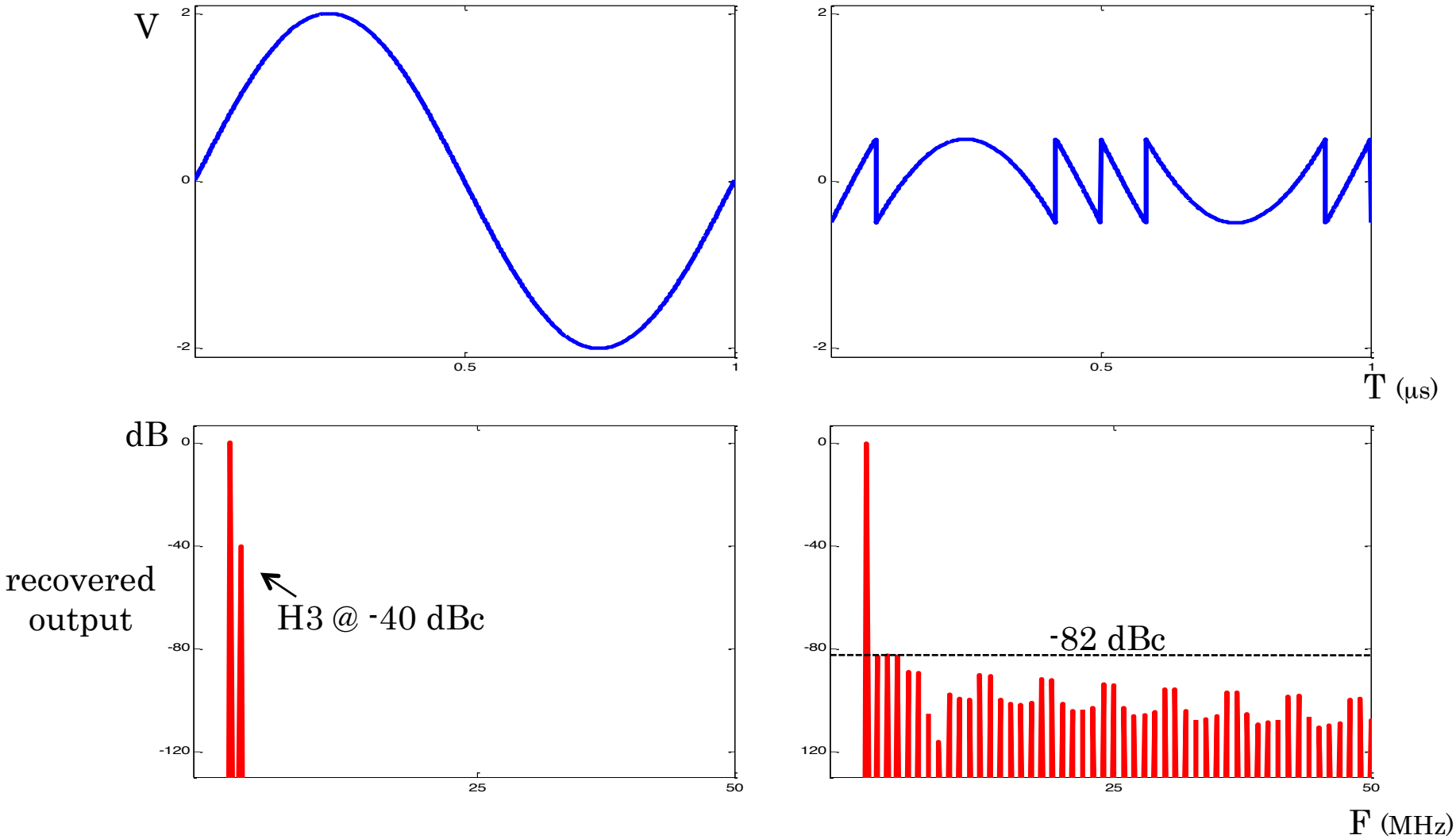
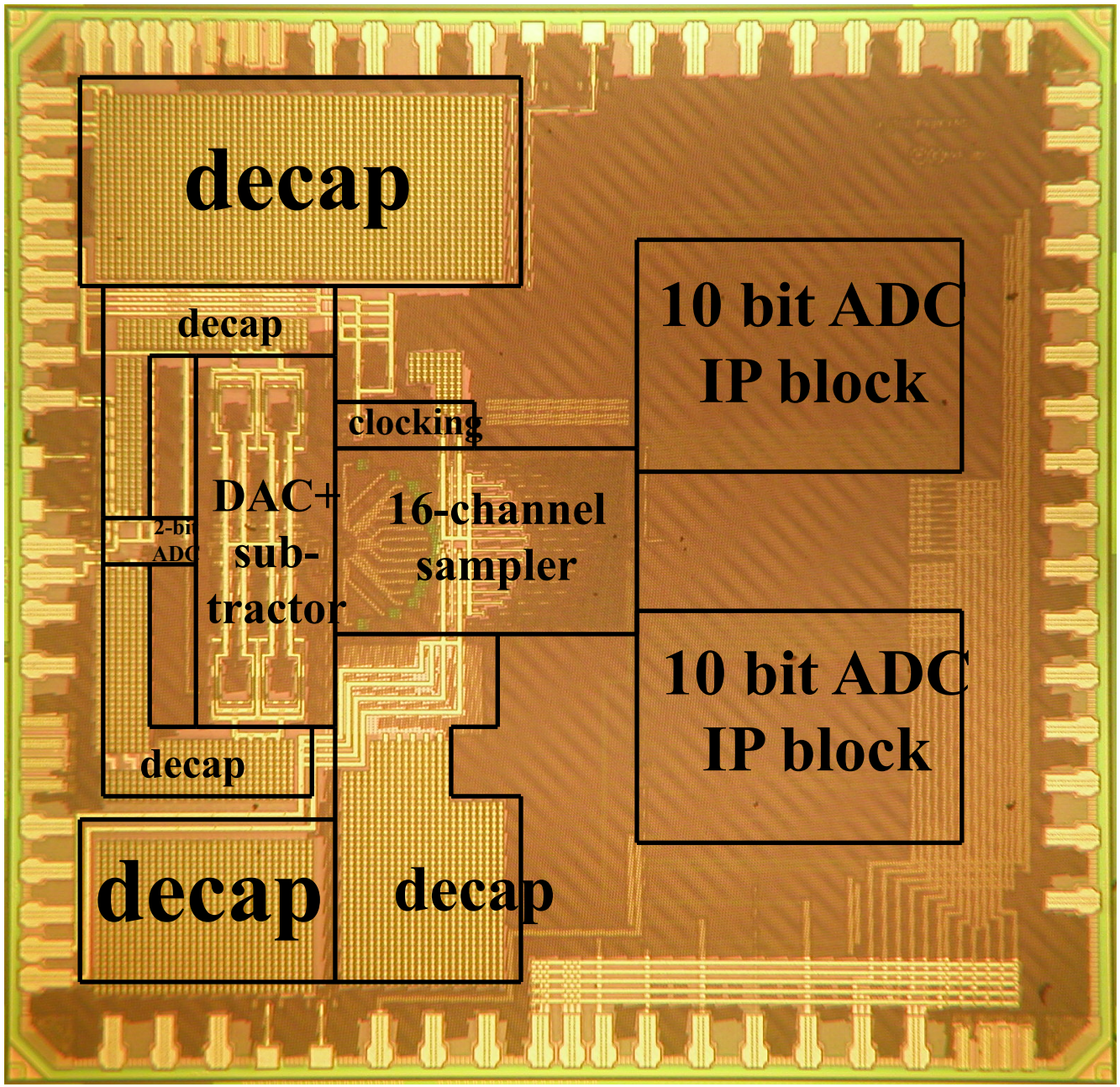
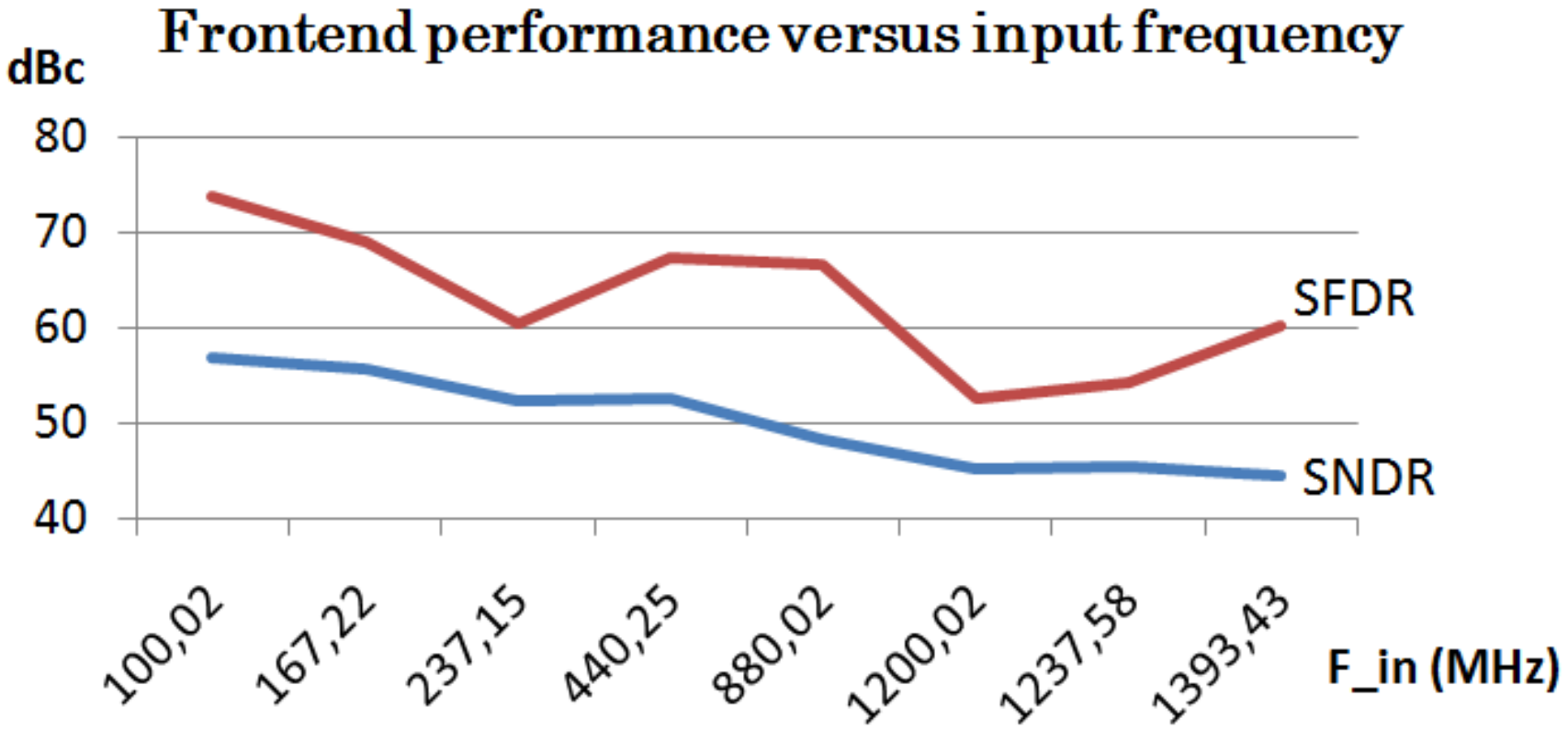


Die photo (total 5 mm^2, bolt-on circuit = 0.27 mm^2



Measurements

fs=800 Ms/s,



Summary

- Interferer robust RX
  - No voltage gain @ RF
  - **Filter** before voltage gain
  - HR: error of errors

- Digital Harmonic Rejection RX
  - **Adaptively** kills the biggest harmonic interferer

Summary

- Mixer-first RX
  - Very **linear**
  - Reasonably low noise without LNA

- N-path RF filter
  - very **linear**
  - high Q

Summary

- Interferer scrambler
  - Relaxes ADC design (linearity)
  - 2 bits extra input swing + better SFDR