



Cellular Electronics - Baseband Processing

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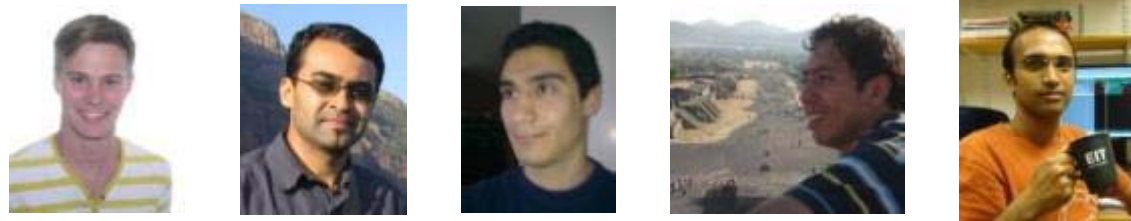
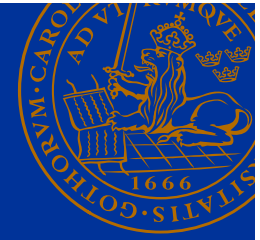
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Outline



- The team
- Multi-standard/Multi-mode
- Wrap-up: Multibase project and DFE Rx
- Sign-bit processing: an OK alternative?
- Knowing the channel: channel estimation for LTE.
- Multi-mode MIMO detection
- Life after OFDM: Going Faster than Nyquist?
- Conclusion

The Team



Multi-standard/Multi-mode



Multi-standard: Do we need a motivation today?

Multi-mode:

- experience fluctuating channel conditions
- satisfy dynamic system specifications
- static implementation for the worst case is highly inefficient
- Multi-mode implementation chooses the best mode dynamically



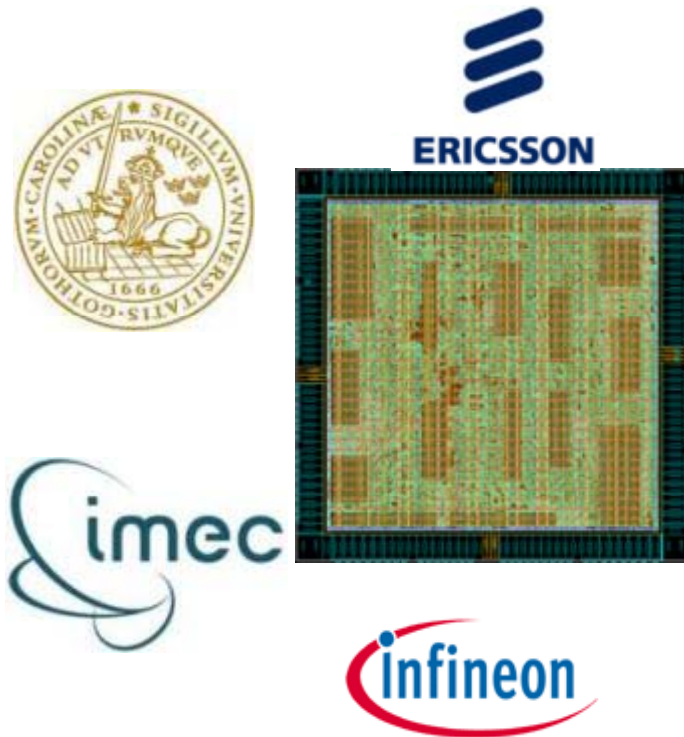
Different Environments



Different Applications

Main Focus: Investigate/develop algorithm with a hardware perspective!

Lund focus in circuits: DFE Rx



Contributors:

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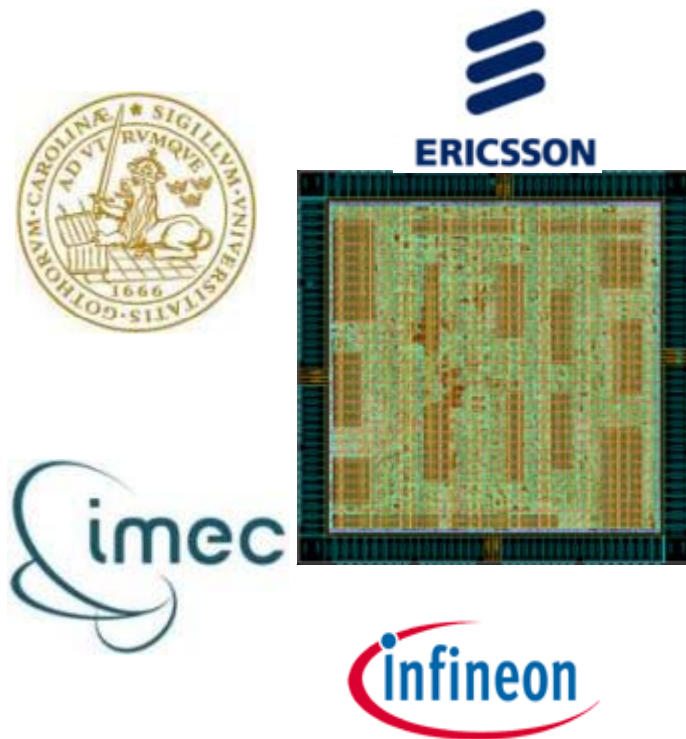
²IMEC

³Ericsson

Status of Multibase



Passed with flying colors at the final review.



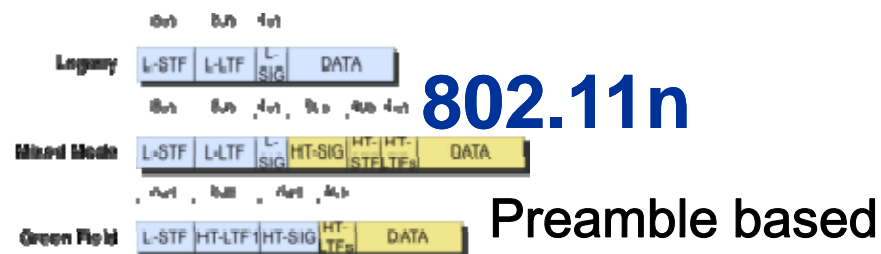
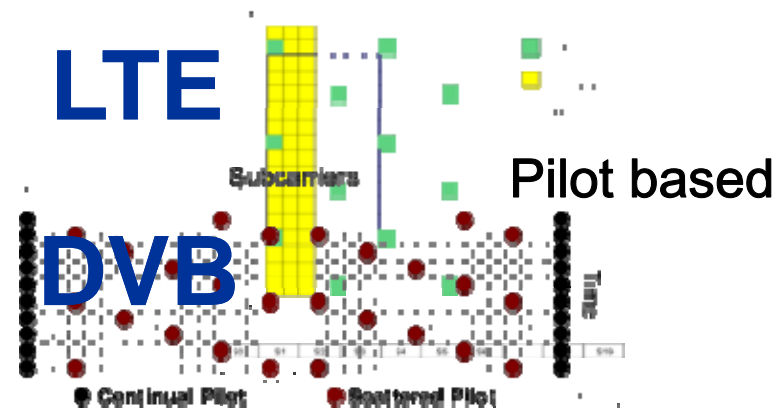
Status:

- Complete DFE Rx taped out in June.
- Working Silicon.
- Infineon 65nm CMOS
- Chip area 5mm²
- Core area 3.5mm²



Multi-standard concurrency...

- All three standards are OFDM based, however with different FFT-size:
 - LTE: 128-2048
 - DVB-H: 2048, 4092 (and 8192)
 - IEEE 802.11n: 64-128
- ...and different sample rates:
 - LTE: 30.72 Msp/s
 - DVB-H: 9.143 Msp/s
 - IEEE 802.11n: 20 or 40 Msp/s

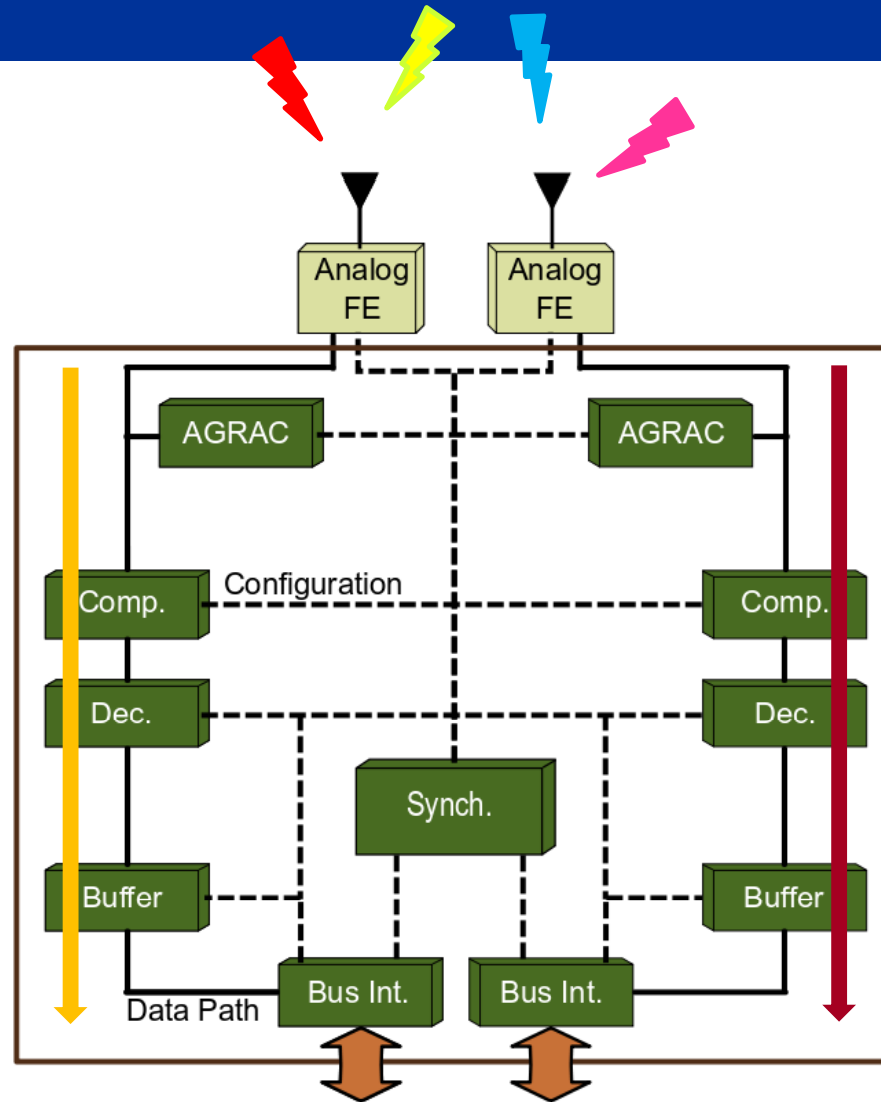


The Motivation: multi stream DFE-Rx



Two concurrent data streams in hardware.

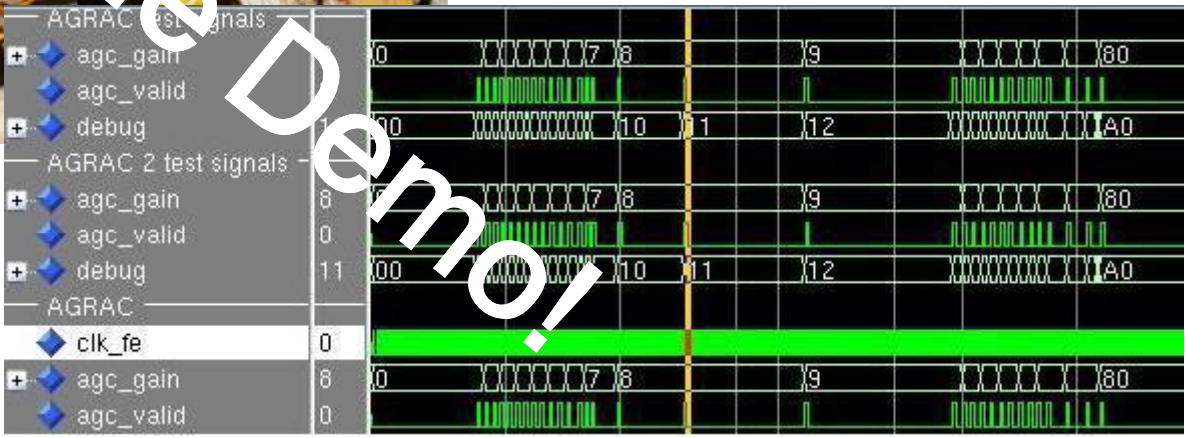
More data streams possible since they do not transmit all the time.





Verification and Test

Considerable testing is ongoing.



See the Demo!

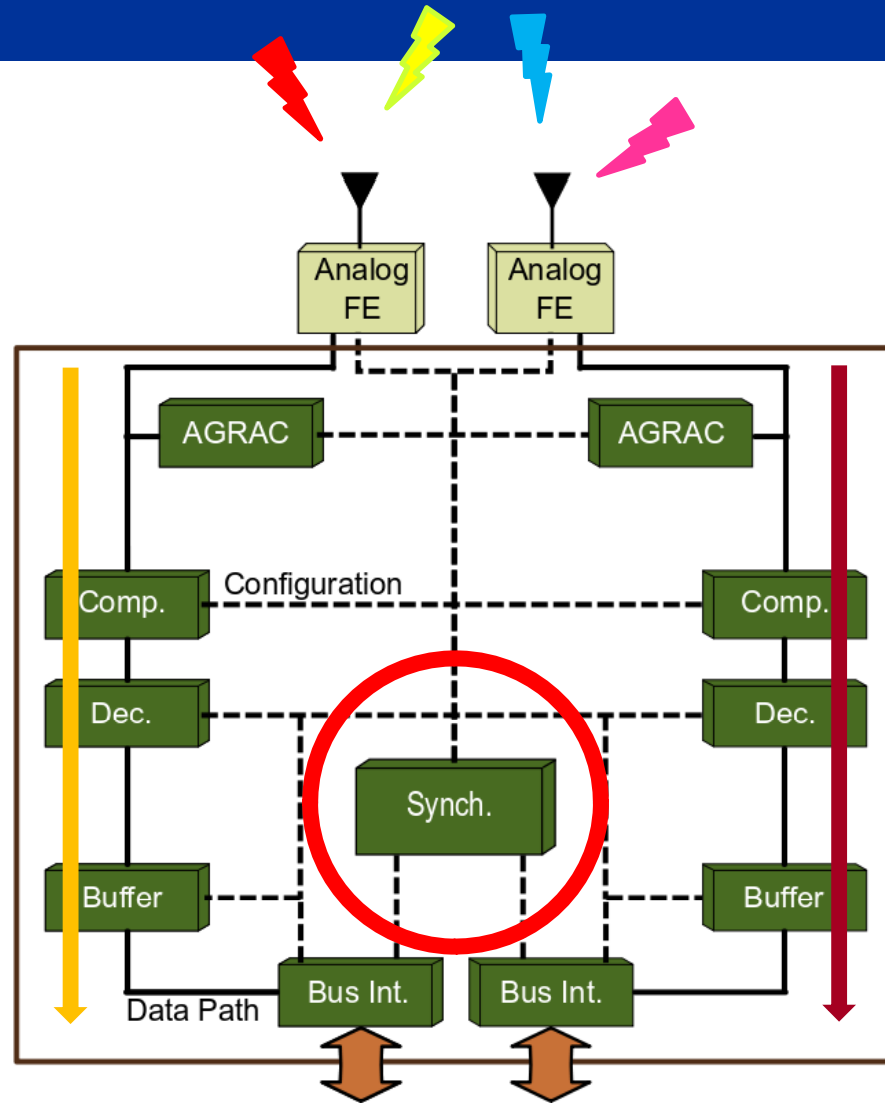


The Motivation: multi stream DFE-Rx

Two concurrent data streams in hardware.

More data streams possible since they do not transmit all the time.

 = Lund University

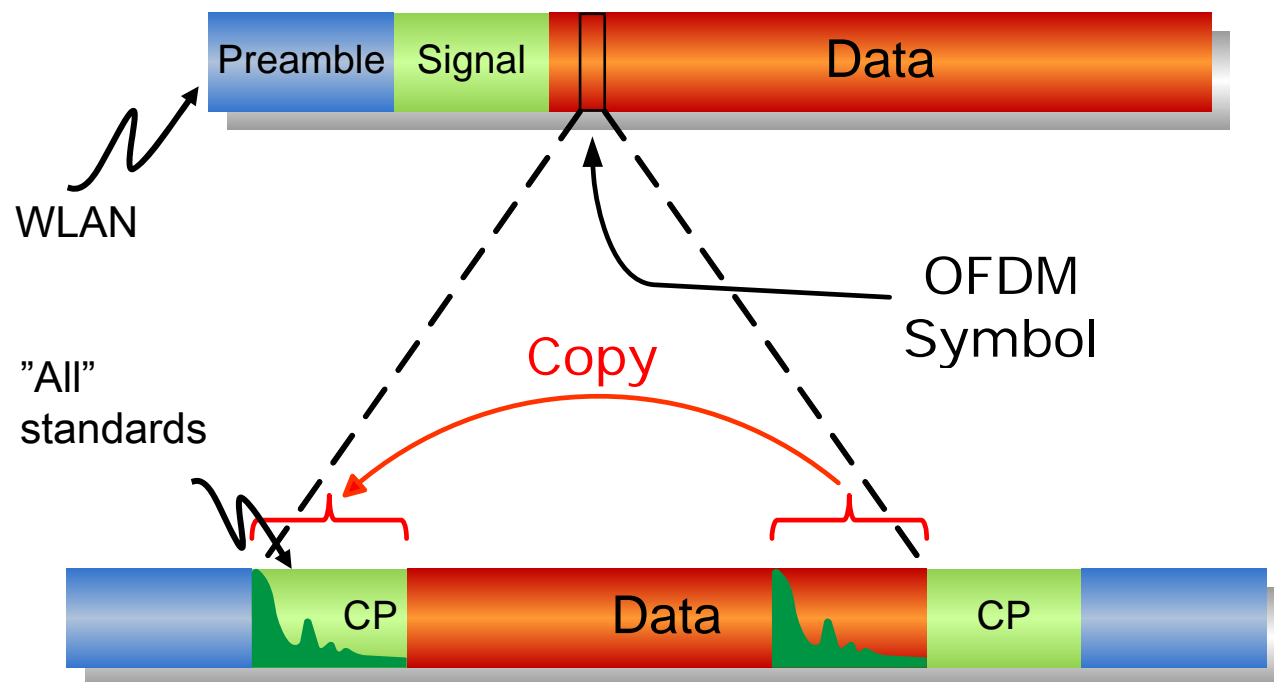


OFDM Synchronization

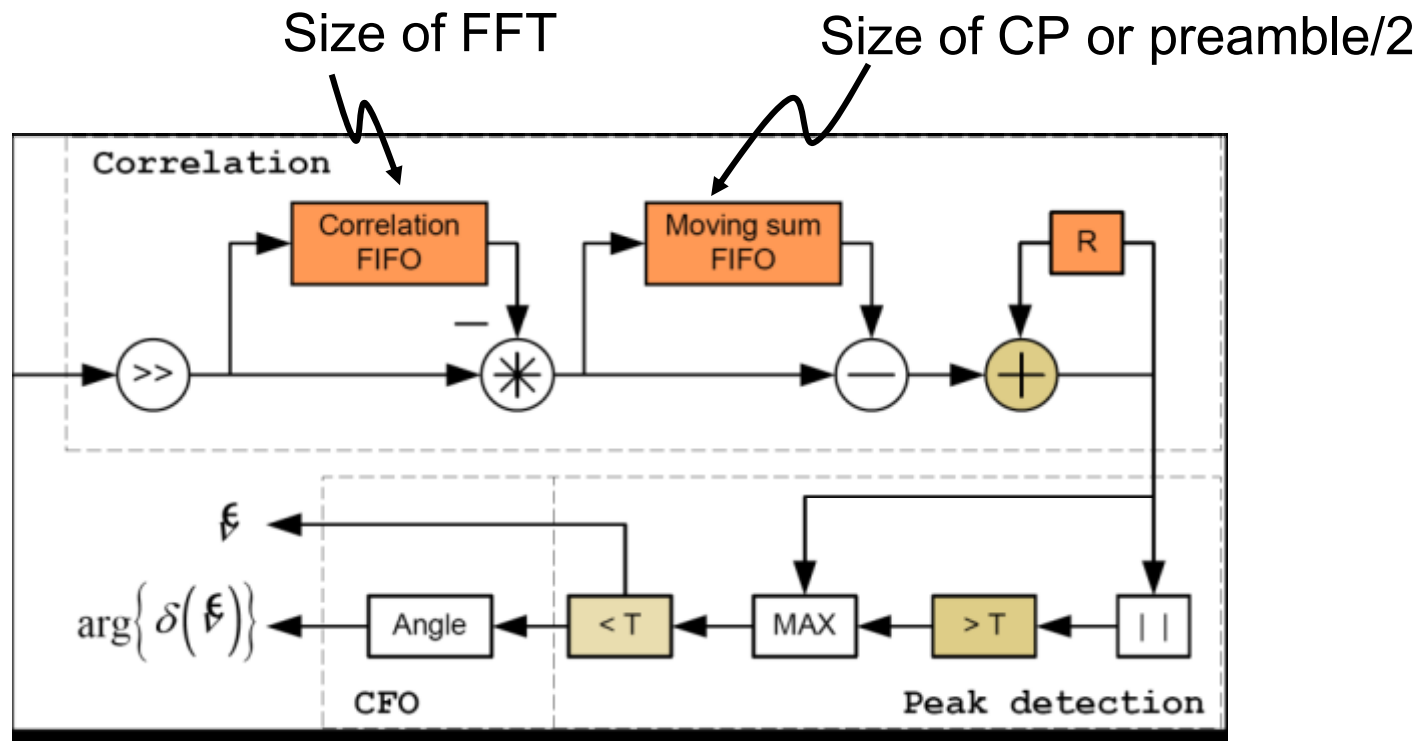


Synchronization

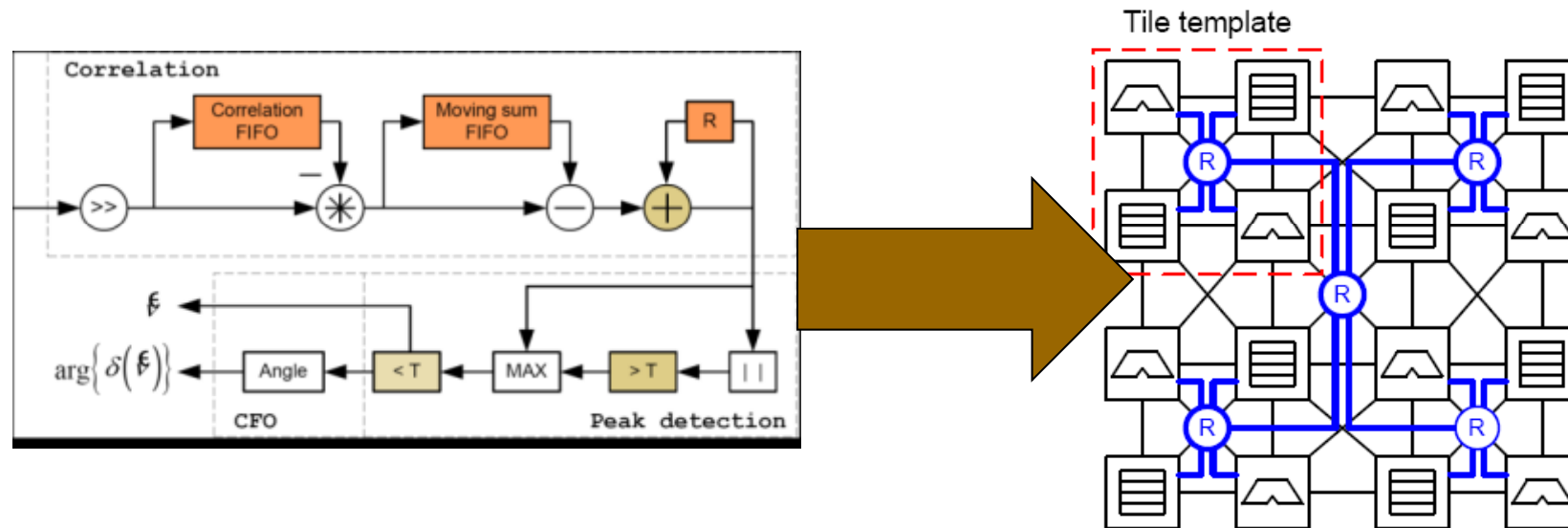
- either using the Preamble for WLAN
- or cyclic prefix for LTE and DVB-H (also WLAN but...)



Synchronization Architecture



Multibase Synchronization Hardware



Mapped onto a reconfigurable processing array:

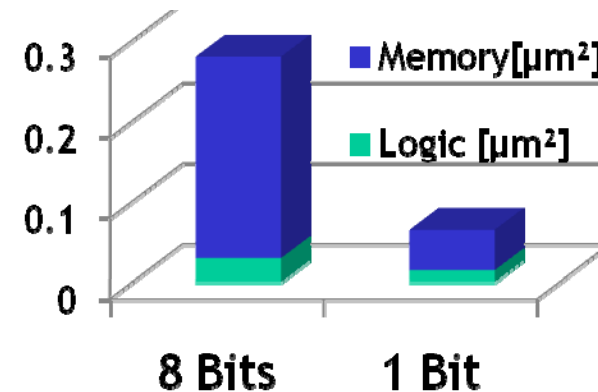
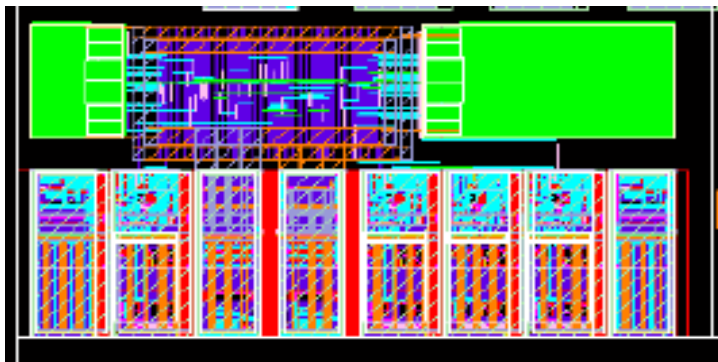
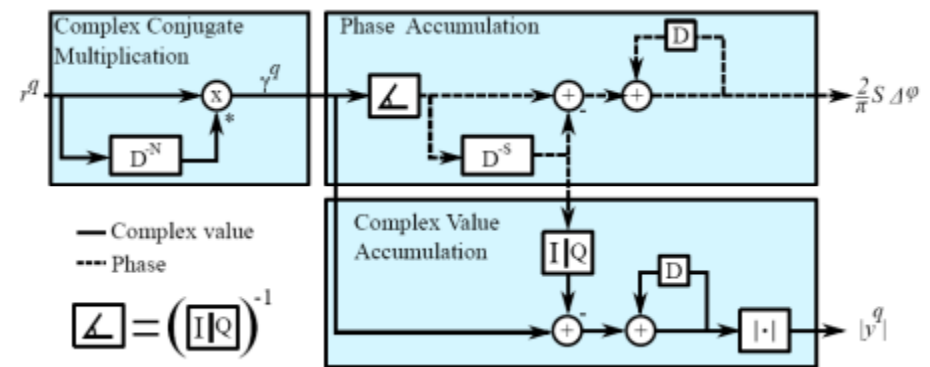
- flexibility since multi-standard
- hardware reuse since sync only part of the time

Next presentation!

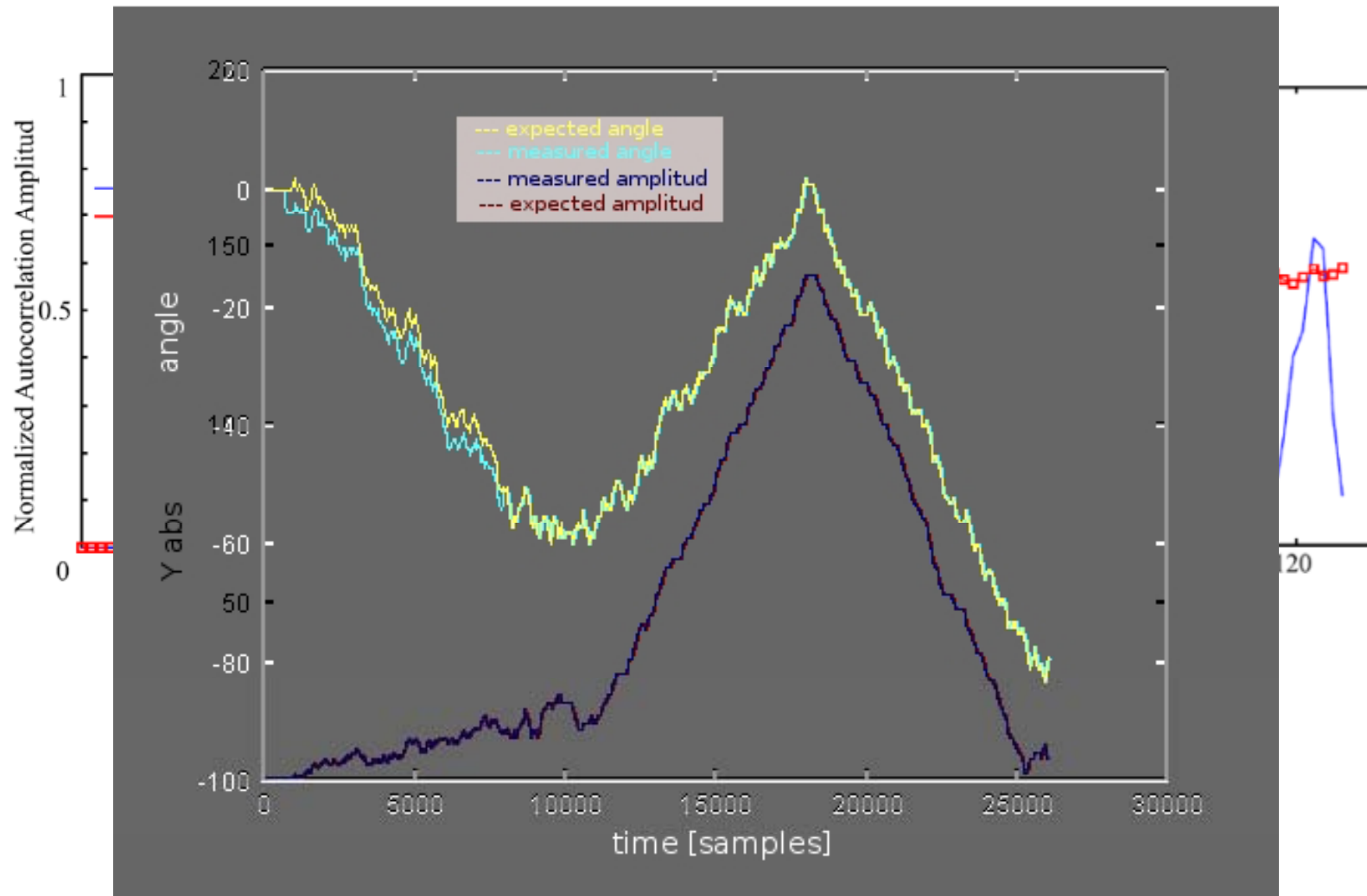
Alternative: Sign-Bit Synchronization together with Leif Wilhelmsson @Ericsson



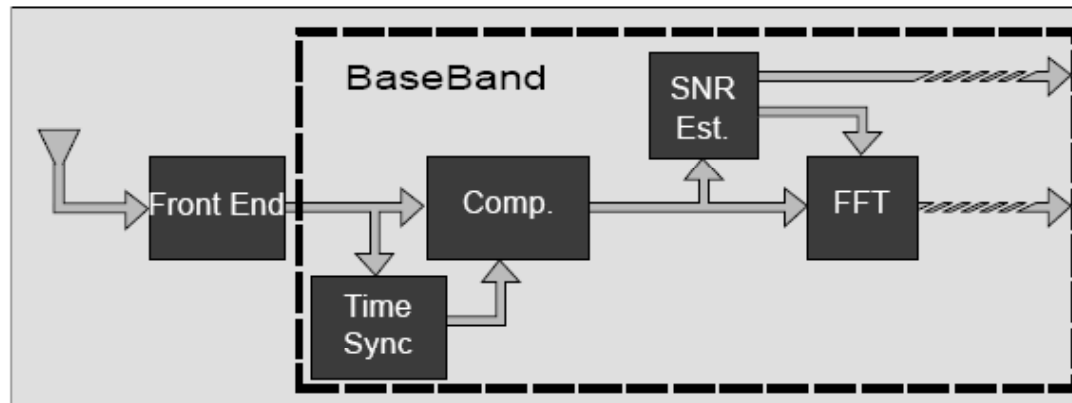
- Huge complexity reduction at a cost of performance degradation
- Area improvement for memories 97% when compared to 8-bits
- Area improvement for logic 70% when compared to 8-bits
- Total Area improvement 93% when compared to 8-bits



Sign-Bit Synchronization: Performance

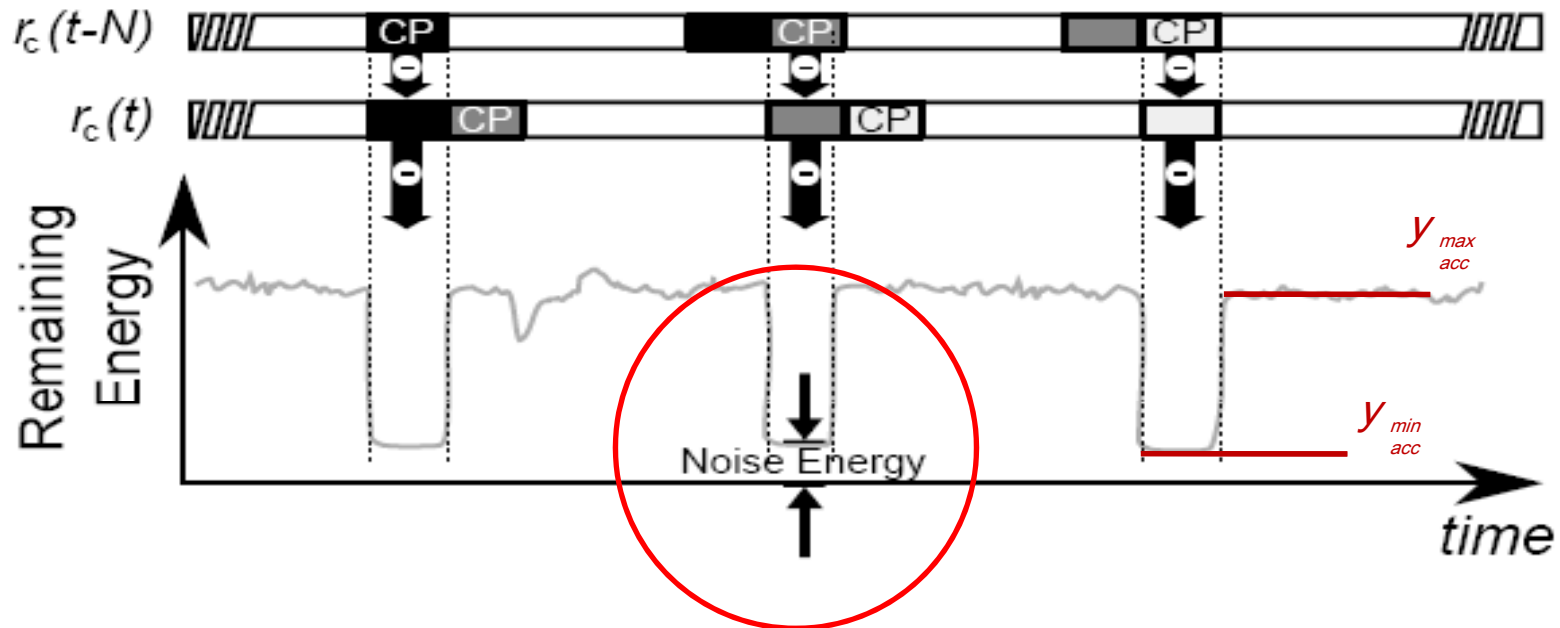
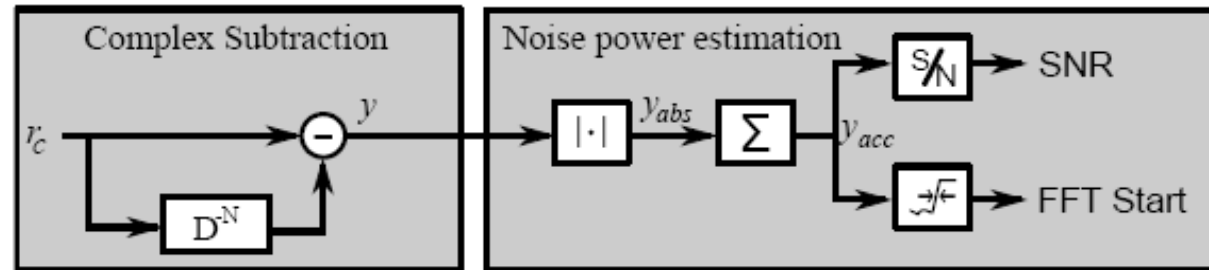


Early SNR estimation: useful for many functions

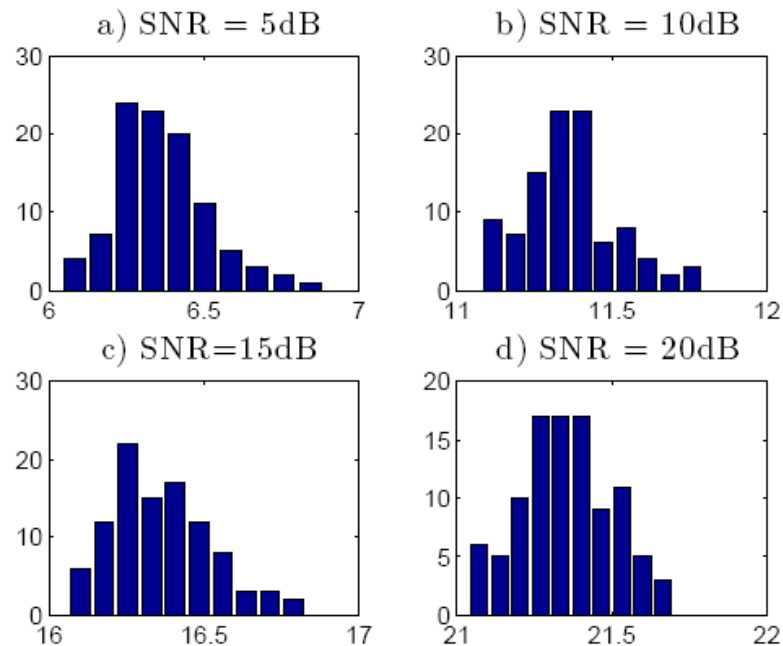


- Adapting Coding
- Channel Estimation
- Time Synchronization
- Base Station handover

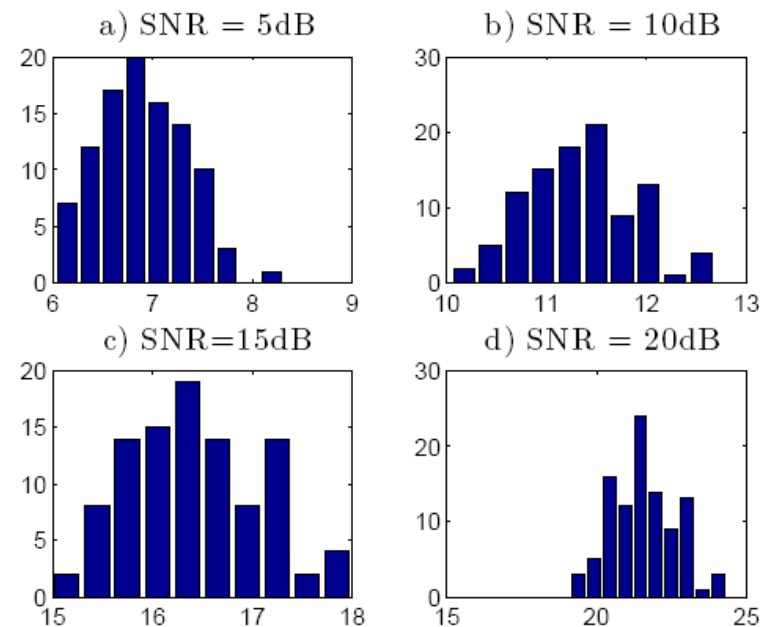
The SNR Estimator



Performance Analysis: clearly distinguishes low-medium-high SNR classes

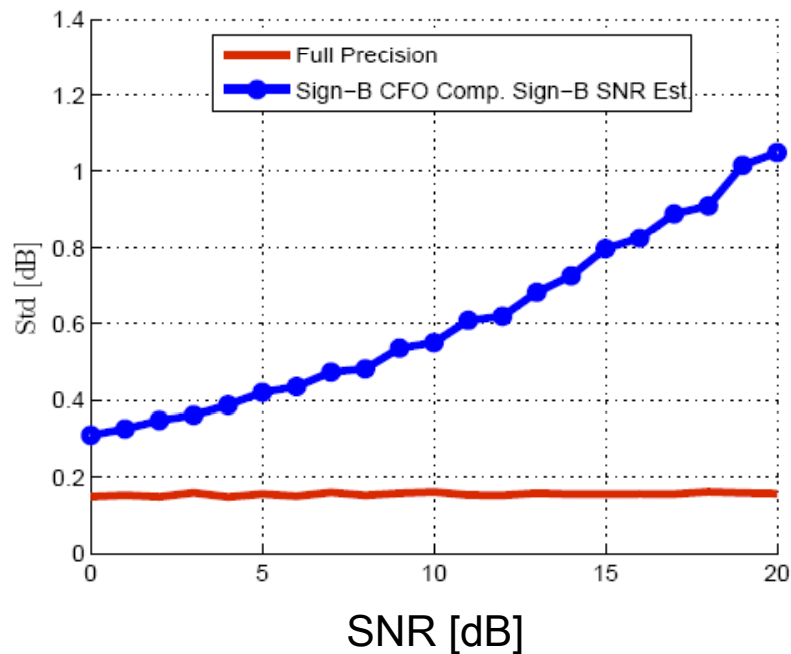


Full Precision under various SNR and CFO=50Hz

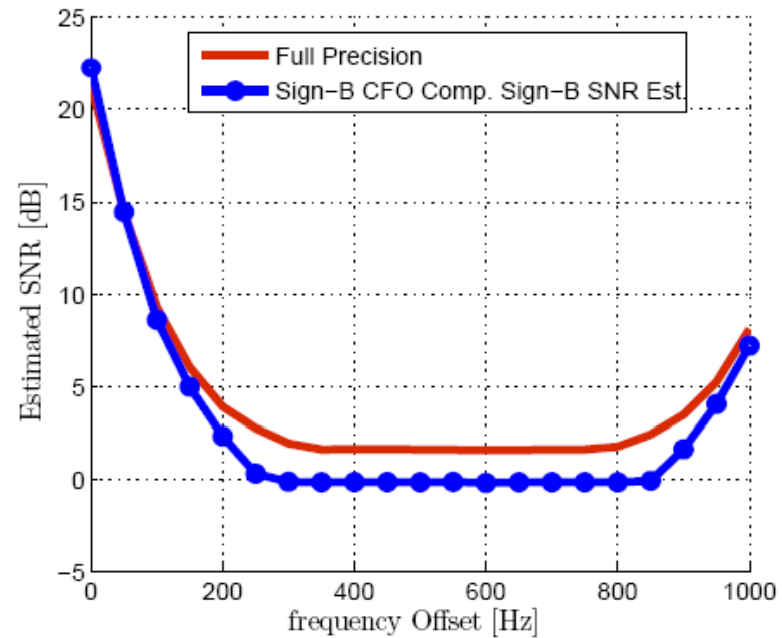


Sign Bit under various SNR and CFO=50Hz

Performance Analysis: Good results, mind CFO

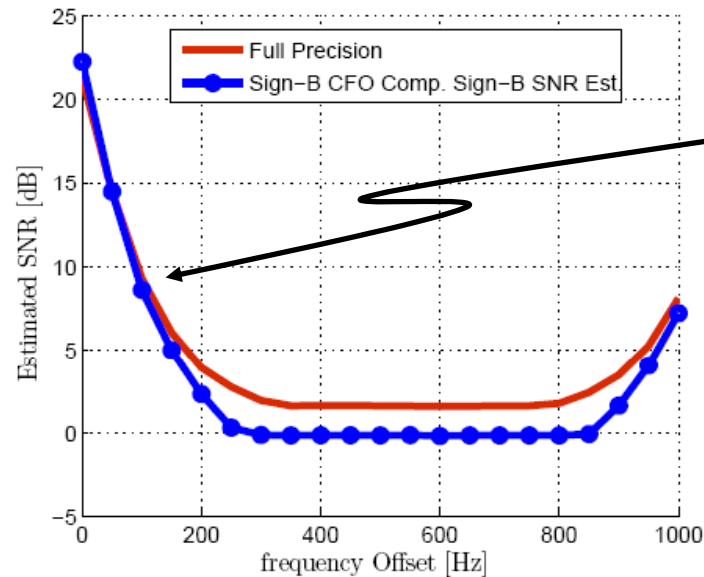
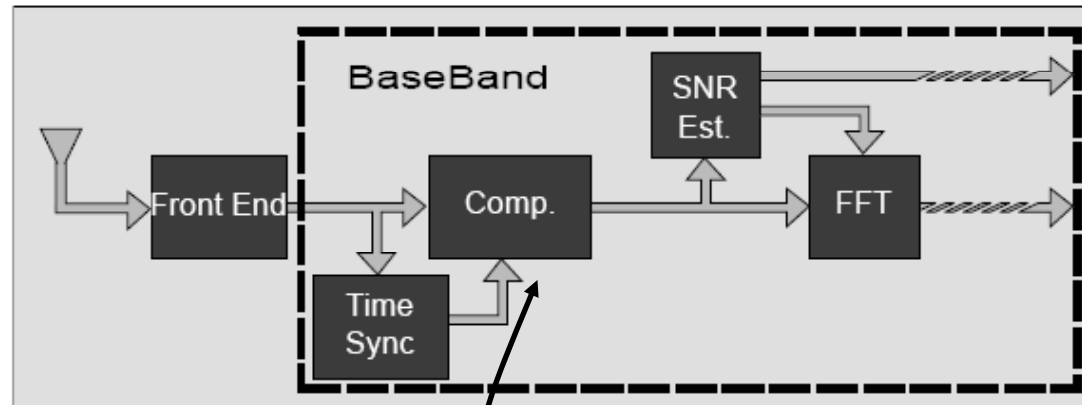


Standard deviation vs SNR



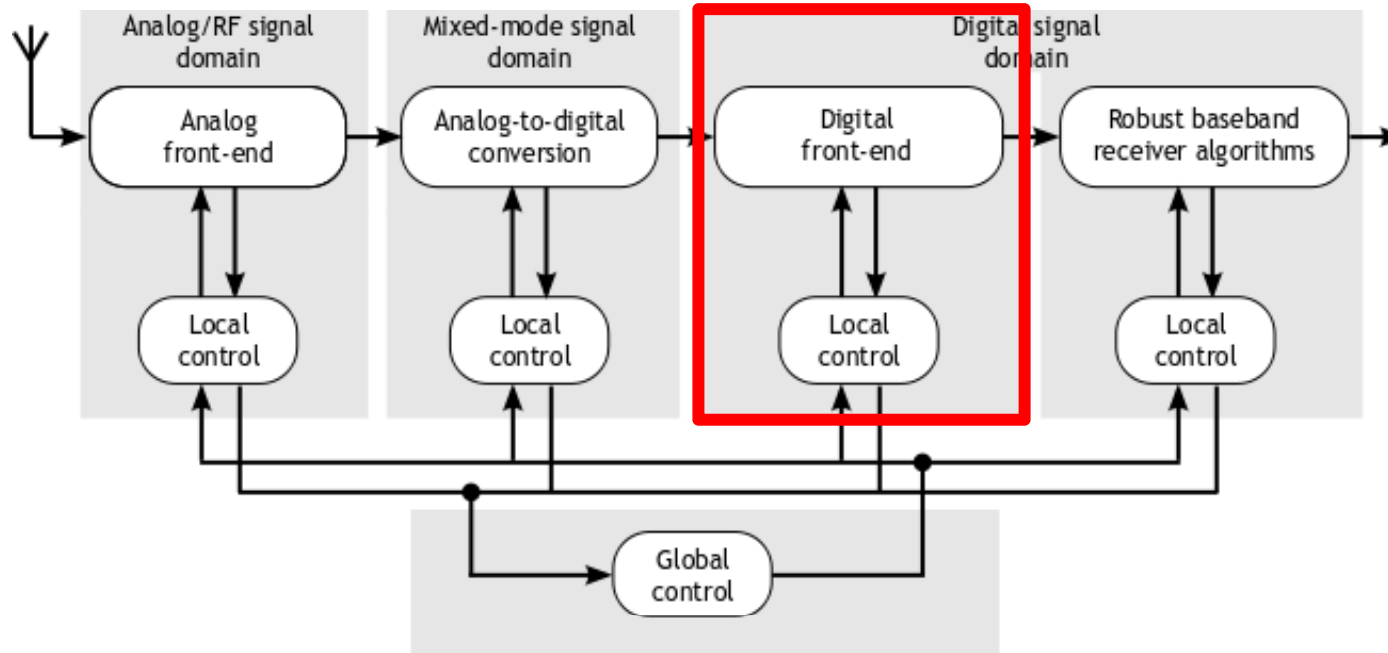
Estimated SNR vs CFO
(real SNR = 22dB)

SNR estimation in the baseband



• It is crucial to fix the CFO before the SNR estimation

We will continue the DFE within DARE!



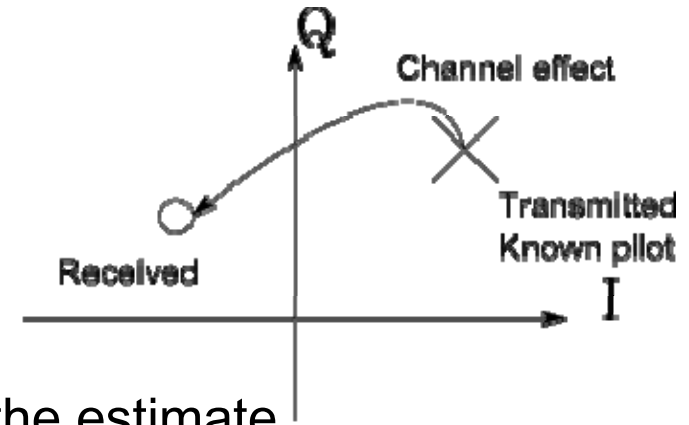
- *Target: LTE – rel. 10 , a.k.a. LTE-advanced*
- Compensation in the digital domain, e.g. IQ-imbalance, CFO, mismatch, etc.
- Adapt analog and AD blocks
- Exchange info with following baseband processing

Channel Estimation



Matching Pursuit Algorithm:

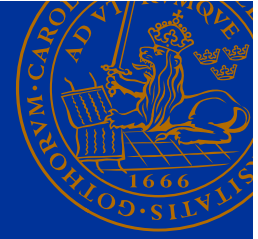
- The channel is estimated in the time domain
- A Successive Cancellation approach
 - The strongest tap is found and added to the estimate
 - At the same time its effects are removed from the input



What resolution should we use in the time domain?

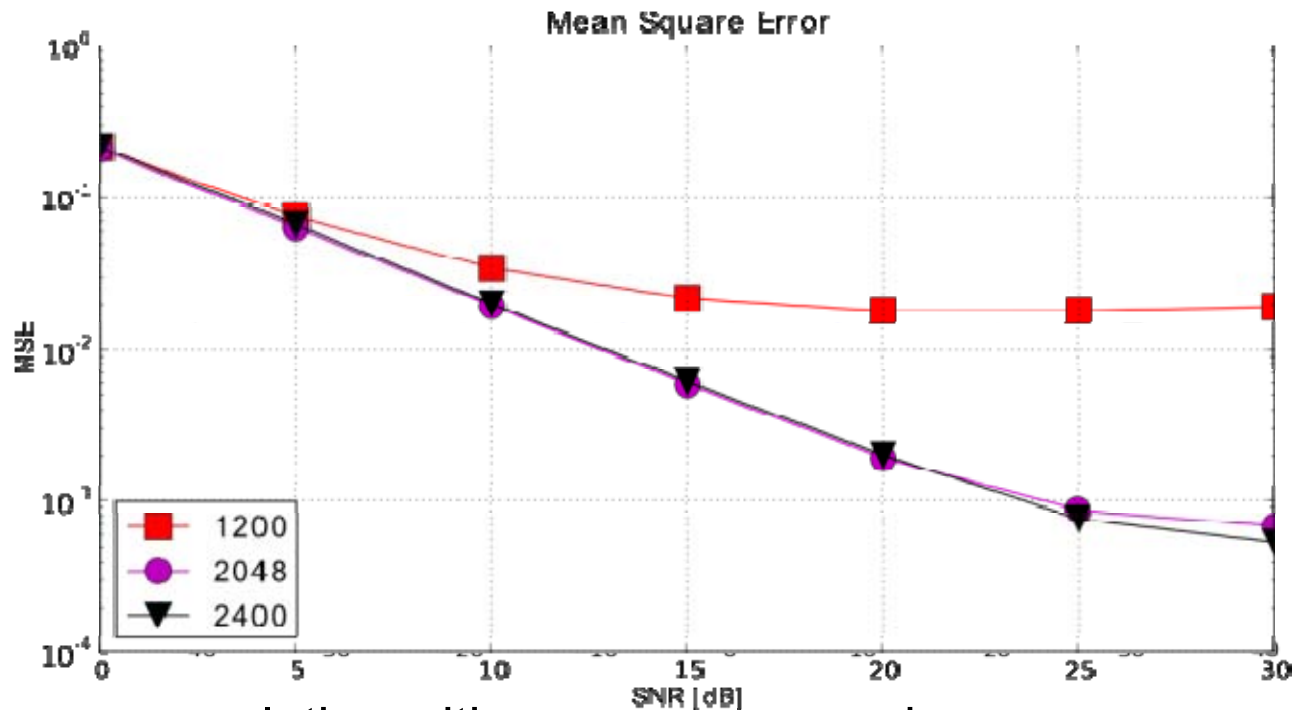
- Higher resolution tends to improve the estimate
 - ⇒ higher complexity.
- Certain resolutions with nice properties can be found
 - ⇒ large number of zero coefficients
 - ⇒ reduced complexity

LTE parameters



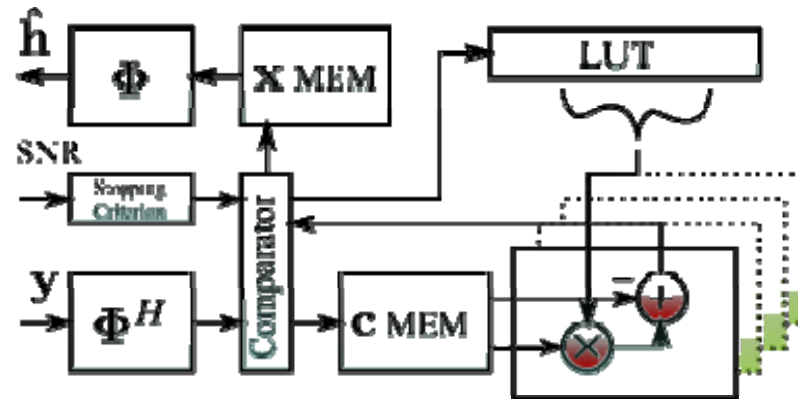
- Long Term Evolution
 - LTE Advanced has been accepted as the 4G standard
- Up to 20 MHz bandwidth
 - FFT Size (i.e. samples/symbol): 2048
 - Used Sub-Channels: 1200
- Two different cyclic prefix modes:
 - Short Cyclic Prefix: 144 samples
 - Long Cyclic Prefix: 512 samples
- Pilots or Reference Signals continuously transmitted

The coefficients



- Chose a resolution with many zero crossings
 - 1200 samples gives only one non-zero coefficients
 - Unfortunately low performance
 - 2400 samples means that every second coefficient is zero
 - Leads to lower complexity than for 2048 samples!

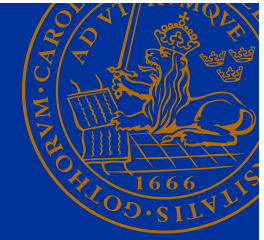
Hardware Architecture



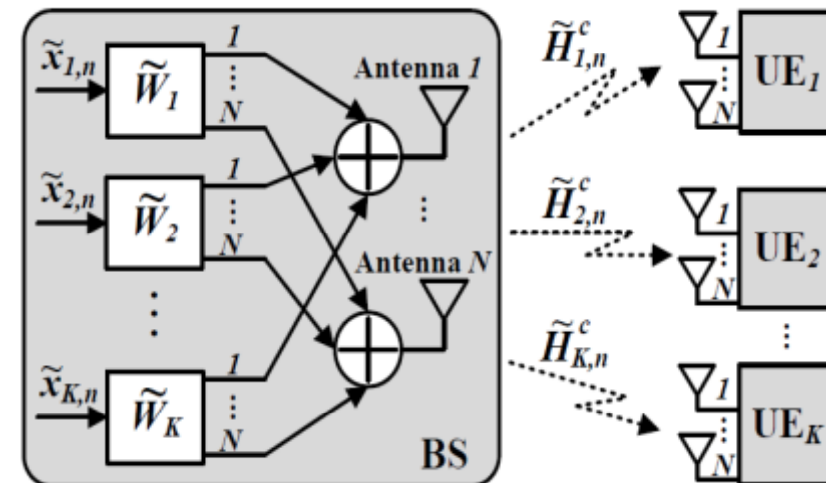
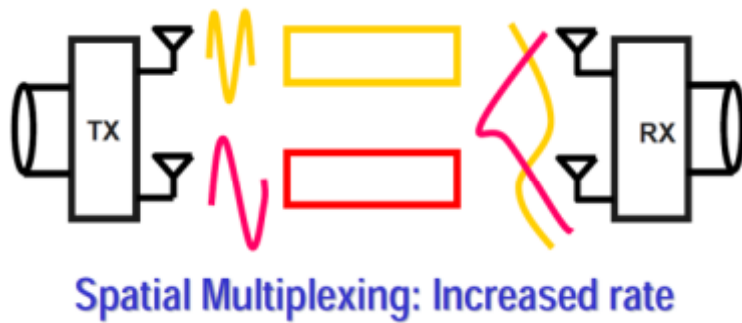
The FFT of 2400 points Decomposes as $N = 2^5 3^1 5^2$
 \Rightarrow requires Radix 3 and Radix 5 units

TABLE I
 MULTIPLICATIONS IN DIFFERENT STAGES

Design	One Iteration	IDFT/DFT	IFFT/FFT	Full Estimate
Original	512	~614K	~22.5K	~96K
Proposed	300	720K	~27K	~84K

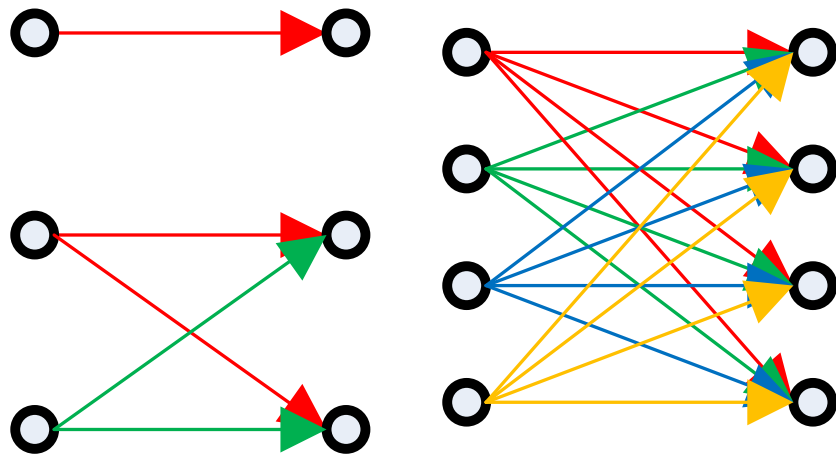


Multi-mode MIMO in LTE-A

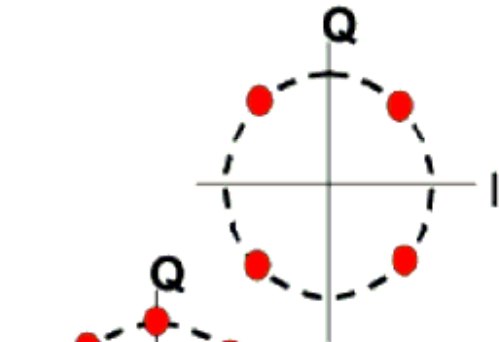


Space Division Multiple Access: Increase cell spectrum efficiency

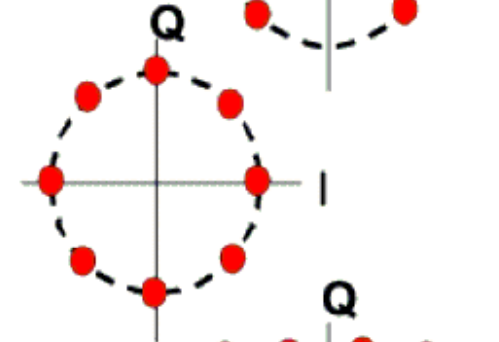
Different antenna configurations and modulation schemes



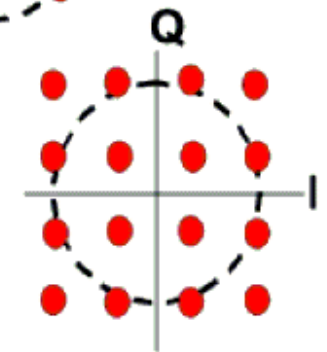
QPSK



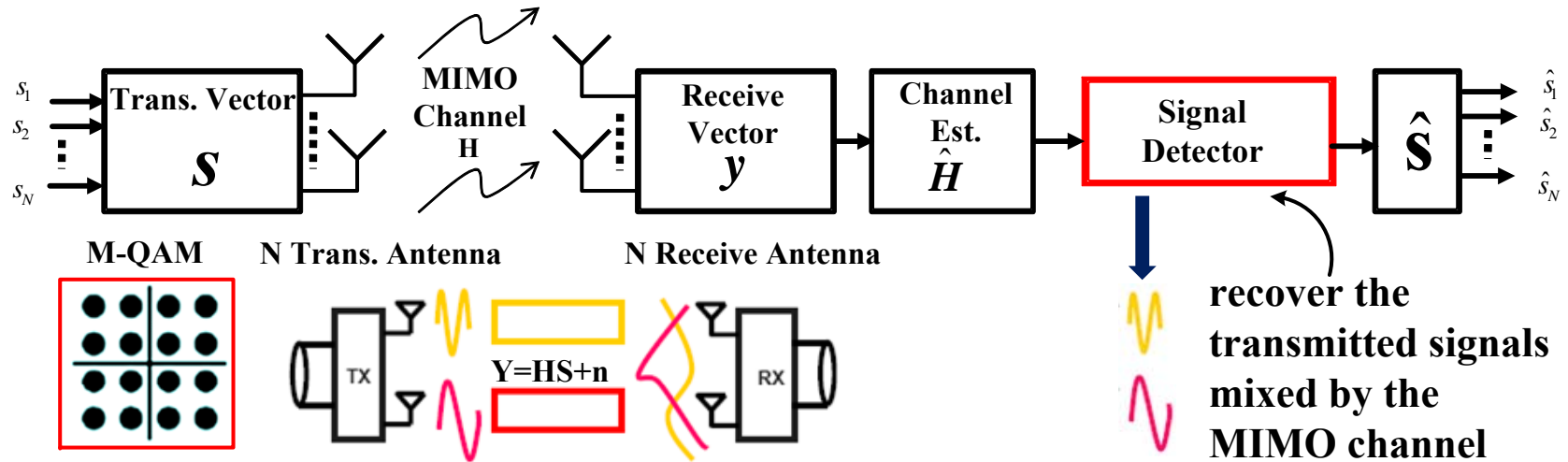
8PSK



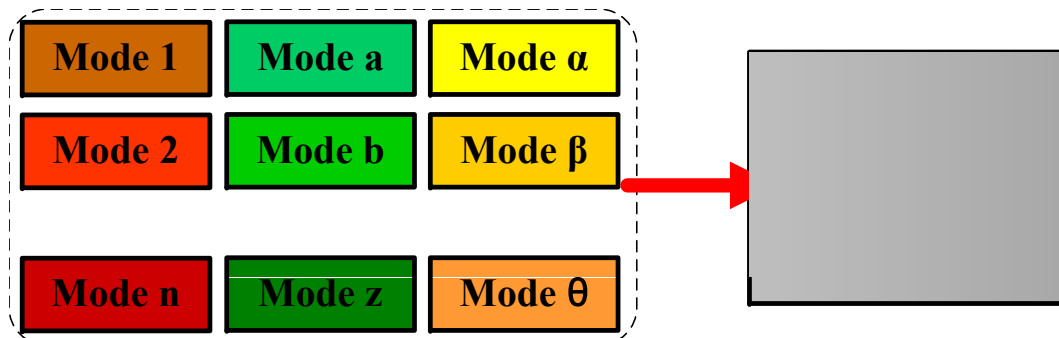
16QAM



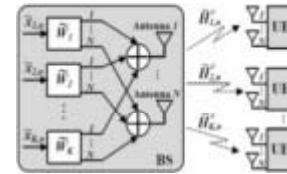
Objective: unified multi-mode signal detector



- Unified MIMO detector supporting multiple modes
 - Integrate multiple detectors into a single module \rightarrow area efficiency



Needed Resources



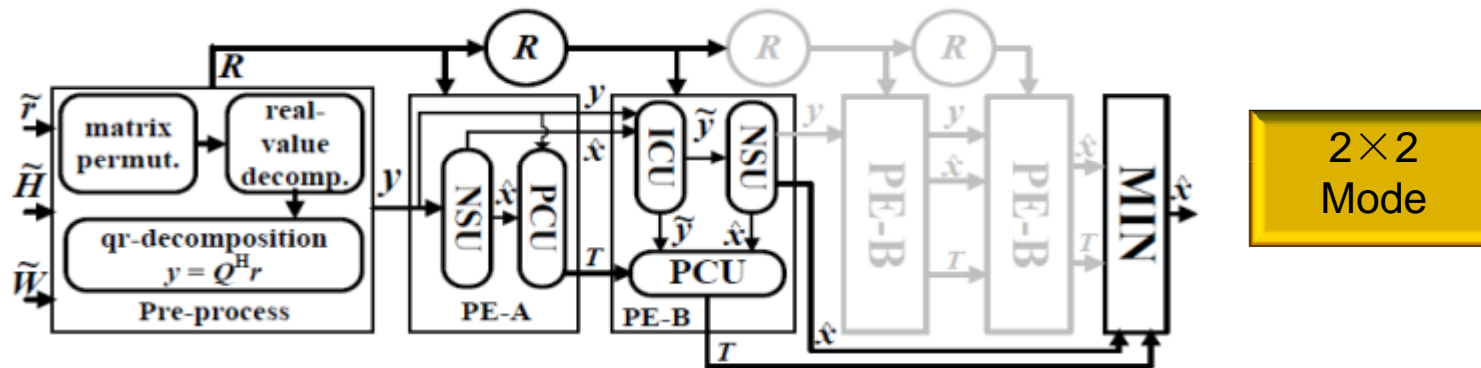
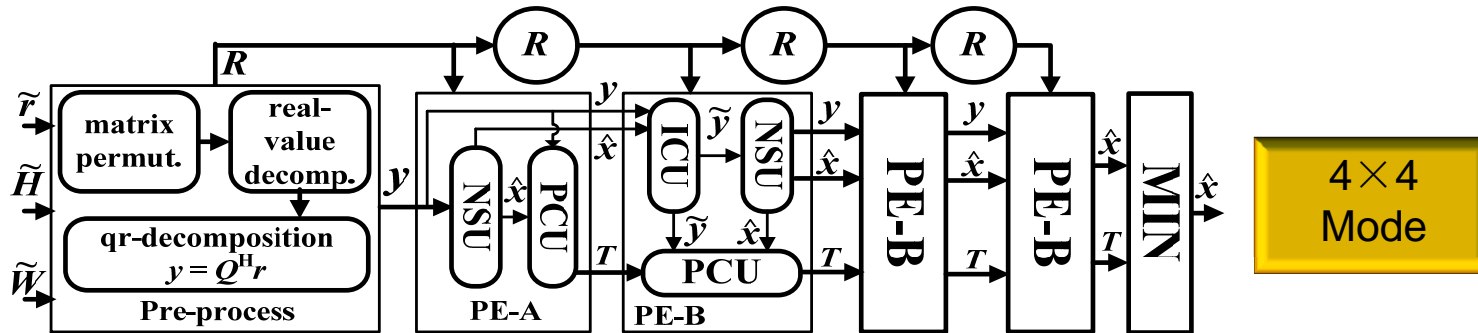
Operations	MIMO Technologies		
	SM	SDMA	SD
Matrix decomposition	✓	✓	✓
Matrix-permutation	✗	✓	✗
Node Selection	✓	✓	✓
Interference Cancellation	✓	✓	✗
Euclidean Distance	✓	✓	✓
Sorter	✓	✓	✗

- SM – using Imbalanced fixed-complexity sphere decoder
- SDMA – using Matrix permuted fixed-complexity sphere decoder
- SD – using Real-valued successive interference calculation

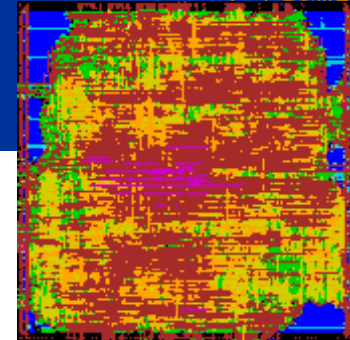
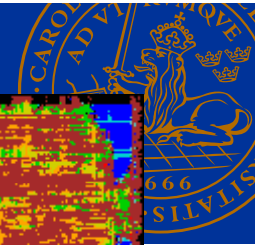
Example: SDMA



- Unified at the architecture design level
 - Multi-stage architecture corresponding to antennas
 - Activate different stages according to antenna configuration



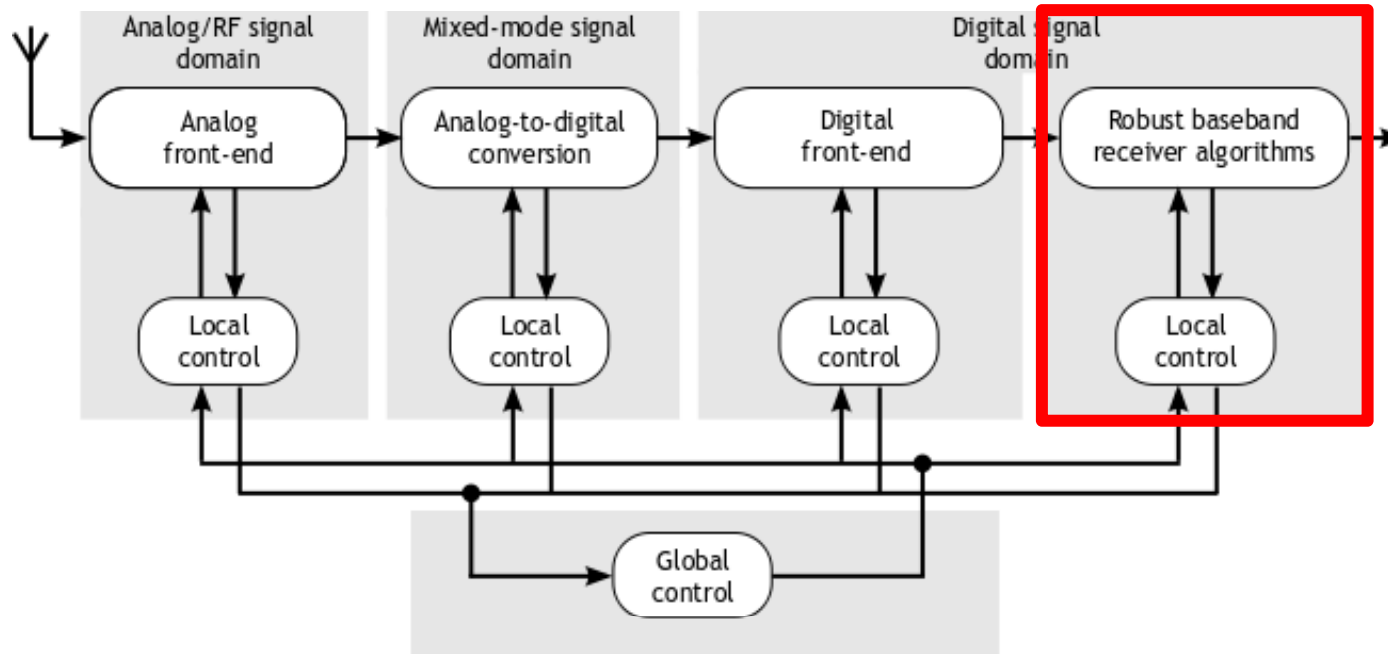
Results



- Proposed work 65nm CMOS, other 0.13 μ m CMOS technology
- Supports the largest number of MIMO modes
- Consumes the least hardware and energy

	TCAS-I'09	ISSCC'09	TCAS-II' 10	This Work
MIMO Tec.	SM	SM	SM	SM/SD/SDMA
Antenna Size	up to 6 \times 4	4 \times 4	up to 4 \times 4	up to 4 \times 4
Modulation	up to 64-QAM	64-QAM	up to 64-QAM	up to 64-QAM
Core Area	1.46 mm ²	0.9 mm ²	3.9 mm ²	0.25 mm ²
Gate Count	205 KG	114 KG	491 KG	88.2 KG
Clock Rate	71 MHz	282 MHz	137.5 MHz	165 MHz
Throughput	114 Mb/s	675 Mb/s	1.1 Gb/s	1.98 Gb/s
Power Consumption	30 mW @ 1.1 V	135 mW @ 1.3 V	127.2 mW @ 1.2 V	102.7 mW @ 1.2 V
Normalized Power	17.9 mW	57.5 mW	63.6 mW	102.7 mW
Normalized Energy	156.6 pJ/b	85.2 pJ/b	57.8 pJ/b	51.8 pJ/b

We will continue MIMO within DARE!



- **Target: LTE – rel. 10 , a.k.a. LTE-advanced**
 - Robust baseband receiver algorithms
 - Including carrier aggregation, e.g. Isael Diaz is currently visiting IMEC and is working on a project looking at hardware architectures within this area.

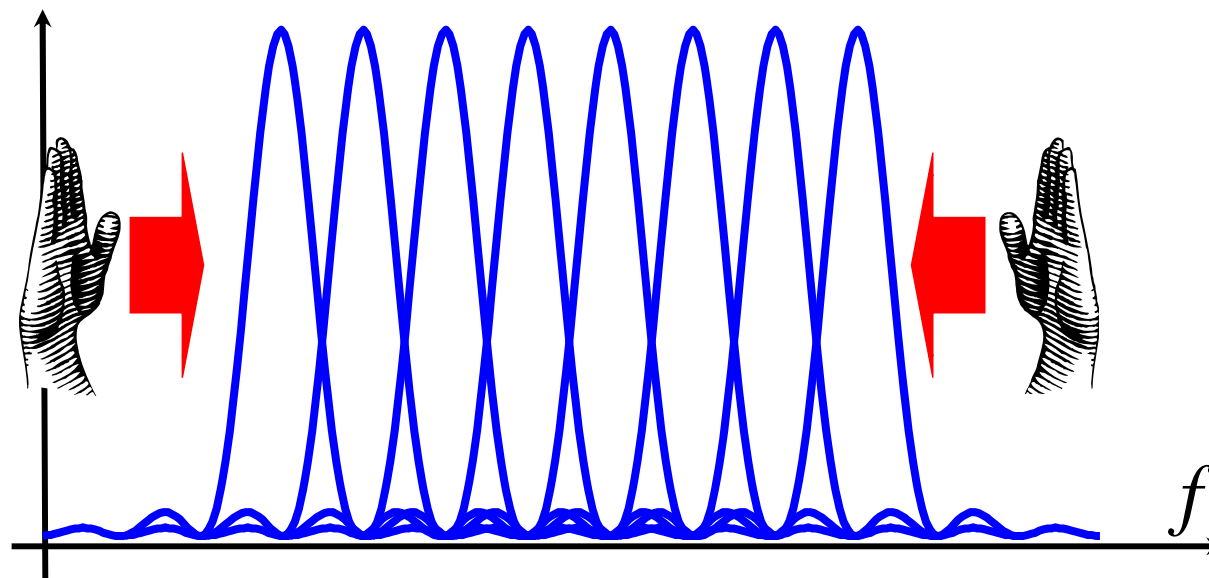


Life after OFDM: Going Faster than Nyquist?

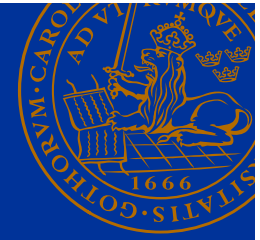
FTN Signaling



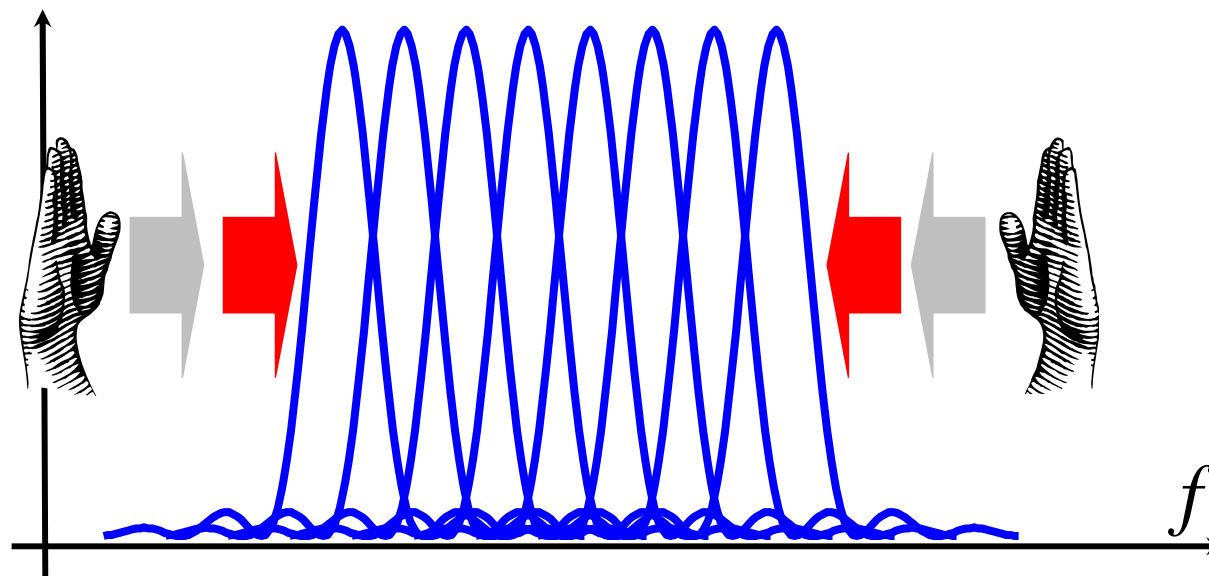
- Original concept by J.E. Mazo in 1975 (Bell Syst. Tech. J).
- Main idea
 - transmit info beyond Nyquist's criterion for ISI free transmission.
 - Stack closer in time and/or freq – induce intentional interference.



FTN Signaling



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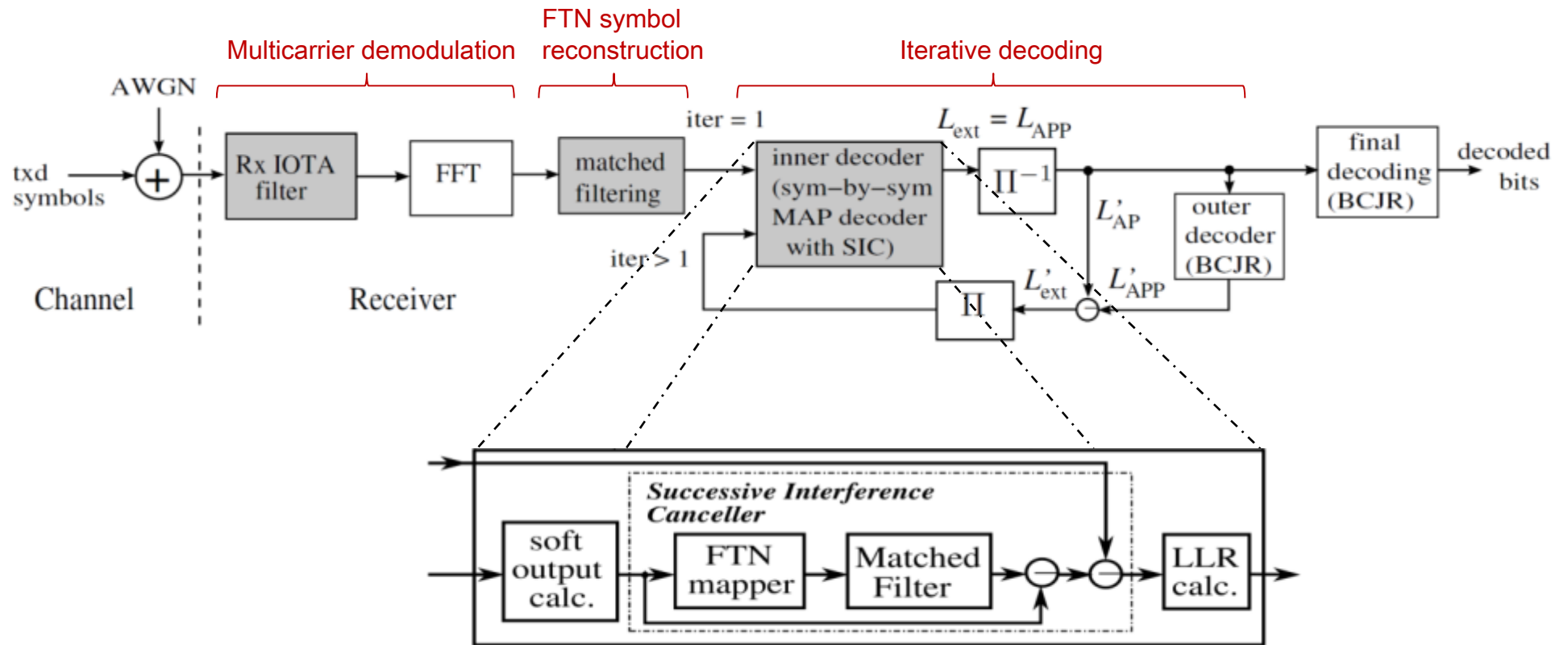


FTN Signaling



- Original concept by J.E. Mazo in 1975 (Bell Syst. Tech. J).
- Main idea
 - transmit info beyond Nyquist's criterion for ISI free transmission.
 - Stack closer in time and/or freq – induce intentional interference.
 - Investigate OFDM-systems due to their popularity
 - Reuse as much as possible from a "standard" system
- Motivation: Bandwidth efficient systems
 - Alternative to higher order modulation
 - Study hardware feasibility

FTN Architecture

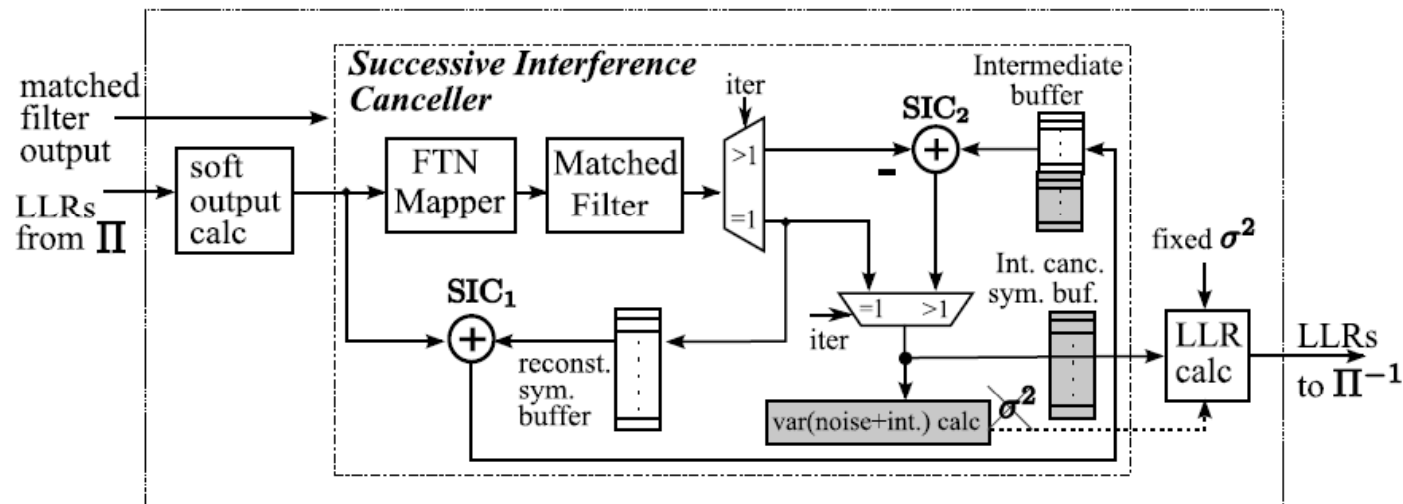


- Trade-off bandwidth for hardware complexity!
- Keep as much as possible from a "traditional" system.

Optimizing the architecture



- Initial design: 0.5 mm² in ST65 nm standard cell CMOS
- Power: 44mW (80% in the memories)!

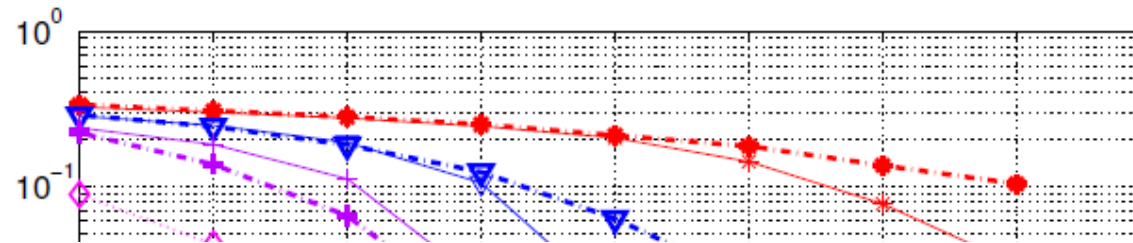


Main target for optimization: the memories!

For example by using a fixed variance:

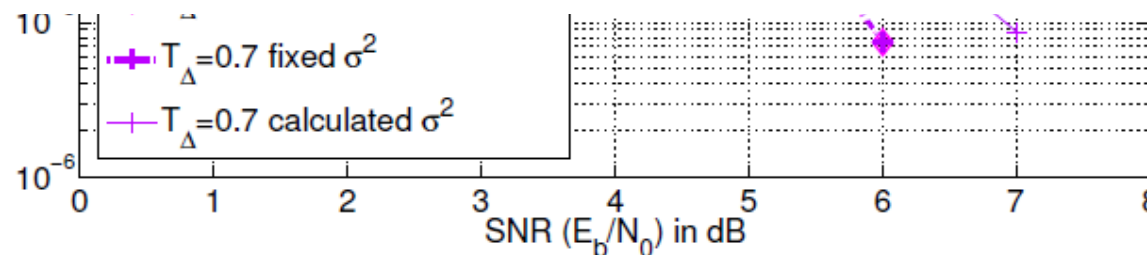
- Reduce algorithmic complexity (minor)
- Saves buffer (major)!

Performance with fixed variance



COMPARISON OF TOTAL AREA AND POWER BETWEEN BASELINE AND MEMORY OPTIMIZED IMPLEMENTATIONS.

	Baseline [7]	Memory optimized	Savings
Chip area	0.519 mm ²	0.370 mm ²	28.7%
Total Power	44.7 mW	25.1 mW	43.8%
- Logic	8.0 mW	6.5 mW	18.7%
- Memory	36.7 mW	18.6 mW	49.3%

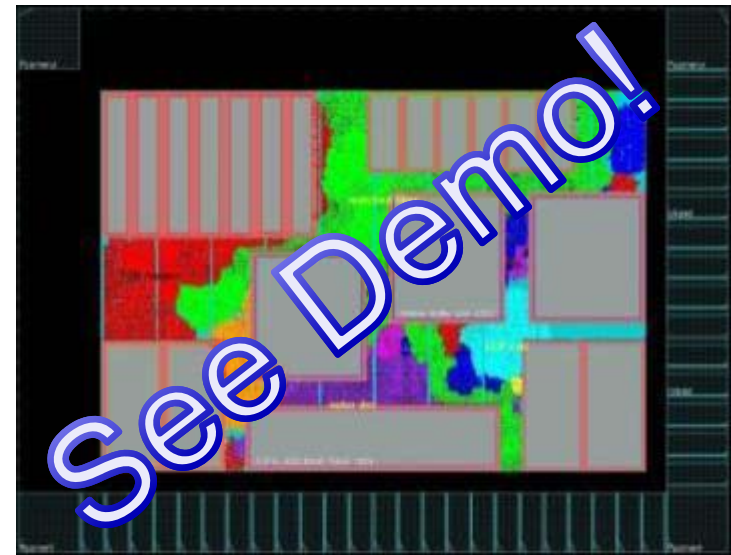


Fabricated Silicon



- Chip area: 0.5 mm² in ST65 nm standard cell CMOS
- Power: 44mW (80% in the memories)
- Throughput: 3.2Mbps at 300MHz.
- Tape-out: November 2010
- Measured and working.

- FTN-signaling is deemed feasible from a hardware perspective.
- Complexity overhead.
 - Memory : same order as a max-log-MAP implementation, (7,5) conv code.
 - Logic: ~5 times



Published in IEEE Transactions of Circuits and System – I (TCAS-I)

Conclusion



- Results and future plans for Digital Front End architectures
- Sign-bit processing for low complexity
- Reduced complexity channel estimation in LTE
- Multi-mode MIMO detection architectures
- Architecture and implementation of an FTN-signaling receiver.



Thank You!

2010-09-09

Lund Circuit Design Workshop 2011