Reconfigurable Cell Array as an Enabler for Future Processing

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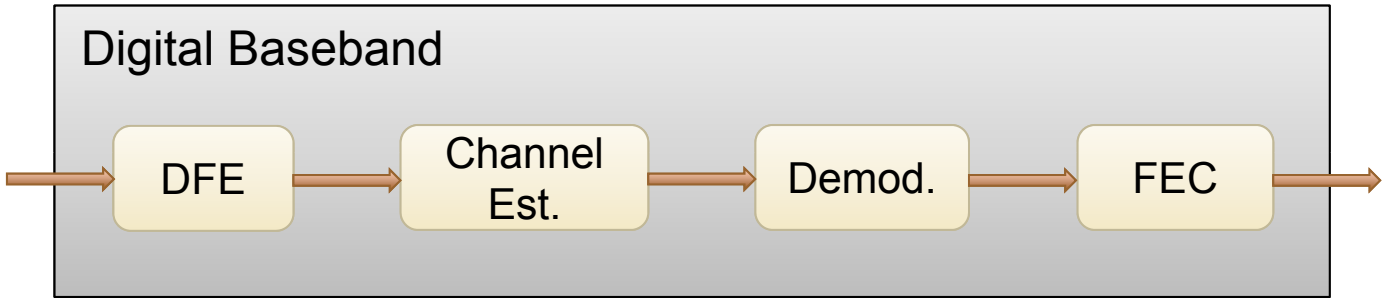
Outline

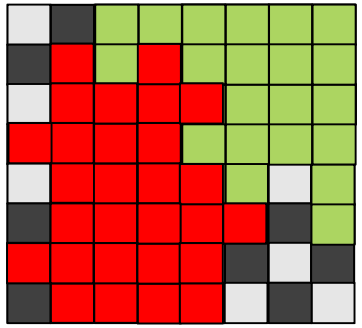
- Motivation
- Coarse-grained reconfigurable cell array
  - Resource cell
  - System reconfiguration
- Software development
  - Application mapping
  - Design exploration
- Case study: multi-standard OFDM synchronization

Motivation

- Hardware sharing
  - Accelerators: poor hardware reusability



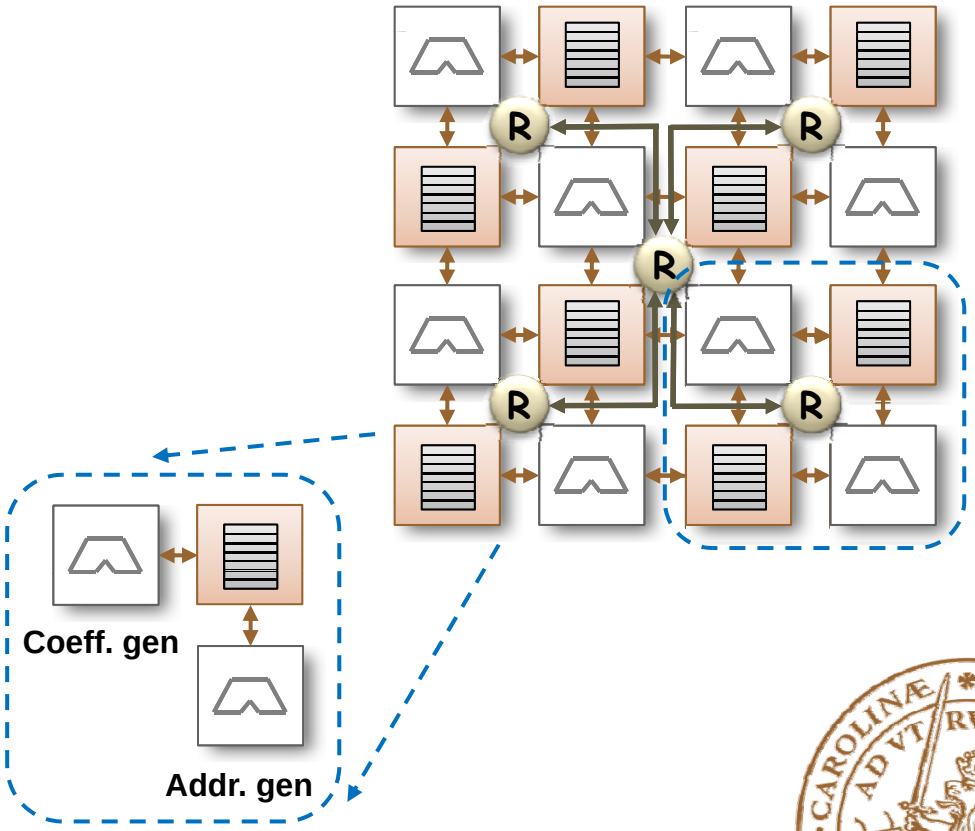
  - Reconfigurable architecture
    - \+ Multi-task
    - \+ Multi-standard
    - \+ Multi-algorithm
    - − Control overhead, e.g. area, power.



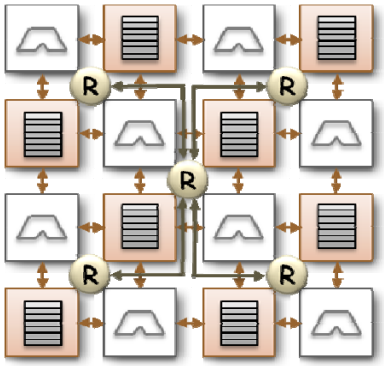
System infrastructure

- An array of resource cells.
- Heterogeneous cell array:
  - Processing cell
  - Memory cell
  - Accelerator

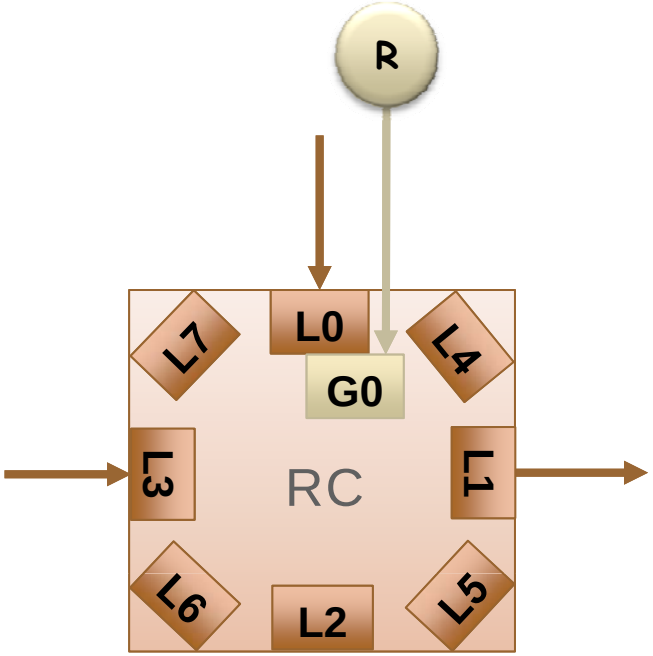
    (e.g. no configuration)
- Hierarchical cell array.



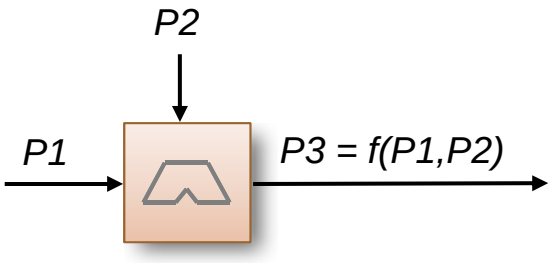
Resource cell



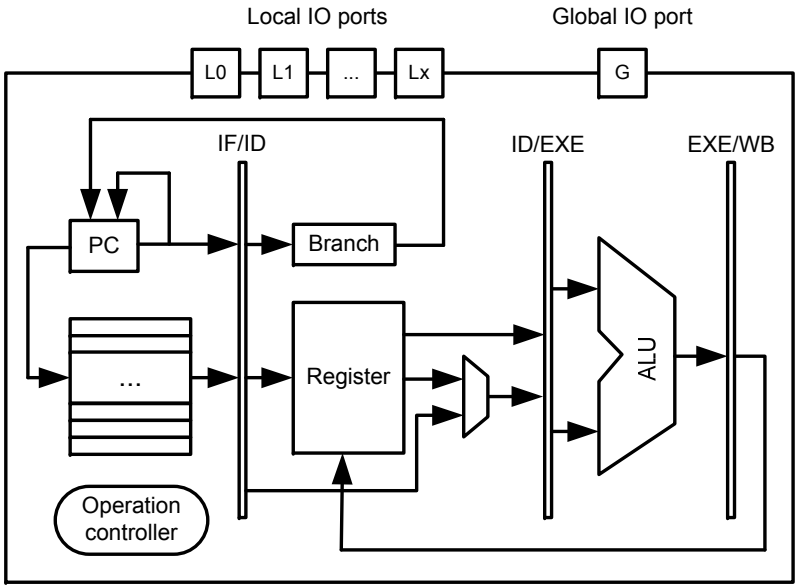
- Dedicated local interconnections:
  - High data throughput
- Hierarchical global routing network:
  - Flexible global data transmission
  - External data access
  - Global cell (re)configuration
- AMBA 4 AXI4-stream protocol
- Single-Cycle-Per-Hop latency
- Data driven synchronization
- GALS network data transmission



Processing cell

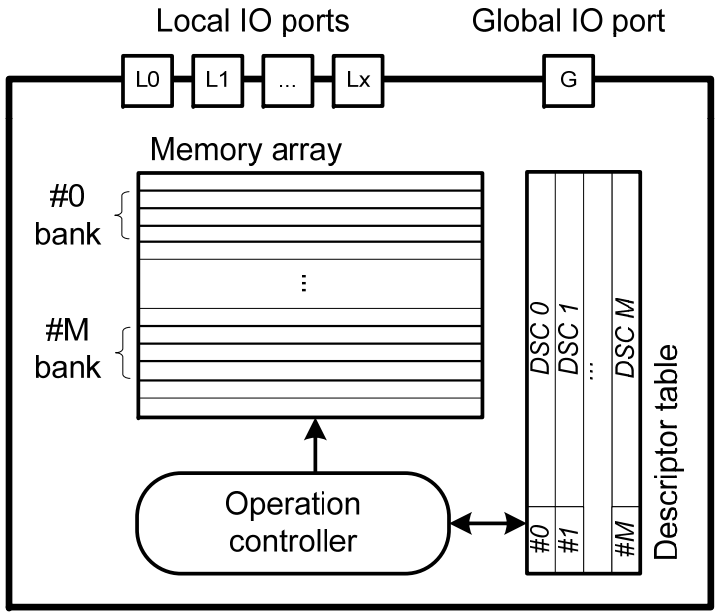


- Processing core
  - ALU, DSP, SIMD, VLIW, CORDIC...
  - Implicit load-store operations in all instructions.
  - Run-time control and conditional reconfiguration.
  - In-cell NoC supervision and reconfiguration.
- Processing shell
  - Network adapter

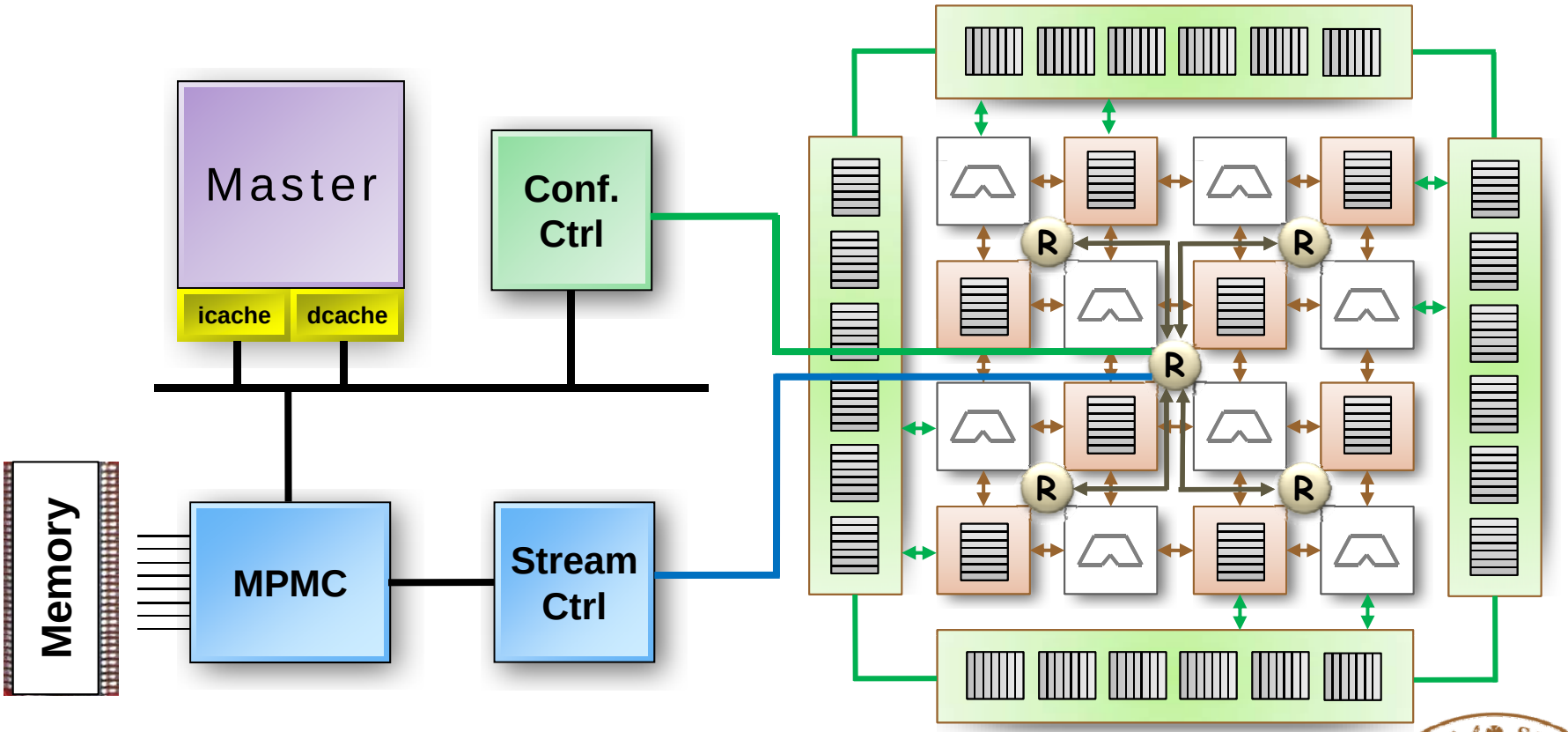


Memory cell

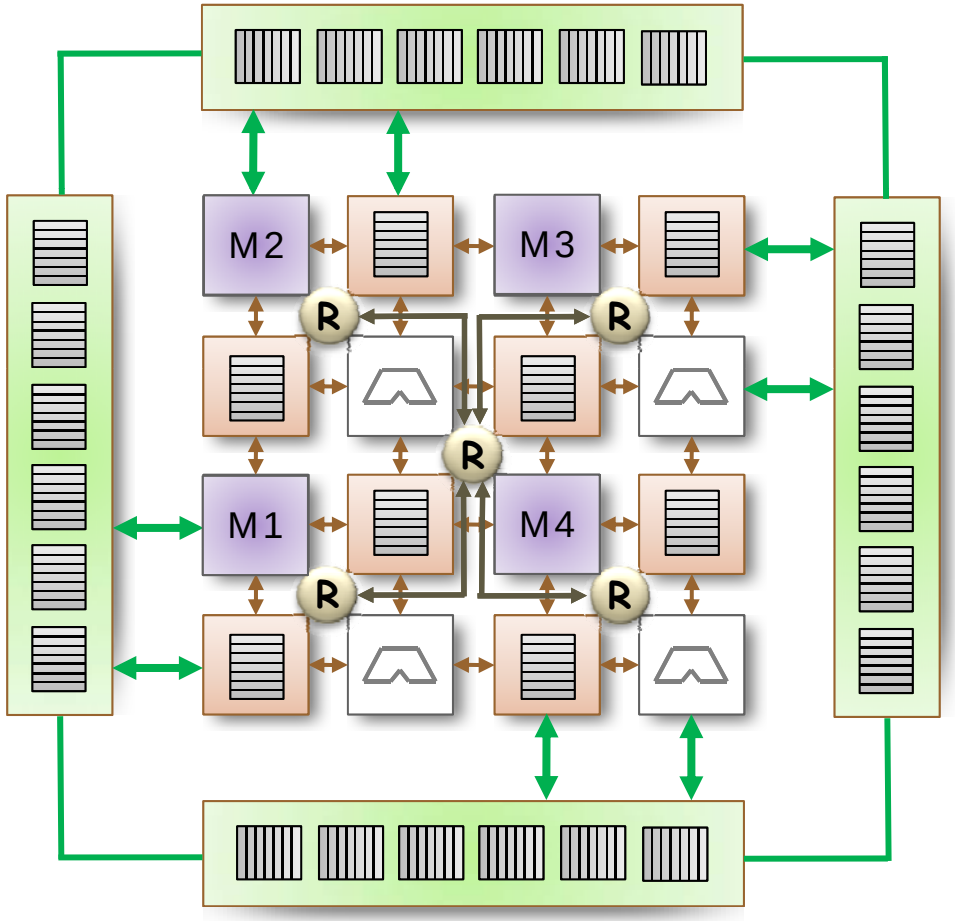
- Cell structure:
  - Divided into banks
  - Configurations and operations handled locally
- Operation mode: FIFO & RAM
- Run-time memory cell concatenation in FIFO mode.
- Blocking/Non-blocking execution.
- Programmable descriptor execution.
- Micro-block memory access.



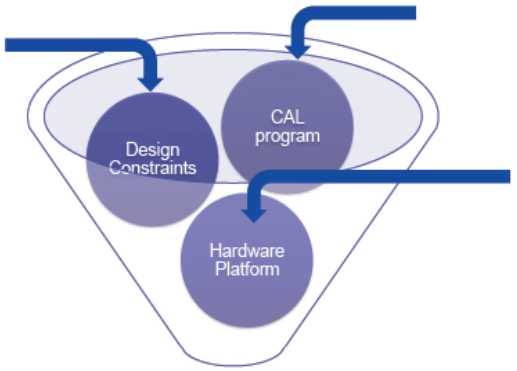
Static & Dynamic configuration (I)



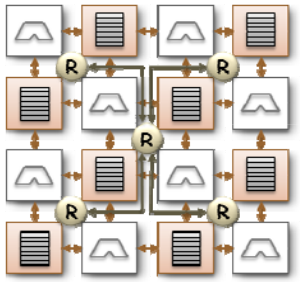
Static & Dynamic configuration (II)



Software development

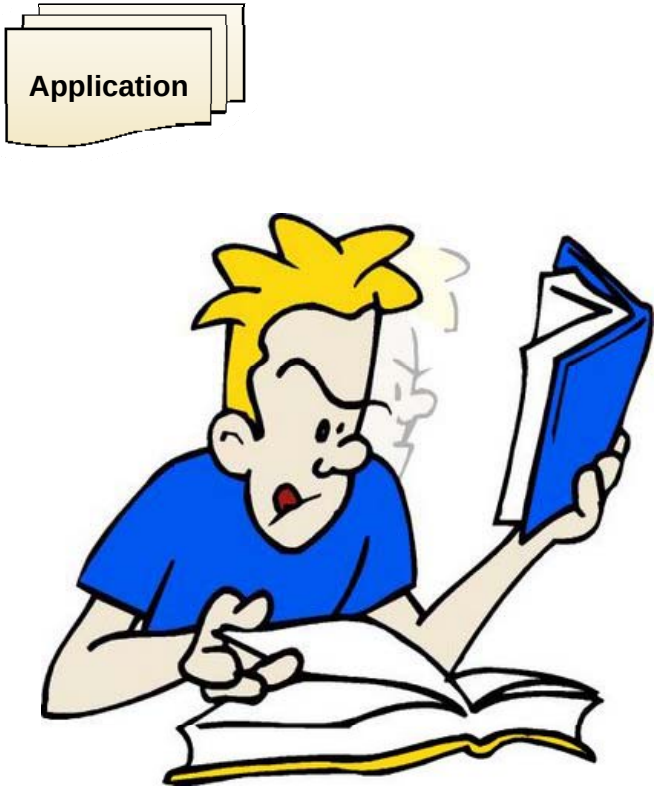


- Automated application mapping.
  - CAL dataflow language
  - Parallelism exploration
  - Within the HiPEC project together with CS dept.

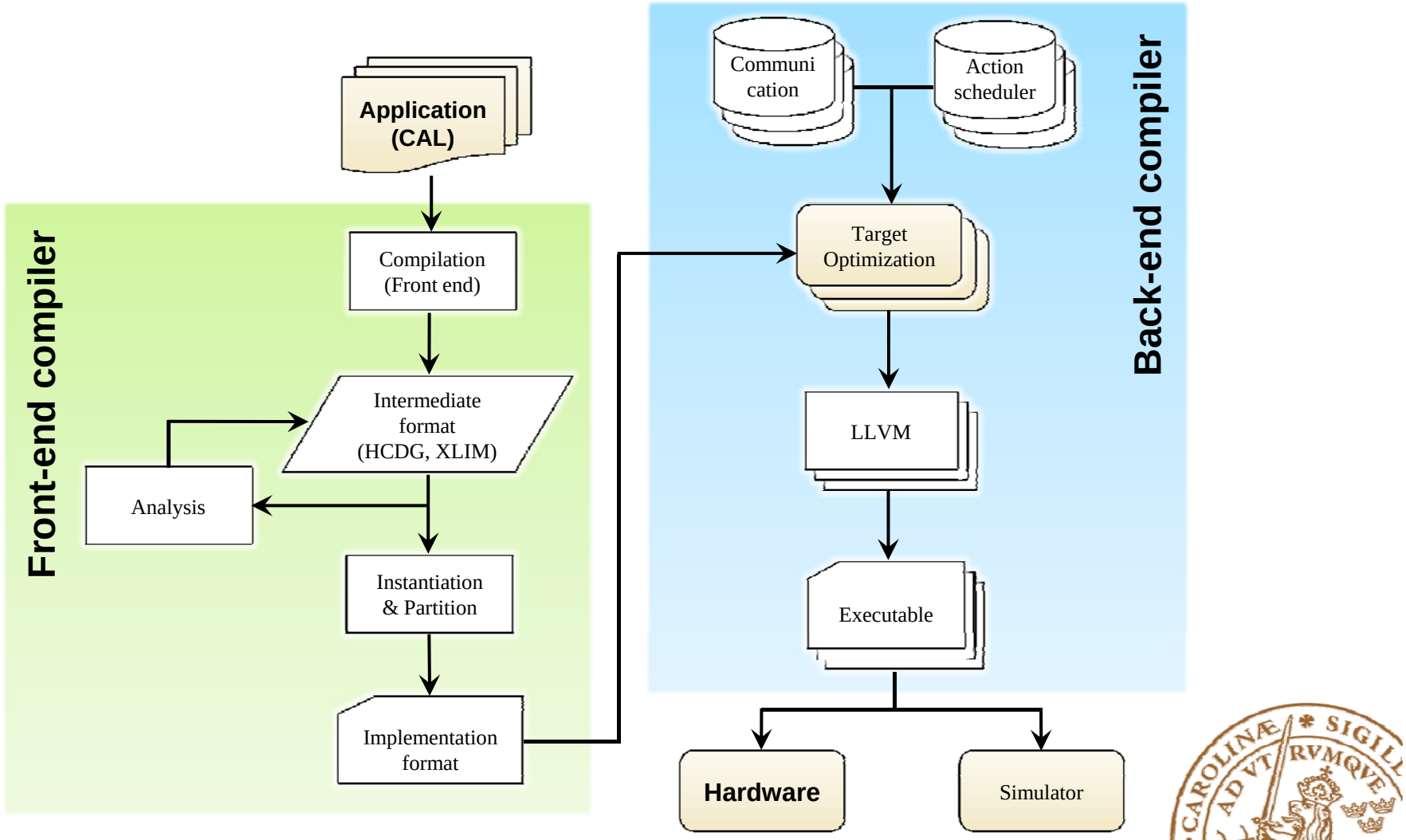


- Design exploration with SCENIC framework.
  - SystemC-based virtual platform
  - Explore system behavior and evaluate performance

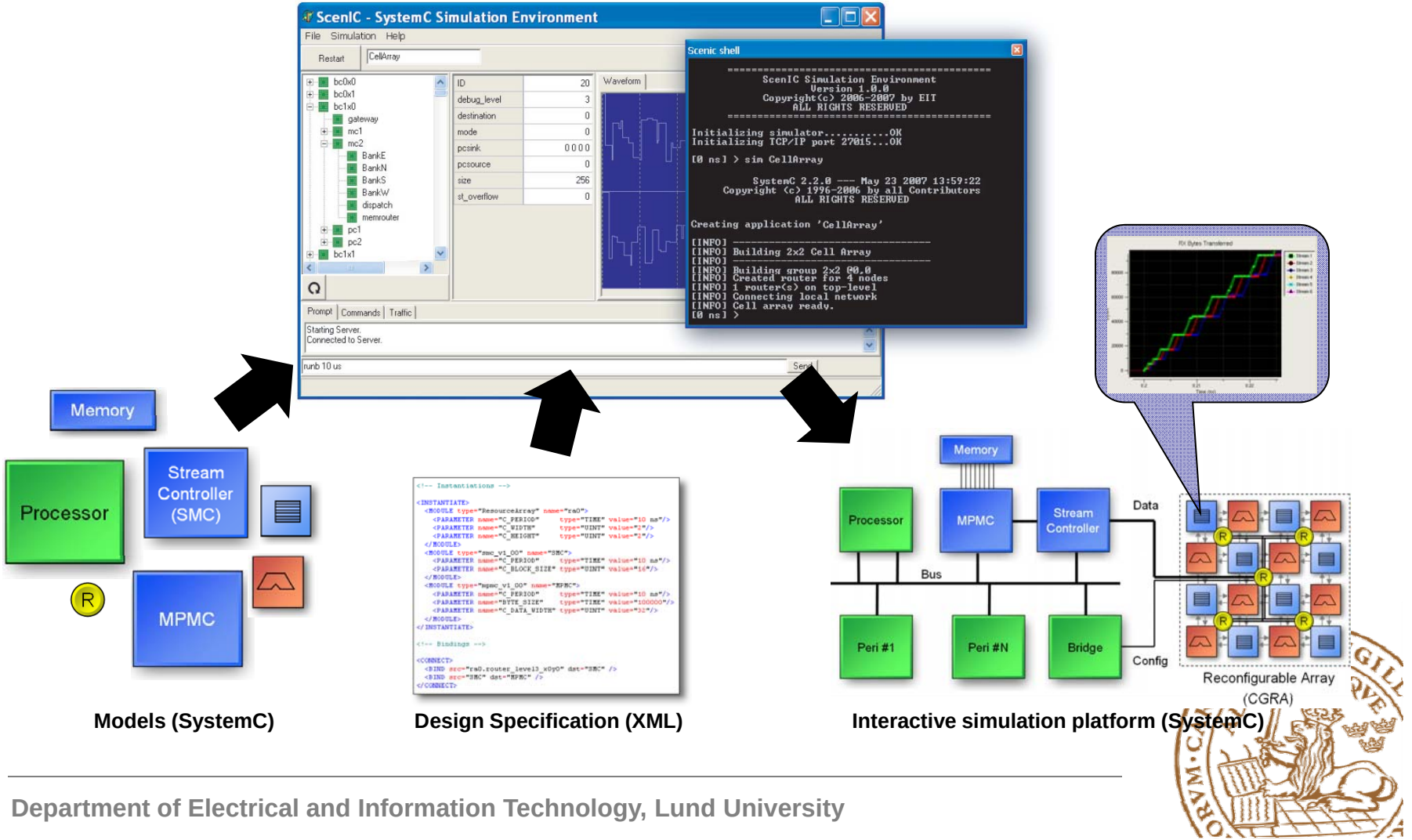
Application mapping



Application mapping from CAL



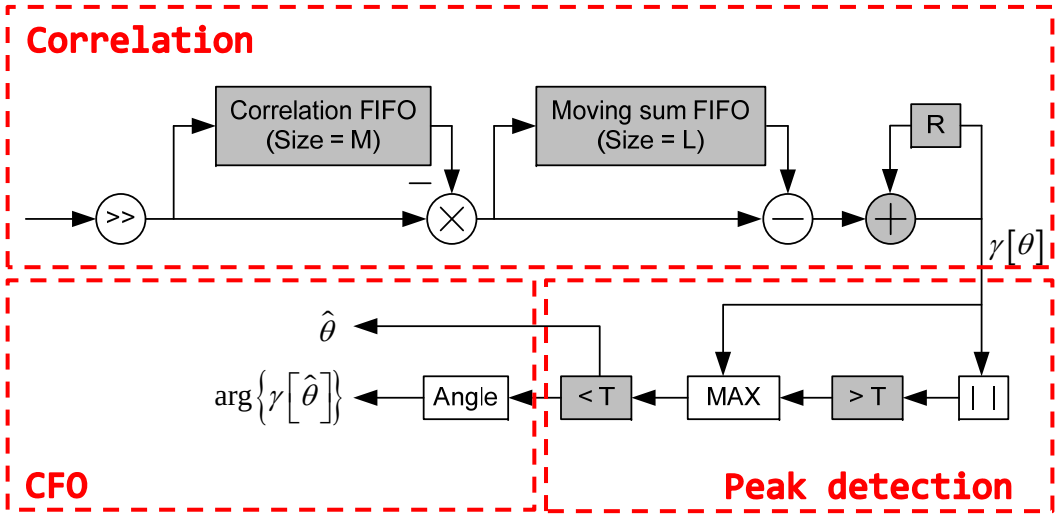
SCENIC – Design Exploration

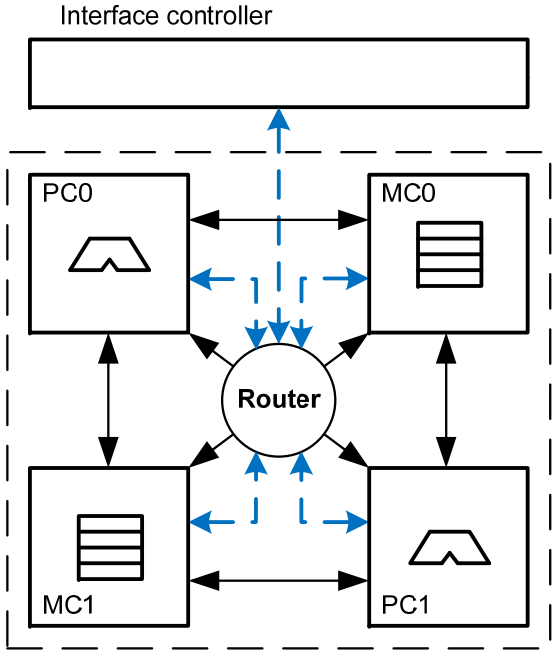


Models (SystemC) **Design Specification (XML)** **Interactive simulation platform (SystemC)**

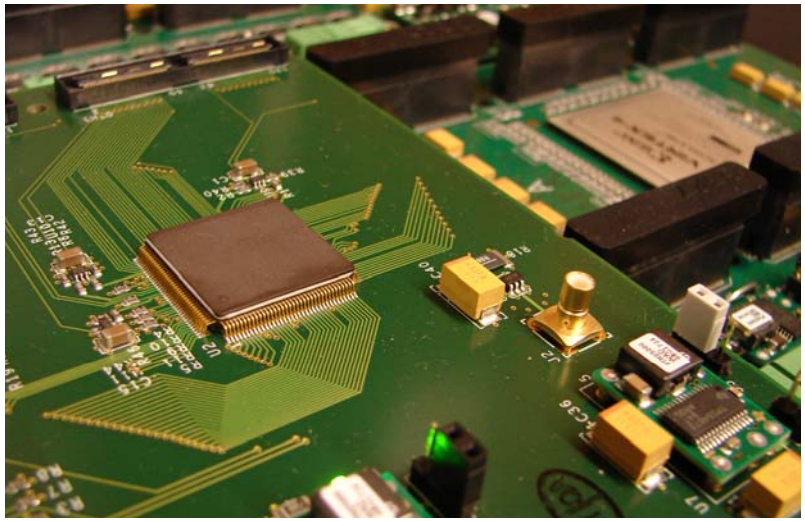
Case study: multi-standard OFDM synchronization

- Multiple wireless radio standards
- Concurrent data stream processing
- Coarse Time Synchronization
- Carrier Frequency Offset (CFO) estimation





Implementation results (I)



- 65 nm low-power regular VT CMOS:
  - Area: 0.479 mm^2
  - Clock frequency: 534 MHz

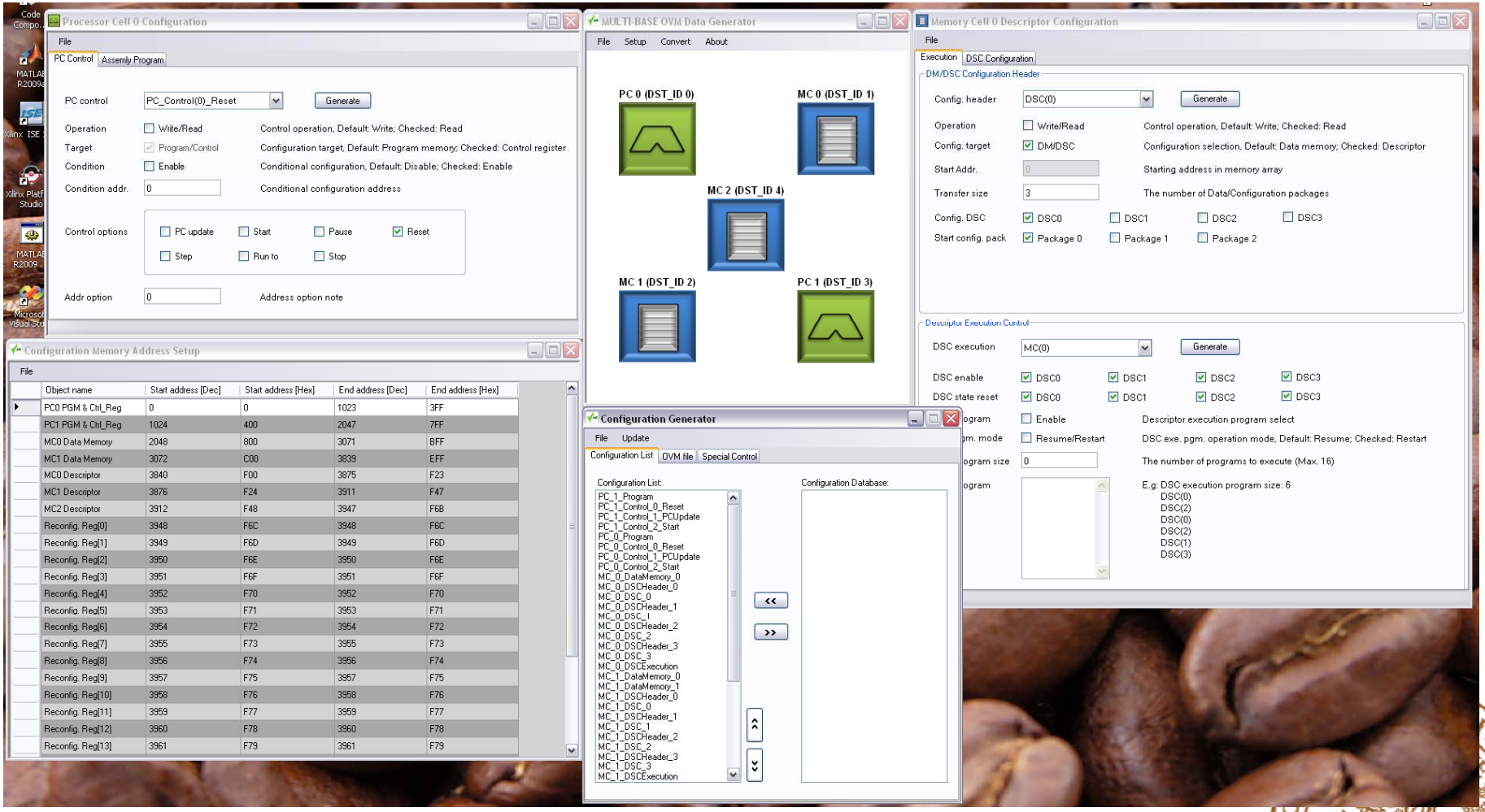
- Adaptive word length scheduling.
- Adoption of different algorithms, e.g. Novel sign-bit OFDM acquisition.

Concurrency	Standard	Quantization accuracy	Memory utilization
Single-Stream	802.11n	4 bits	08.48%
	LTE	4 bits	65.18%
	DVB-H 2K	4 bits	85.71%
	DVB-H 4K	2 or Sign bit	85.71%
	DVB-H 8K	Sign bit	85.71%
Dual-Stream	802.11n & 802.11n	4 or 2 bits	16.96%
	802.11n & LTE	2 bits	45.09%
	802.11n & DVB-H 2K	2 bits	65.63%
	LTE & LTE	2 bits	73.21%
	LTE & DVB-H 2K	2 bits	93.75%

Implementation results (II)

- Compare with ASIC solution, ~4 times more area cost.
- Case study does not explore the potential usage.
  - Simple algorithms
  - No task-level hardware sharing
- Currently looking at channel estimation & MIMO detection for LTE-A.
  - Task-level hardware sharing
  - Cooperation with the DARE project

Configuration generator



Conclusion

- Reconfigurable cell array enables hardware sharing at different levels, i.e., task-, function-, and algorithm-level.
- *Coarse-grained reconfigurable cell array* comprises distributed processing and memory cells, and a *hierarchical* NoC structure.
- In-cell *dynamic reconfiguration* enables fast context switching.
- Application mapping from CAL and design exploration with SCENIC tool.
- The system flexibility is illustrated by performing OFDM synchronization for multiple standards.

Thanks & Questions