Cellular Electronics – Baseband Processing

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Outline

- The team
- The researches
  - DFE: filtering for CA/sign-bit processing
  - Learning the channel: channel estimation for LTE
  - The matrix: matrix decomposition/inversion
  - Recovering the signal: multi-mode MIMO detection
  - Multi-task platform: reconfigurable cell array
  - Going faster than Nyqvist: chip measurement
- Conclusion

The Team - Digital ASIC


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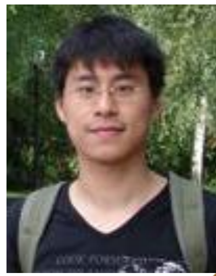
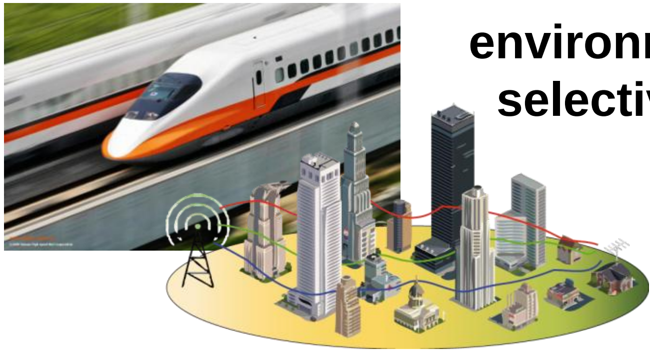

Ph.D. Stud.
Chenxin
Zhang

Research Motivations & Objective



environment selectivity

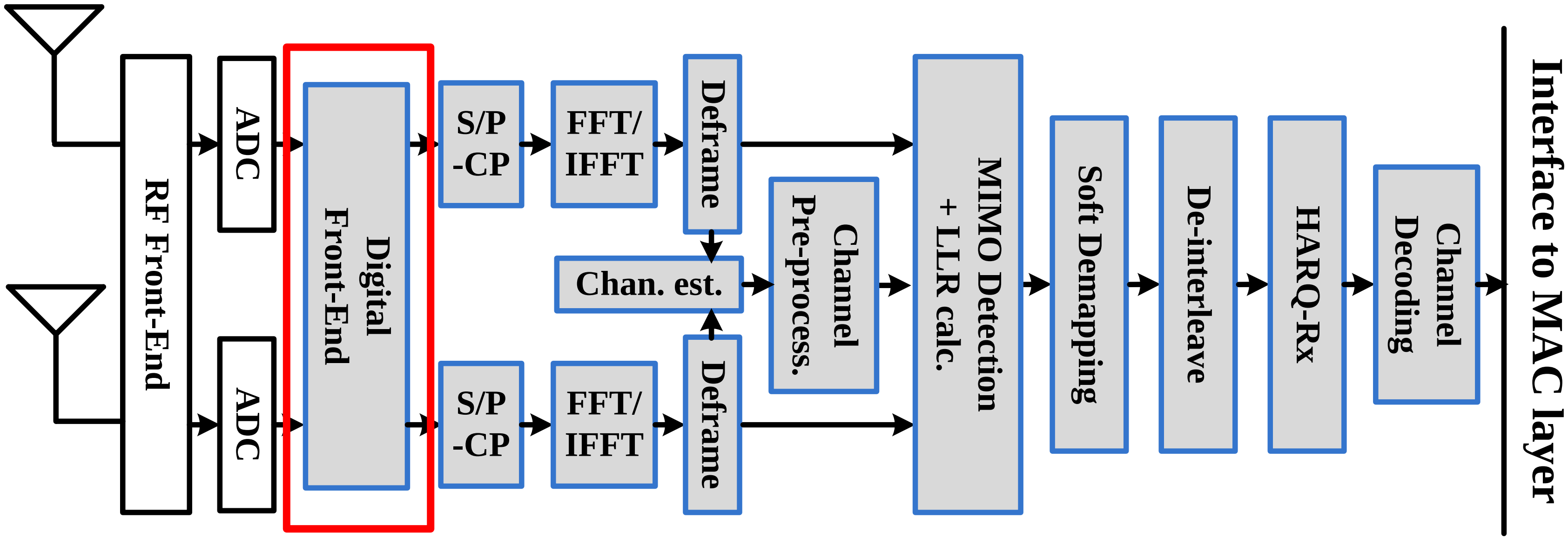
application selectivity

- Multi-standard
- Multi-mode
- Multi-task

- High-speed
- Low-power
- Low-cost

Our Focus: integrate the demands in an efficient hardware

DFE: Digital Front-End



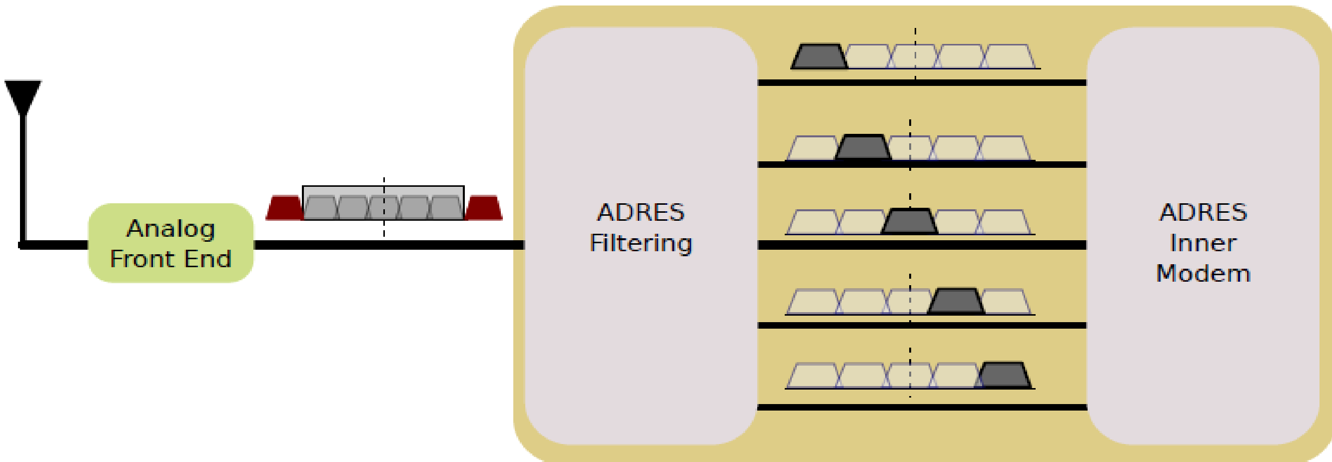
Isael Diaz

- Selective-channelization for LTE-A carrier aggregation (**together with IMEC**)

Channelization for LTE-A Carrier Aggregation

- LTE-A Carrier Aggregation
  - CA scenarios: intra-band continuous, intra/inter-band non-continuous
  - CC bandwidth: 1.4MHz (6RB)~20MHz (100RB)

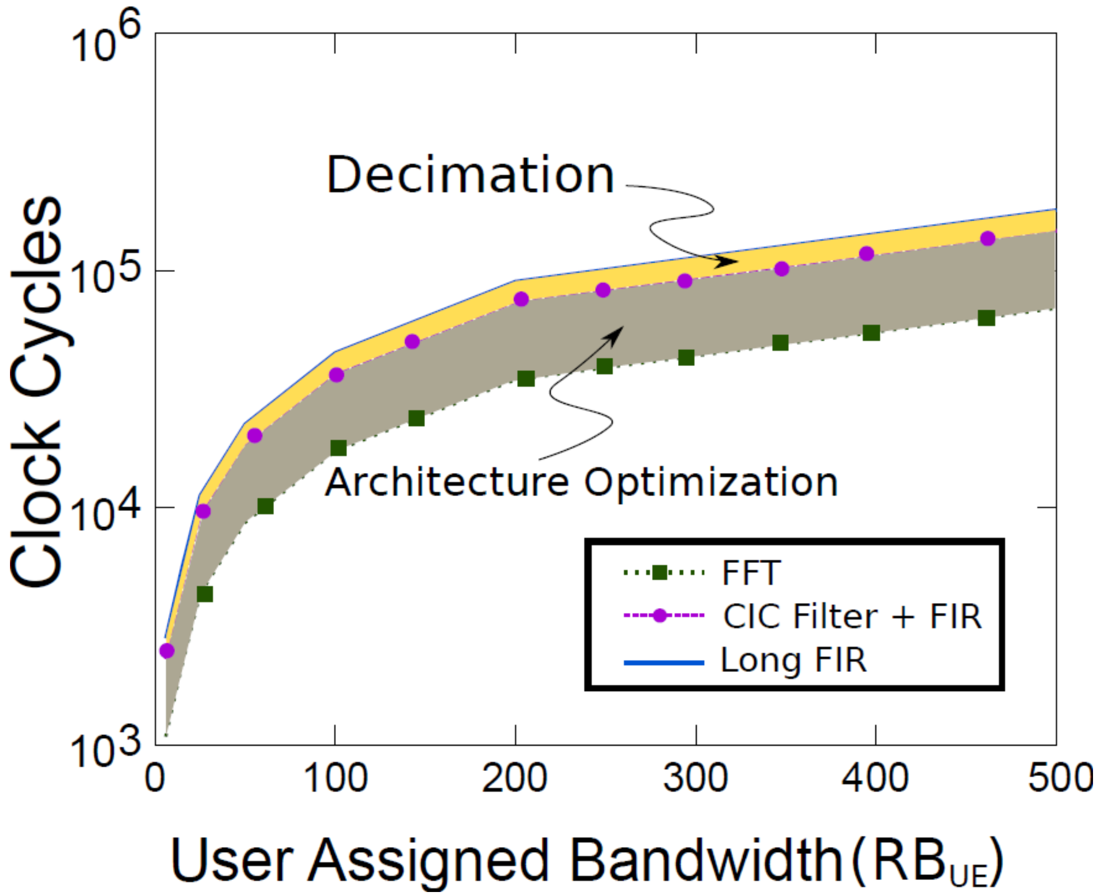
- Software Defined Radio as Potential Solution (ADRES)



FULL SDR FILTERING: ADRES Filtering + ADRES Inner modem

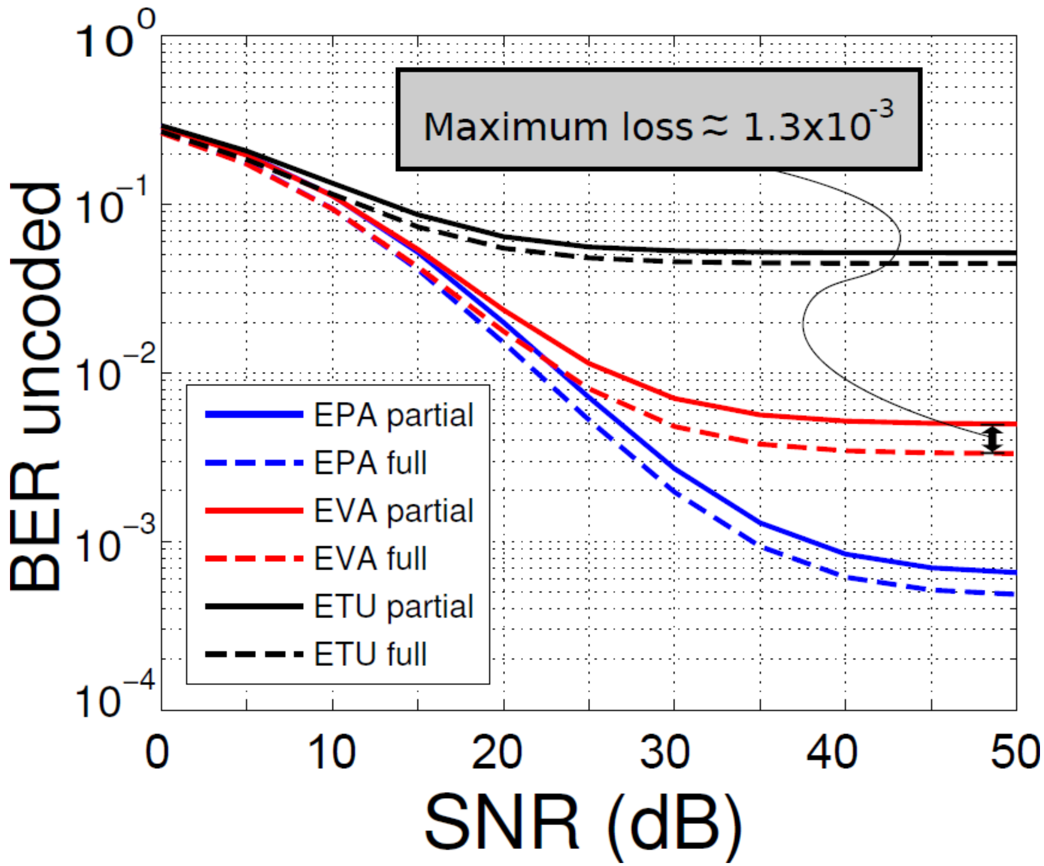
Filtering Methods

- Candidate filtering method: Long FIR Filter/CIC+FIR Filter/FFT
- Power analysis (on ADRES)
  - Clock cycles as metric
  - FFT is the best due to architectural optimization



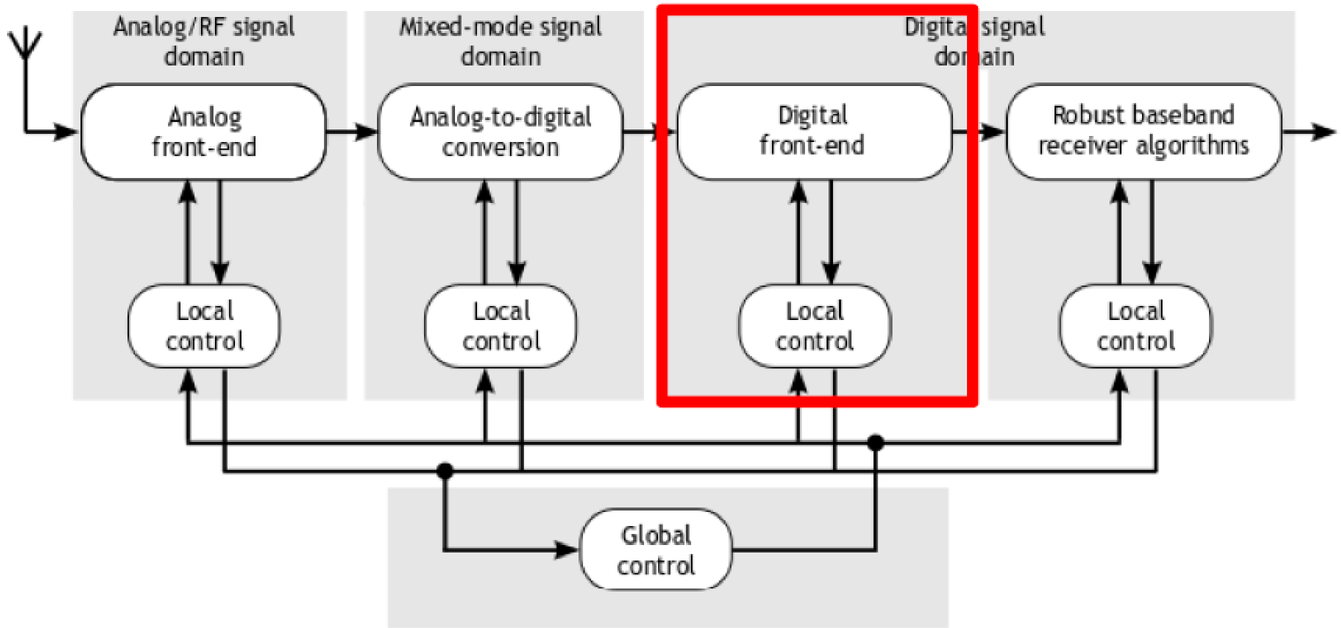
Performance Analysis

- Channelization schemes
  - ***Partial filtering***: only the user assigned bandwidth is extracted
  - ***Full filtering***: the entire transmission bandwidth is extracted



- Performance analysis
  - EPA (2km/h), EVA (30km/h), ETU(130km/h)
  - Marginal performance loss due to CE error
  - Complexity saving is up to 70%

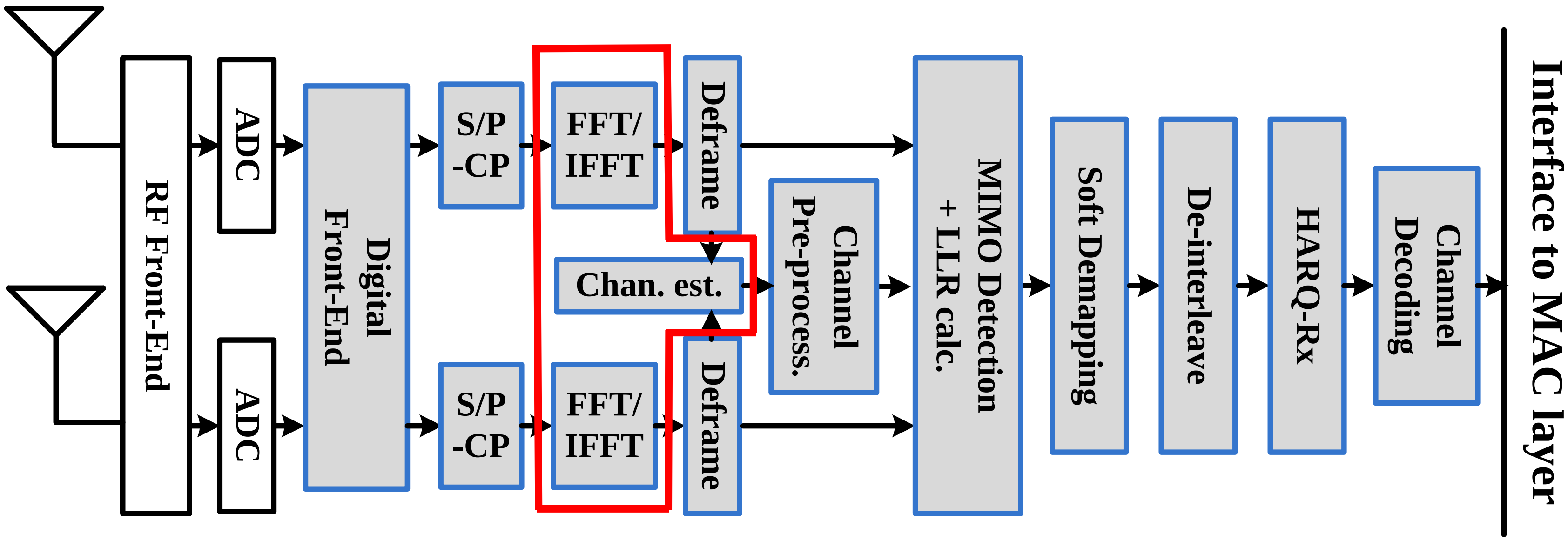
Continue DFE in DARE



Michal Stala **Isael Diaz**

- ➢ Imperfections with carrier aggregation
- ➢ Scalable DFE for both high-end LTE devices and low-end M2M devices
- ➢ Together with Ericsson

Channel Estimation

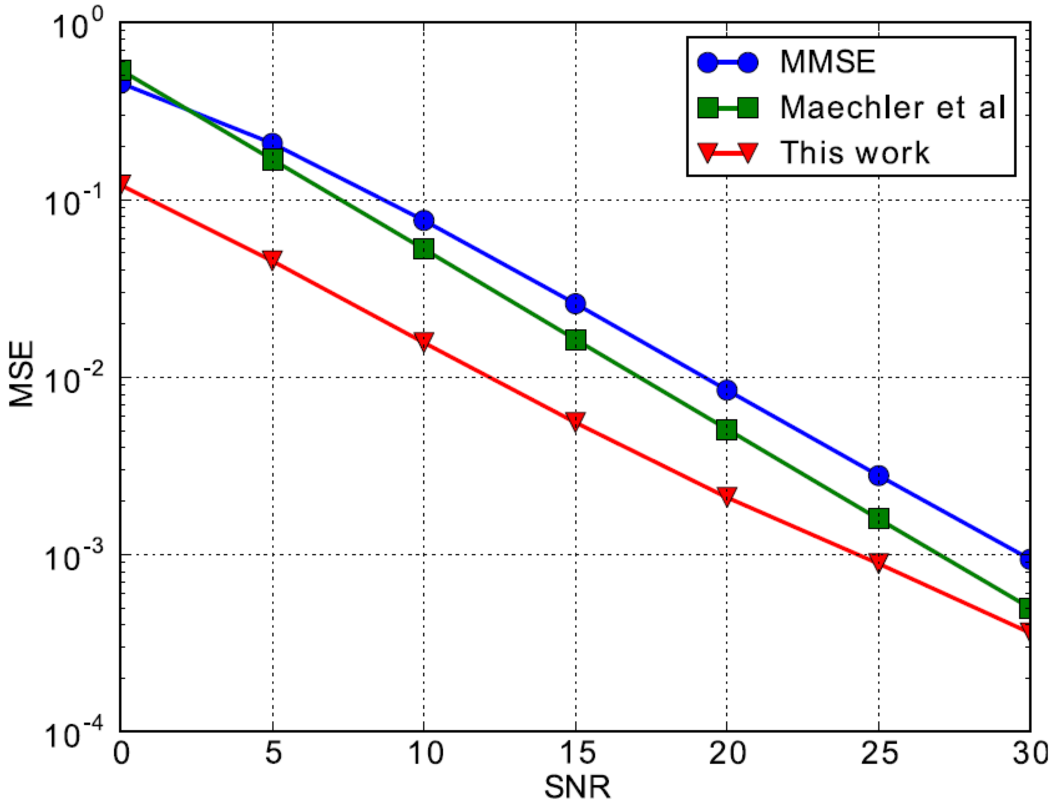


Johan Löfgren

- Improved matching pursuit for LTE channel estimation **(results update from LCDWS 2011)**

Improved Matching-Pursuit for LTE CE

- MP with three modifications:
  - L^1-norm energy calculation, SNR-depended stopping scheme, and smartly increased system resolution
- Better performance than frequency-domain MMSE and original MP

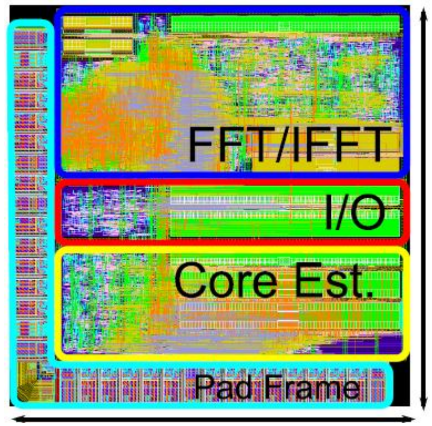


Hardware Implementation Results

- ST 65nm CMOS including FFT/IFFT & core estimator
- Better accuracy with compatible hardware & higher speed

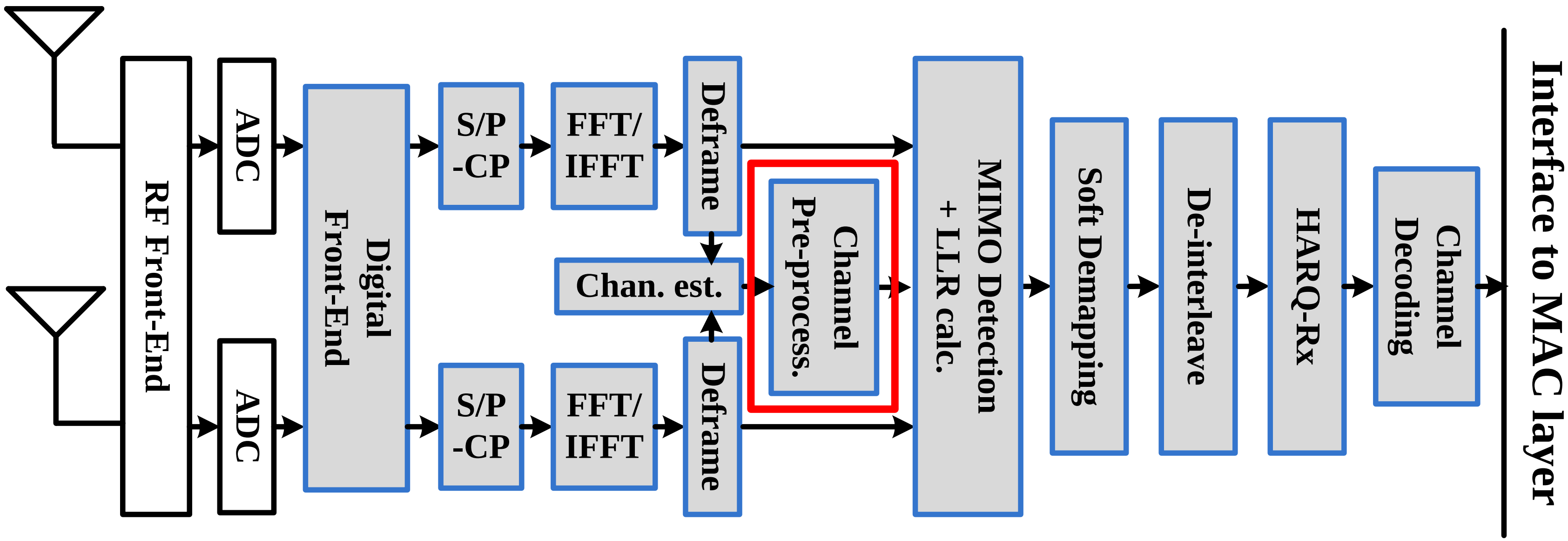
	This work	[9]	[22]
Technology [nm]	65	180	65
Area [mm²]	0.13/0.29(1)	1	0.1
Norm. Area [mm²]	0.13/0.29(1)	0.13	0.1
Frequency [MHz]	125	154	200
Init. [us]	7.62	336	N/A
Update [us]	0.62	3.62	N/A
Estimates in 1ms	10.3	1.6	8

(1) Without/With FFT/IFFT



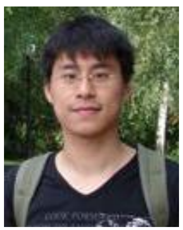
[9] P. Maechler, et.al., "Matching pursuit: evaluation and implementation for LTE channel estimation," *IEEE ISCAS, May 2010.*
[22] M. Simko, et.al., "Implementation aspects of channel estimation for 3gpp LTE terminals," *European Wireless Conference, April 2011*

Energy-Efficient Channel Pre-Processing



Rakesh Gangarajaiah

- Link-adaptive QR-decomposition using Householder transformations



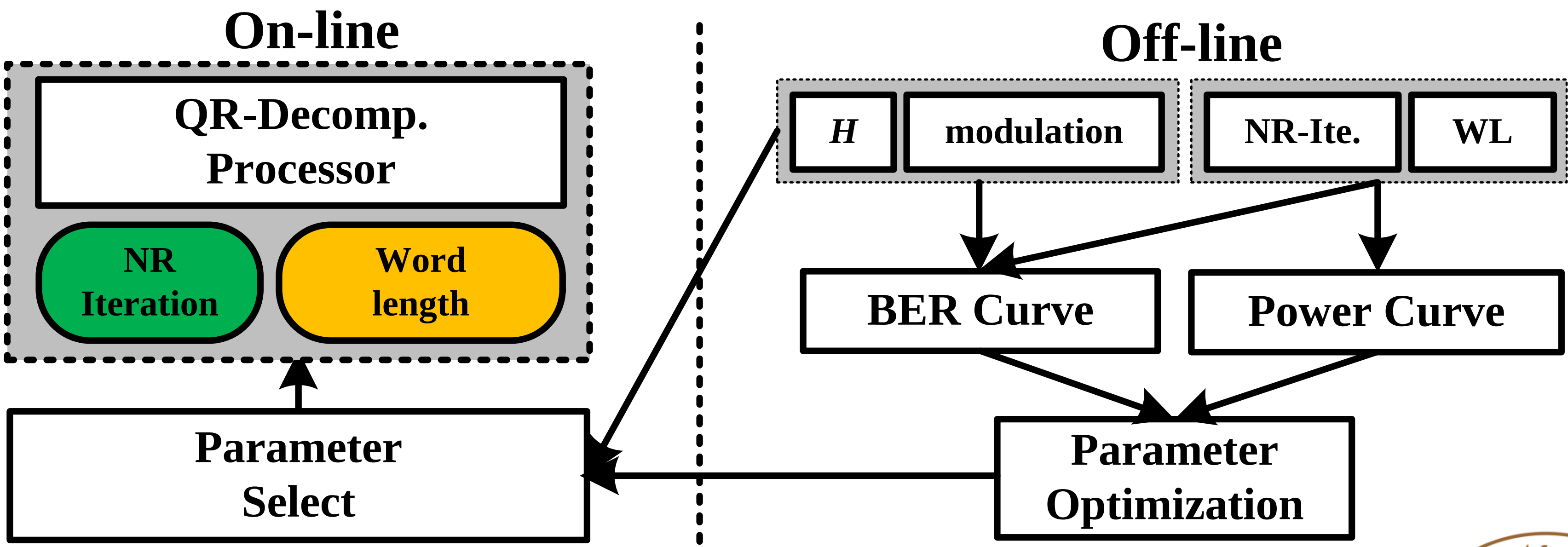
Chenxin Zhang

Hemant Prabhu

- Energy efficient channel pre-processor using partial update scheme

Link-Adaptive QR-Decomposition

- ***Basic idea***: dynamically adjust parameters *energy-efficient* mode according to ***H*** and *modulation scheme*, with constraint: *BER* requirement is satisfied
- Parameters:
  - Newton-Rhapson ***iteration number***
  - ***Word-length*** of the processor



Power Reduction Using Partial Channel Update

- Full channel update (complete QRD)
  - Needed to track channel change
  - Expensive in terms of power

	QRD-1 (TCAS1-11)	MIMOD-1 (ISSCC-09)
Gate Count	**111K**	114K
Throughput (SC/s)	12.5M	28.125M
Energy (nJ/SC/s)	**12.76**	5.37

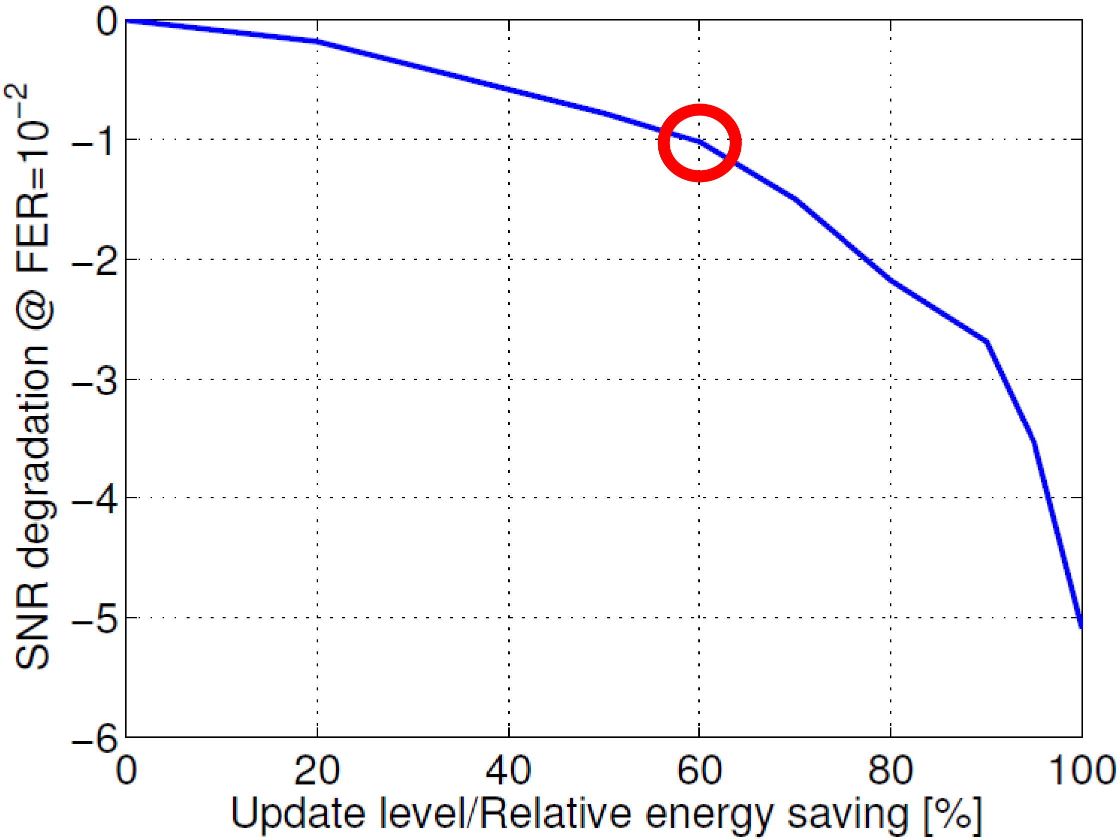
- Partial channel update (approximated QRD)
  - Only upper triangular ***R*** is updated as:

$$\hat{\boldsymbol{R}}'_i = \boldsymbol{Q}^H_{i-t}\boldsymbol{H}_i$$

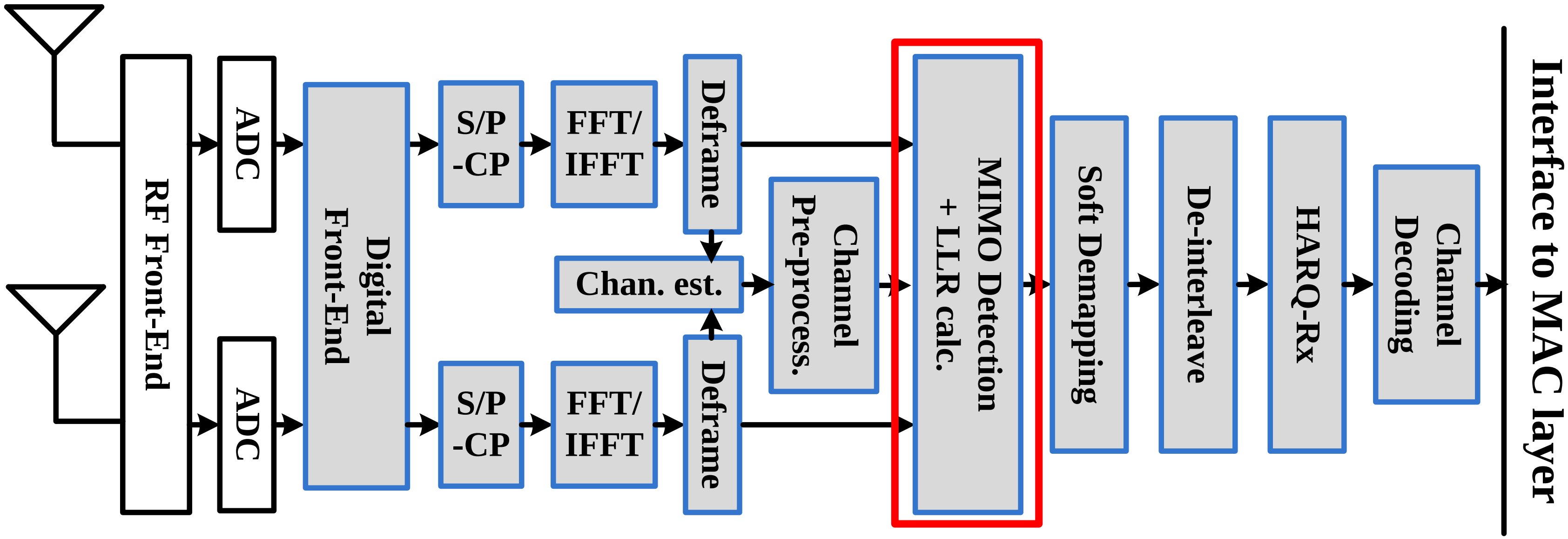
  - Dynamically switch between full and partial update according to time-correlation; full update in low-correlated channel

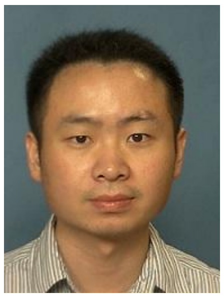
Performance Evaluation

- LTE downlink with 4×4 64-QAM MIMO under EVA-70 channel
- Performance-power tradeoff by adjusting patial update ratio
- Saving 60% power with 1dB performance loss



MIMO Detection



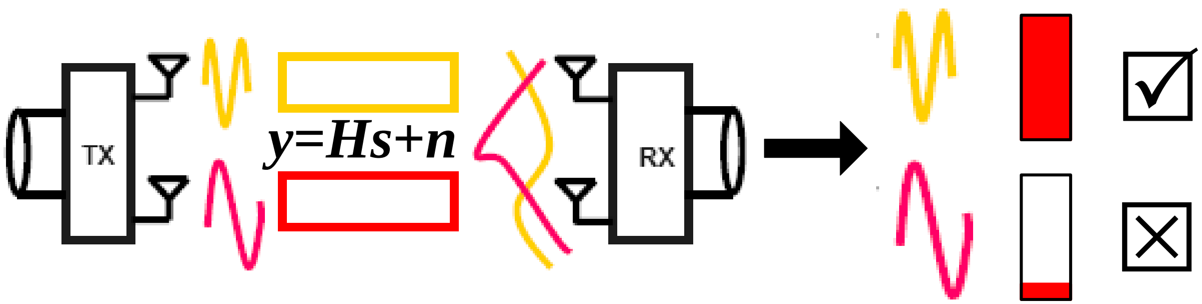


Liang Liu

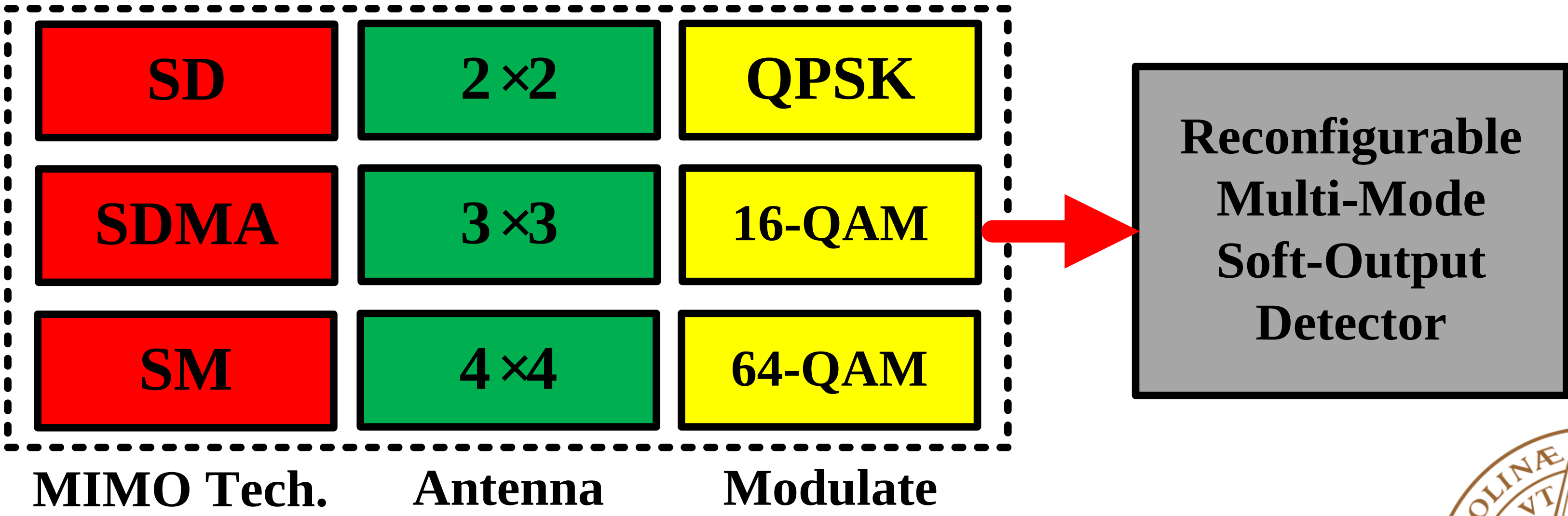
- Multi-mode MIMO signal detection with soft-output

Multi-Mode Soft-Output MIMO Detection

- Soft-output MIMO detection



- Multi-mode MIMO detector



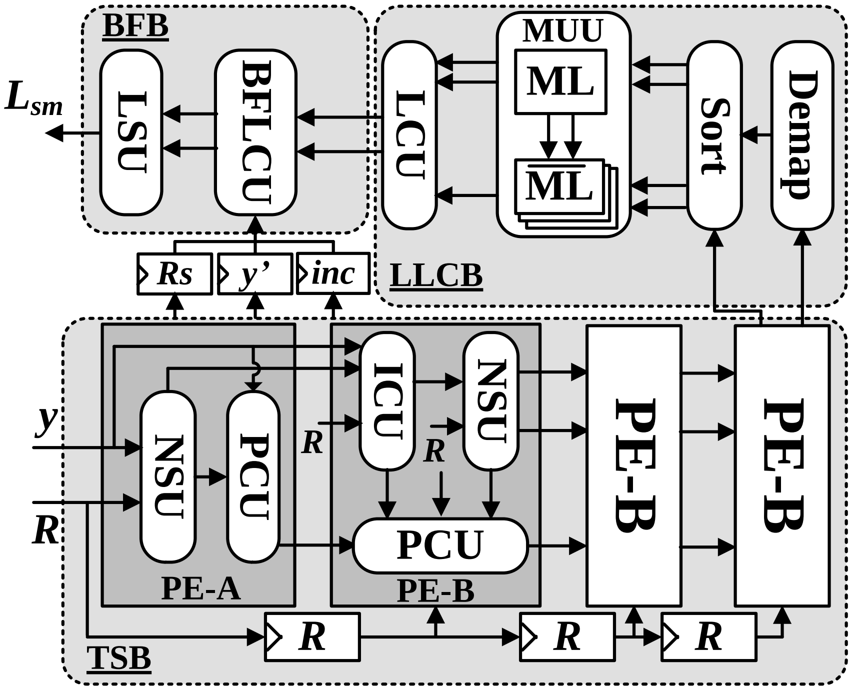
MIMO Techniques – Unified Algorithm

- Algorithms share most of the operations
  - ***SM***: FSD tree-search with bit-flipping
  - ***SDMA***: FSD tree-search with detection reordering
  - ***SD***: Real-valued MAP decoder using bit-flipping

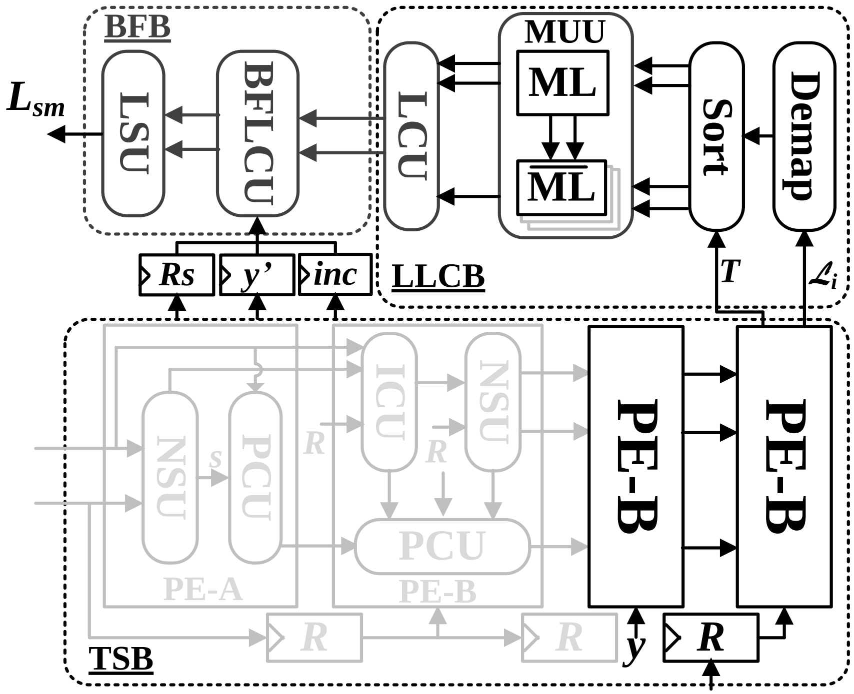
Operations		**MIMO Techniques**		
		SM	**SDMA**	**SD**
Pre Proc.	H decomp.	☑	☑	☑
	H permut.	☑	☑	
tree search	Node selection	☑	☑	☑
	Interf. cancel	☑	☑	
	Euclidean distance	☑	☑	☑
LLR calc.	Sorter	☑	☑	
	List LLR calc.	☑	☑	
Bit-flipping		☑		☑

Antenna Configurations – Scalable Architecture

- Example: SM detector
  - TSB: Activate different stages according to antenna configuration
  - LLCB/BFB: Close half of the LLR/BFB calculation units



4×4 Mode



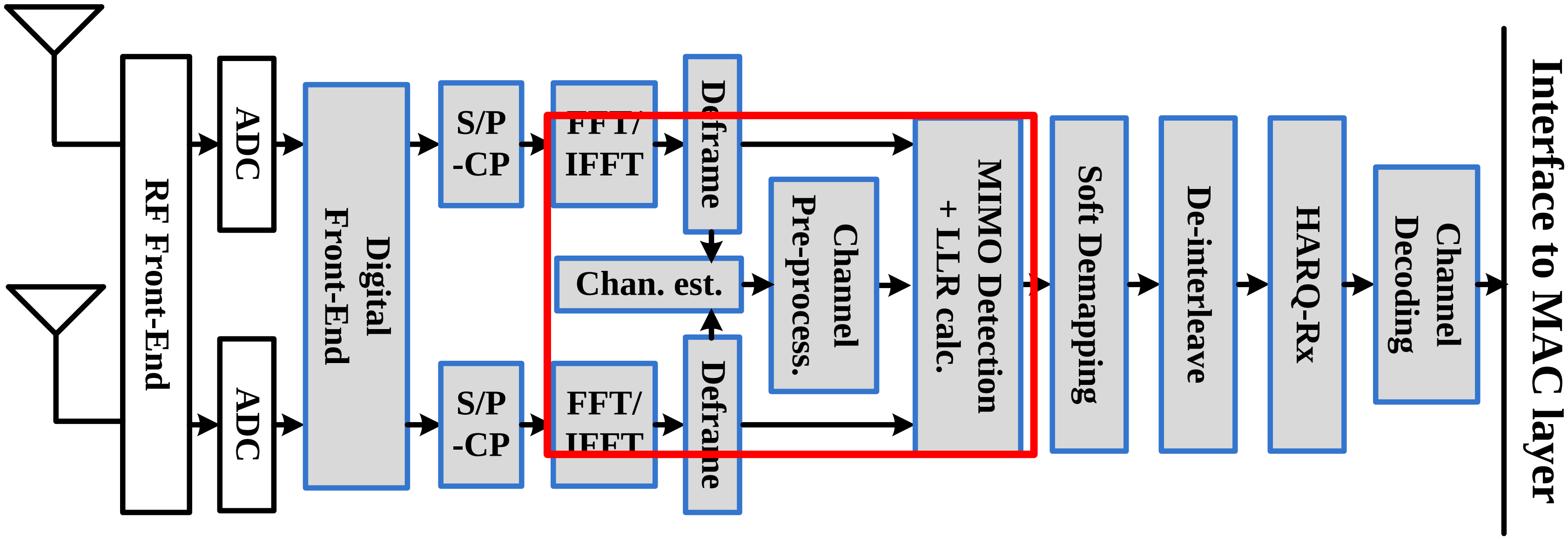
2×2 Mode

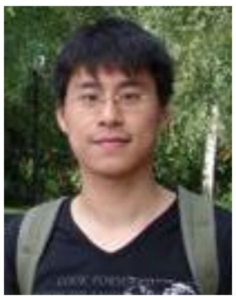
Results

- Post-layout results with ST 65nm CMOS technology
- Supports the most MIMO modes
- Consumes the least hardware and energy

	TVLSI' 07	TVLSI' 11	JSSC' 12	ISCAS' 10	This Work
MIMO Modes	SM	SM	SM	SM	SM/SD/SDMA
Antenna Size	4×4	4×4	4×4	4×4	4×4
Modulation	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM
Algorithm	Soft-output K-best	Soft-output best-first	SISO MMSE-PIC	Soft-output K-best	Early-pruned FSD with bit-flip
Process Technology	0.13 μm	65 nm	90 nm	65 nm	65 nm
Max. Clock Rate	270 MHz	333 MHz	568 MHz	833 MHz	167 MHz
Throughput	8.57 Mb/s	83.3 Mb/s	757 Mb/s	2 Gb/s	1 Gb/s
Core Area	2.38 mm^2	N/A [2]	1.5 mm^2	0.57 mm^2	0.25 mm^2
Gate Count	280 kG[a]	64 kG[a]	410 kG[b]/160 kG[a]	298 kG[a]	83.7 kG[a]
Hardware Efficiency kG/(Mb/s)	32.67 [a]	0.77 [a]	0.21 [a]	0.15 [a]	0.084 [a]
Power Consumption	94 mW @ 1.2 V	11.5 mW @ 1.0 V	189.1 mW @ 1.2 V	280 mW @ 1.3 V	59.3 mW @ 1.2 V (SM mode)
Normalized Power Consumption	N/A	16.6 mW	136.6 mW	238.6 mW	59.3 mW
Normalized Energy Consumption	N/A	199.2 pJ/bit	180.4 pJ/bit	119.3 pJ/bit	59.3 pJ/bit

Reconfigurable Cell Array (RCA)





Chenxin Zhang

- Mapping channel estimation, QRD, and MIMO detection in LTE-A on a reconfigurable platform

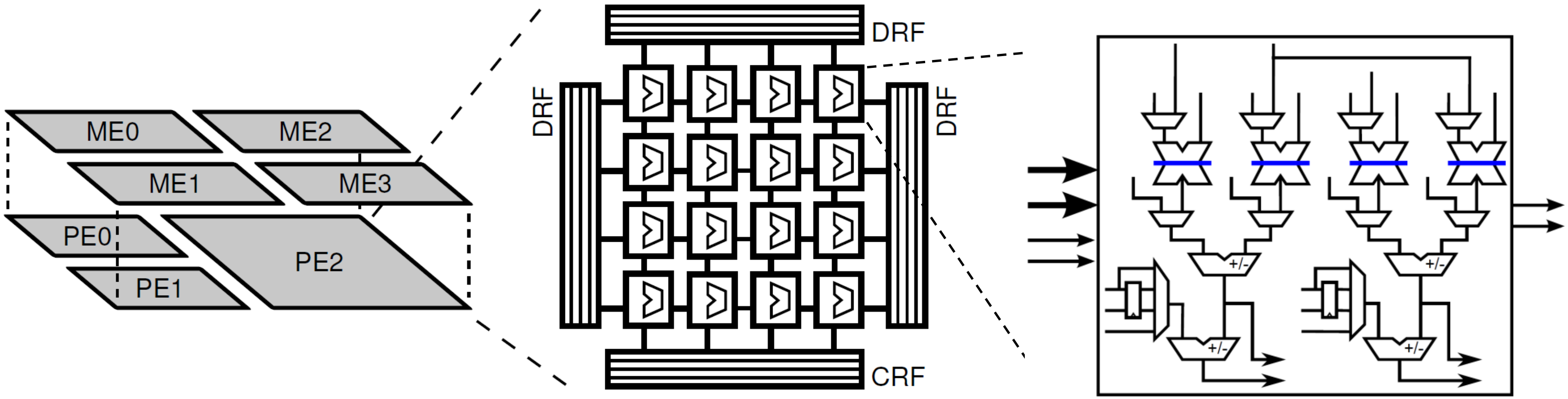
Algorithms

- Operations push to vector-level
  - Improve data parallelism and instruction parallelism
  - Easily mapped to vector processor with high hardware utilization
- Algorithms
  - Channel estimation: Robust MMSE with sliding window
  - QRD: Sorted-QRD using modified Gram–Schmidt processing
  - MIMO detection: MMSE with node perturbation

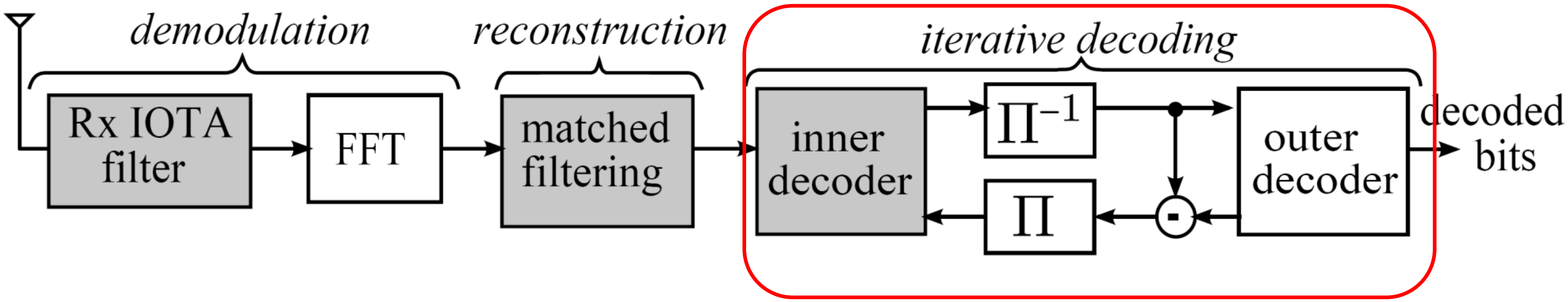
Mathematical operations		Ch. Est.	Ch. Pre-proc.	Signal Det.
Vector Opt.	Vector-vector	☑	☑	☑
	Scalar-vector		☑	
	Matrix-vector			☑
	Vector permutation		☑	
Scalar Opt.	SQRT/DIV		☑	
	Node selection			☑

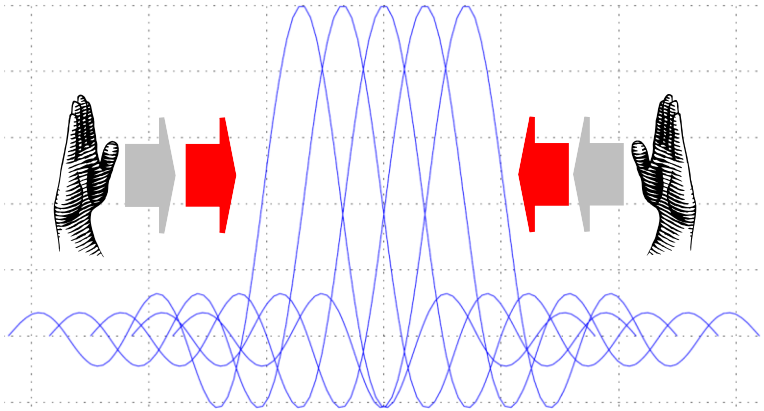
Platform

- Heterogeneous cell array with vector operation
  - ***RISC elements*** (PE0, PE1): task scheduling, cell configuration, and conditional & scalar operations.
  - ***Multiple memory banks***: to improve bandwidth and access flexibility
  - ***Dataflow processor PE2*** (DPE): 2D FUs for vector-based operations.



Faster Than Nyqvist Signaling



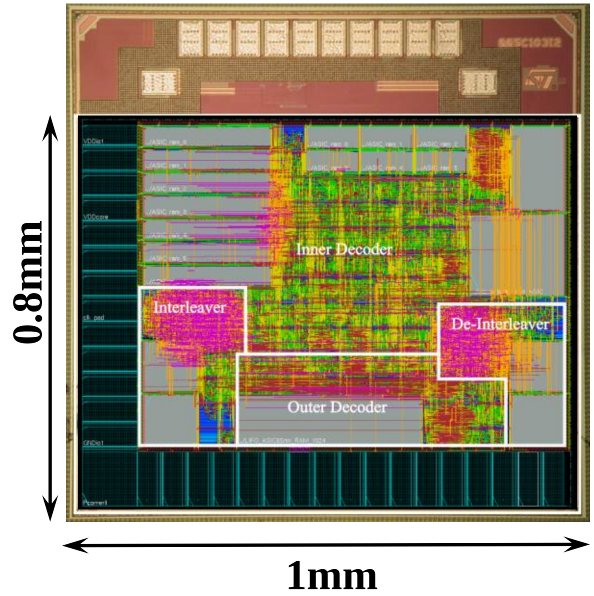


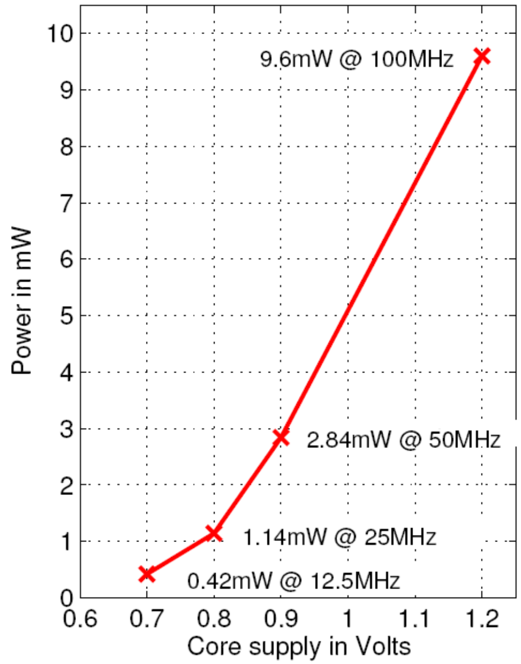
Deepak Dasalukunte

➢ Iterative decoder for multi-carrier faster than Nyqvist system (**measurement result update from LCDWS2011**)

Chip Measurement Results

Tech.	ST 65nm CMOS
Die Area	0.8 mm^2
Gate Count	250k
Total memory	14.68kB
IO & core supply	1.8v & 1.2v
Throughput	1Mbps@8 iter
Power	9.6mW
Energy	6nJ/sym/iter





FTN is a Practical Technique

- Lack of existing hardware implementations for FTN decoder
- To see how FTN decoder fits into exsting systems by referring a reconfigurable FFT and a Turbo decoder in 65nm CMOS

Functionality	FTN iterative decoder	128-2048 point FFT	3GPP LTE Turbo Decoder
	ESSCIRC 2012	*JSSC 2012*	*DATE 2010*
Technology	65nm	65nm	65nm
Core Area	0.567 mm^2	1.375 mm^2	2.1 mm^2
Gate count	250k	1100k	-
Total Memory	14.68kB	6.14kB	54% of area
Power	9.6mW (@ 1.2V, 100MHz)	4.05mW (@ 0.45V, 20MHz)	300mW (@ 1.1V, 300MHz)

Publications (2011-Present)

Journal

[1] ‘Hardware architecture of IOTA pulse shaping filters for multicarrier systems’, *IEEE TCAS-I*
[2] ‘Area-efficient configurable high-throughput signal detector supporting multiple MIMO modes’, *IEEE TCAS-I*.
[3] ‘Low complexity likelihood information generation for spatial-multiplexing MIMO signal detection’, *IEEE TVT*
[4] ‘Multicarrier faster-than-Nyquist transceivers: hardware architecture and performance analysis’, *IEEE TCAS-I*

Conference

[5] ‘Mapping channel estimation and mimo detection in lte-advanced on a reconfigurable cell array’, *IEEE ISCAS*
[6] ‘A unified multi-mode MIMO detector with soft-output’, *IEEE ISCAS*
[7] ‘A 0.8 mm2 9.6 mW implementation of a multicarrier faster-than-nyquist signaling iterative decoder in 65nm CMOS’, *IEEE ESSCIRC*
[8] ‘Reconfigurable cell array for concurrent support of multiple radio standards by flexible mapping’, *IEEE ISCAS*
[9] ‘Detecting multi-mode MIMO signals: algorithm and architecture design’, *IEEE ISCAS*
[10] ‘Improved matching pursuit algorithm and architecture for LTE channel estimation’, *IEEE ISCAS*
[11] ‘Analysis of a novel low complex SNR estimation technique for OFDM systems’, *IEEE WCNC*
[12] ‘Highly scalable implementation of a robust MMSE channel estimator for OFDM multi-standard environment’, *IEEE WSPS*
[13] ‘Low complexity soft-output signal detector for spatial-multiplexing MIMO system’, *IEEE PIMRC*
[14] ‘Unified multi-mode signal detector for LTE-A downlink MIMO system’, *APSIPA- ASC*
[15] ‘Design and implementation of iterative decoder for faster-than-Nyquist signaling multicarrier systems’, *IEEE ISVLSI*
[16] ‘Improved memory architecture for multicarrier faster-than-Nyquist iterative decoder’, *IEEE ISVLSI*
[17] ‘Complexity analysis of IOTA filter architectures in Faster-than-Nyquist multicarrier systems’, *IEEE NORCHIP*
[18] ‘On hardware implementation of radix 3 and radix 5 FFT kernels for LTE systems’, *IEEE NORCHIP*

Conclusions

- Support multi-standard, multi-mode, and multi-task
- High-speed, good performance with energy & area-efficiency
- Co-optimize system schedule, algorithm, and hardware
- Link-adaptive signal processing
- Scalable ASICs & reconfigurable cell array
- LTE/LTE-A as driving applications
- Post-layout simulation & chip measurement

Posters