Beating Moore's Law with the All Programmable SOC aka FPGA

Ivo Bolsens,
Senior Vice President & CTO

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Moore's Law

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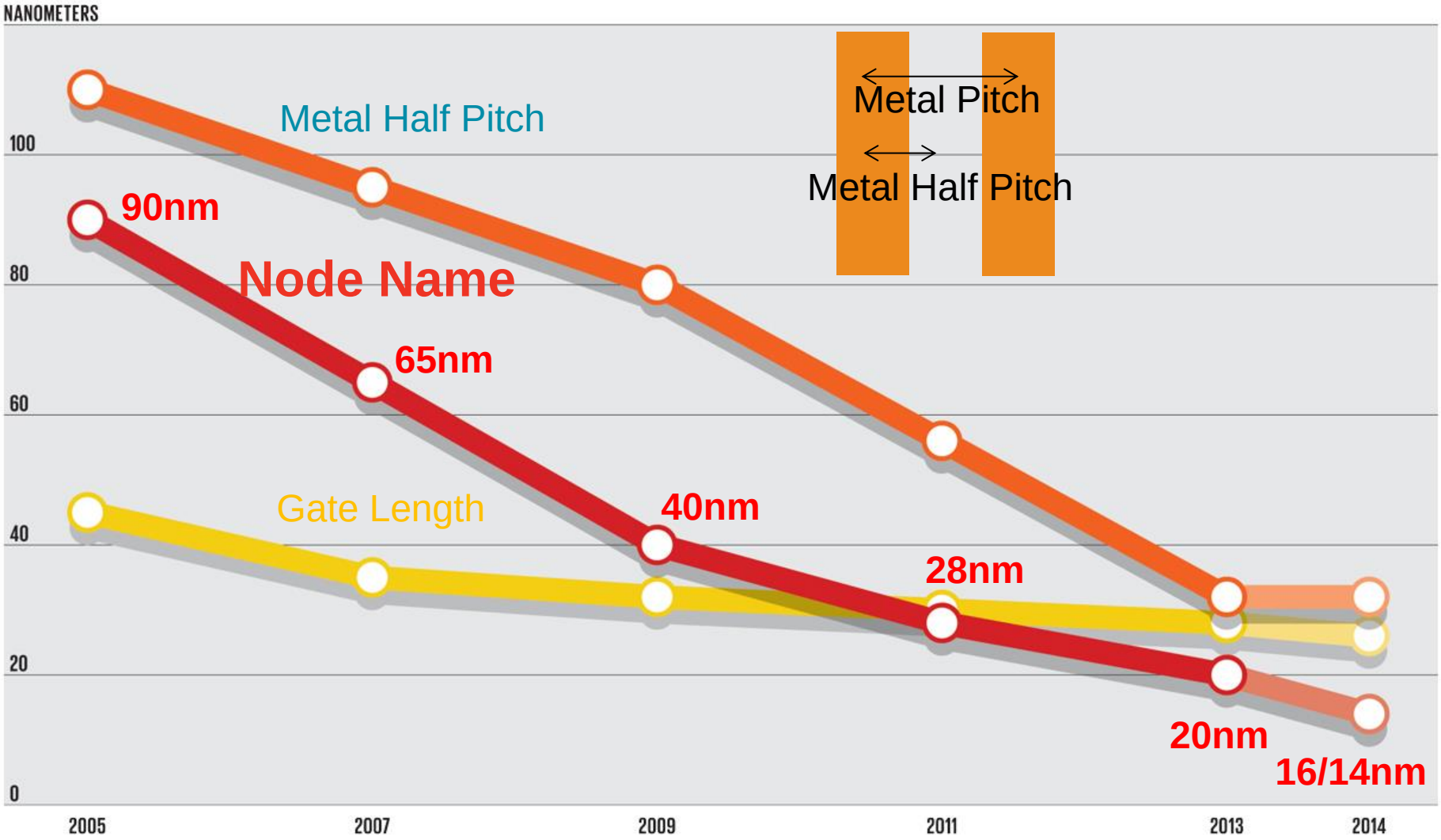
Node Name, Chip Dimensions or Marketing?



IEEE Spectrum Nov 2013: The End of the Shrink

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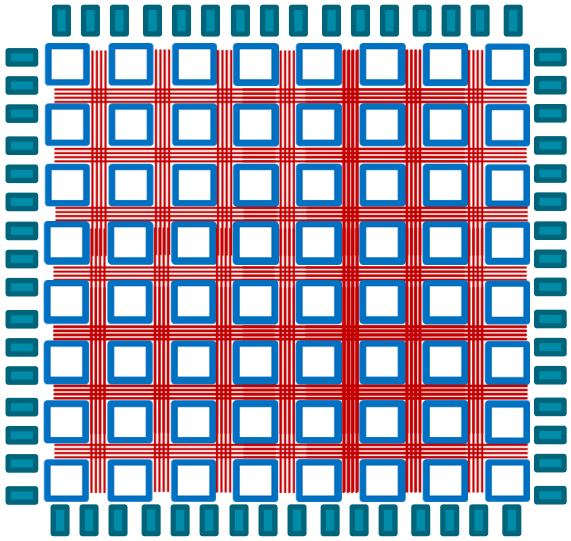
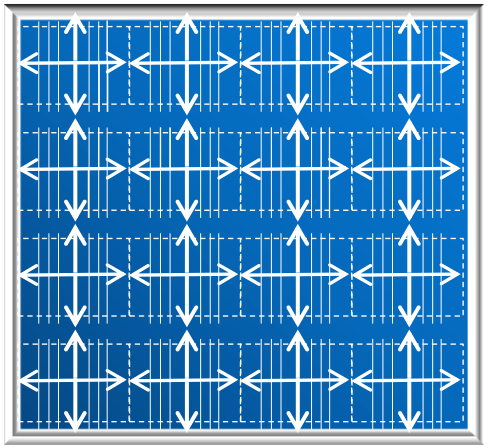
Scalable Architecture : FPGA

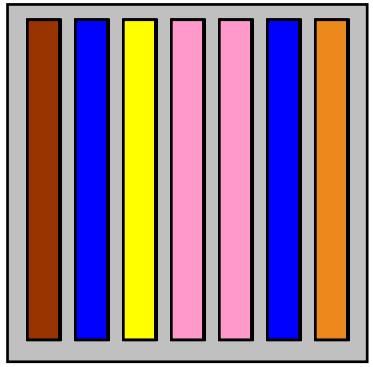
- 2001 : FPGA = Glue Logic

- 2013 : FPGA = UltraSCALE SOC





- Modular
- Hierarchical
- Re-Use



Logic
IO
Memory
Processing
Serdes
DSP

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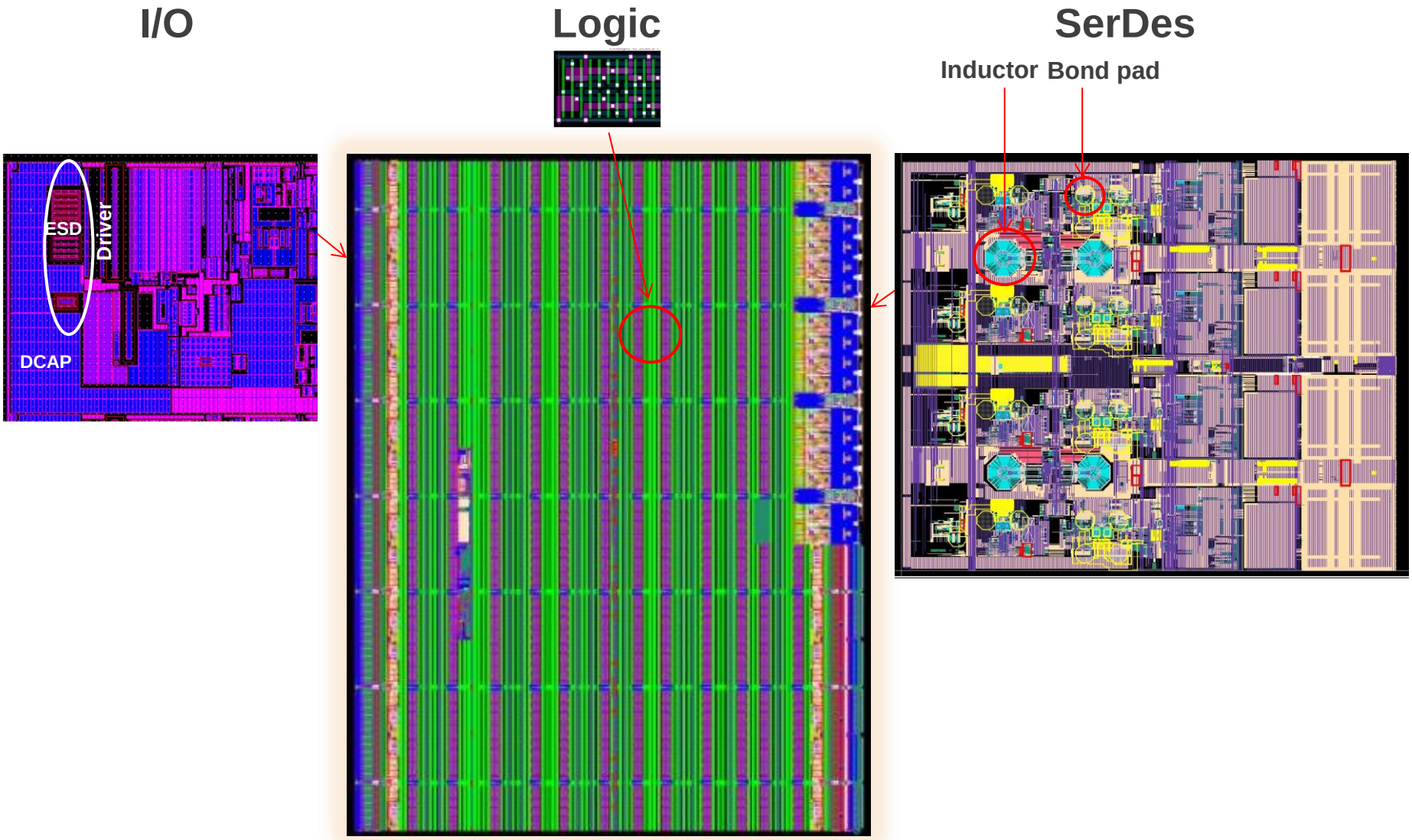
Moore's Law is About Logic, IO and Memory



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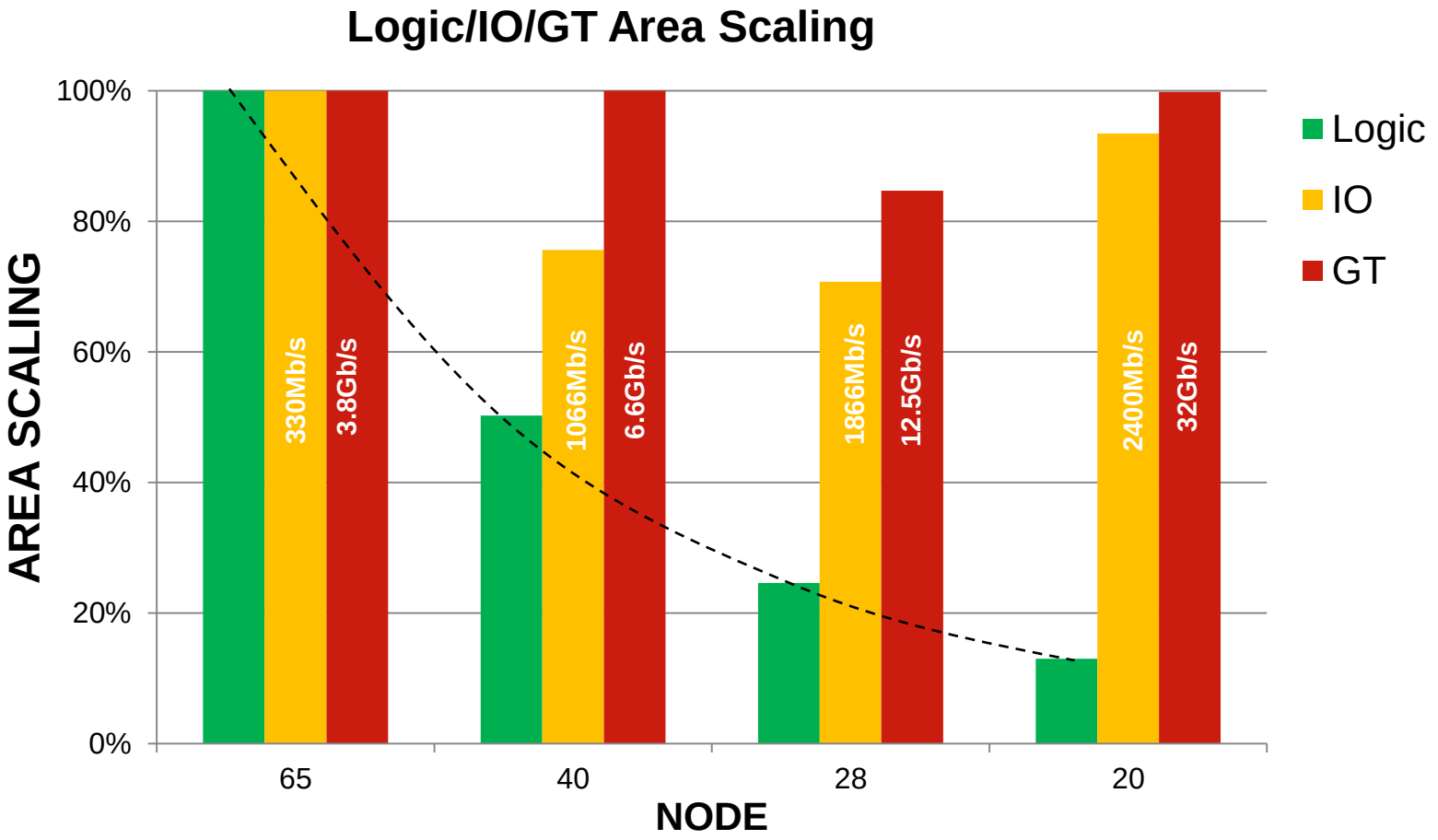
Non-Uniform Block Scaling



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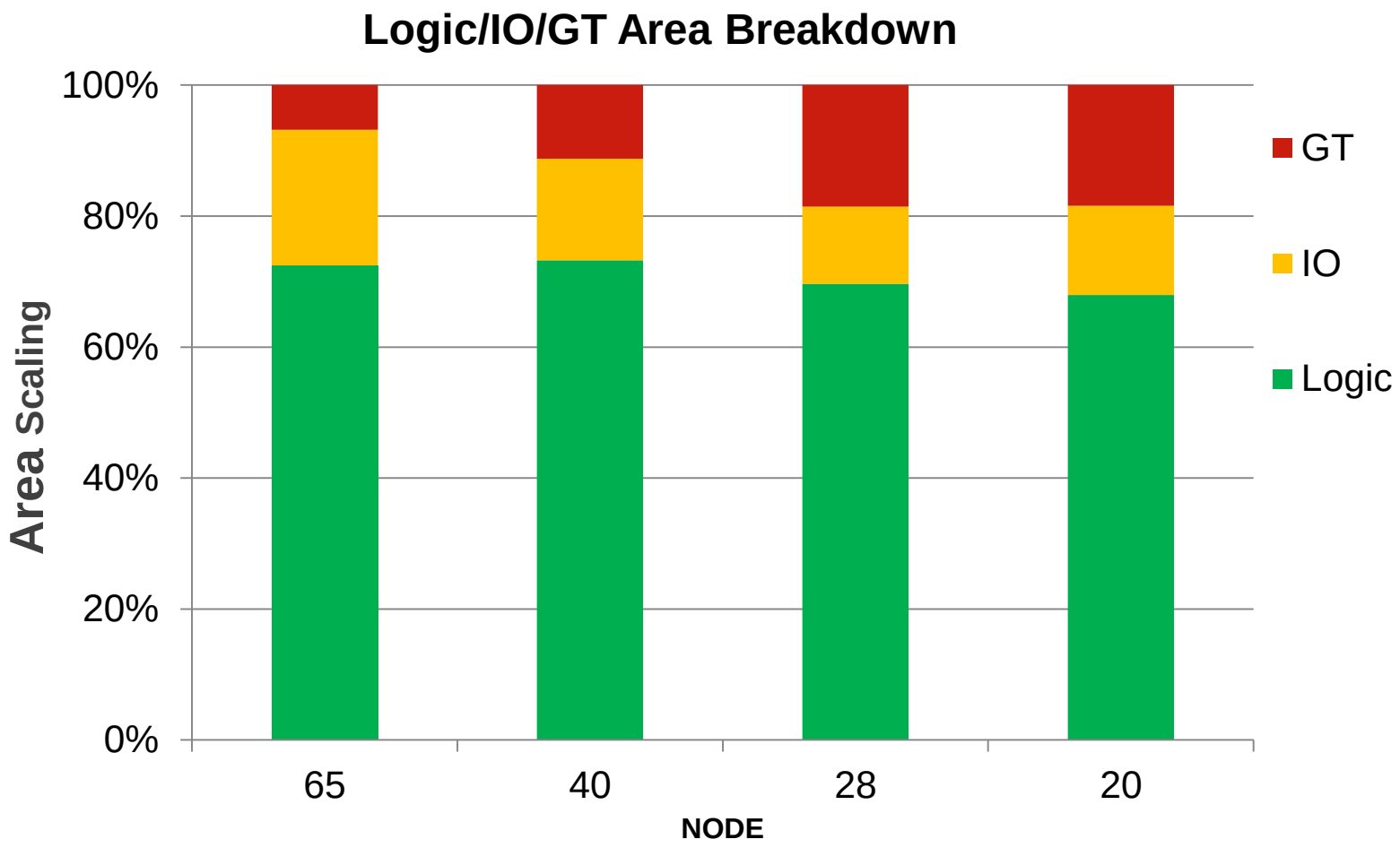
Mix Has Also Changed, Putting More Pressure on Area



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What is Driving the Bandwidth Increase?

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Cable Access Growth Exceeds Moore's Law (Nielsen's Law)

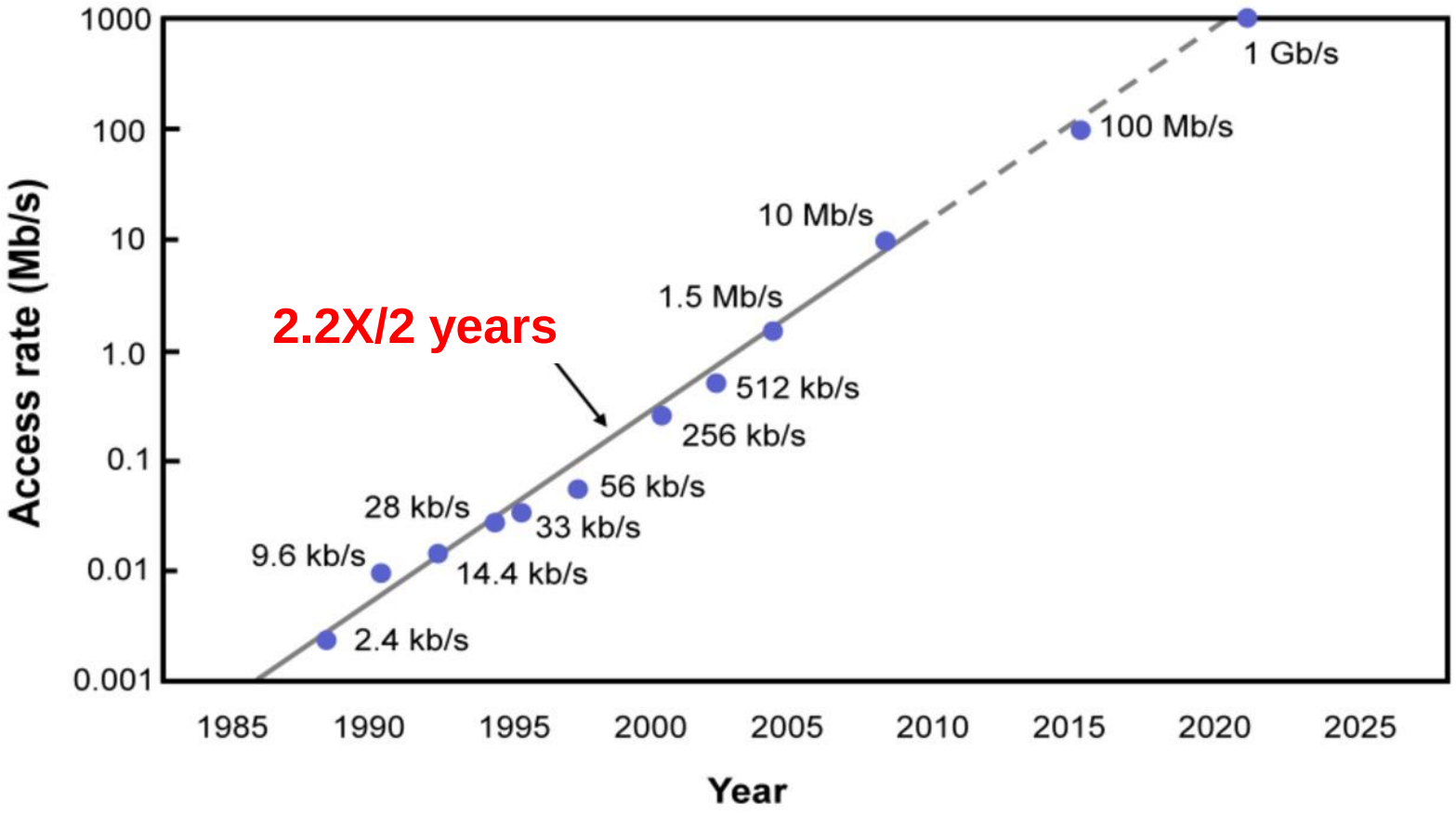

Fig. 1: Historical Evolution of Access Capacity.
Source: Tucker (2010b)

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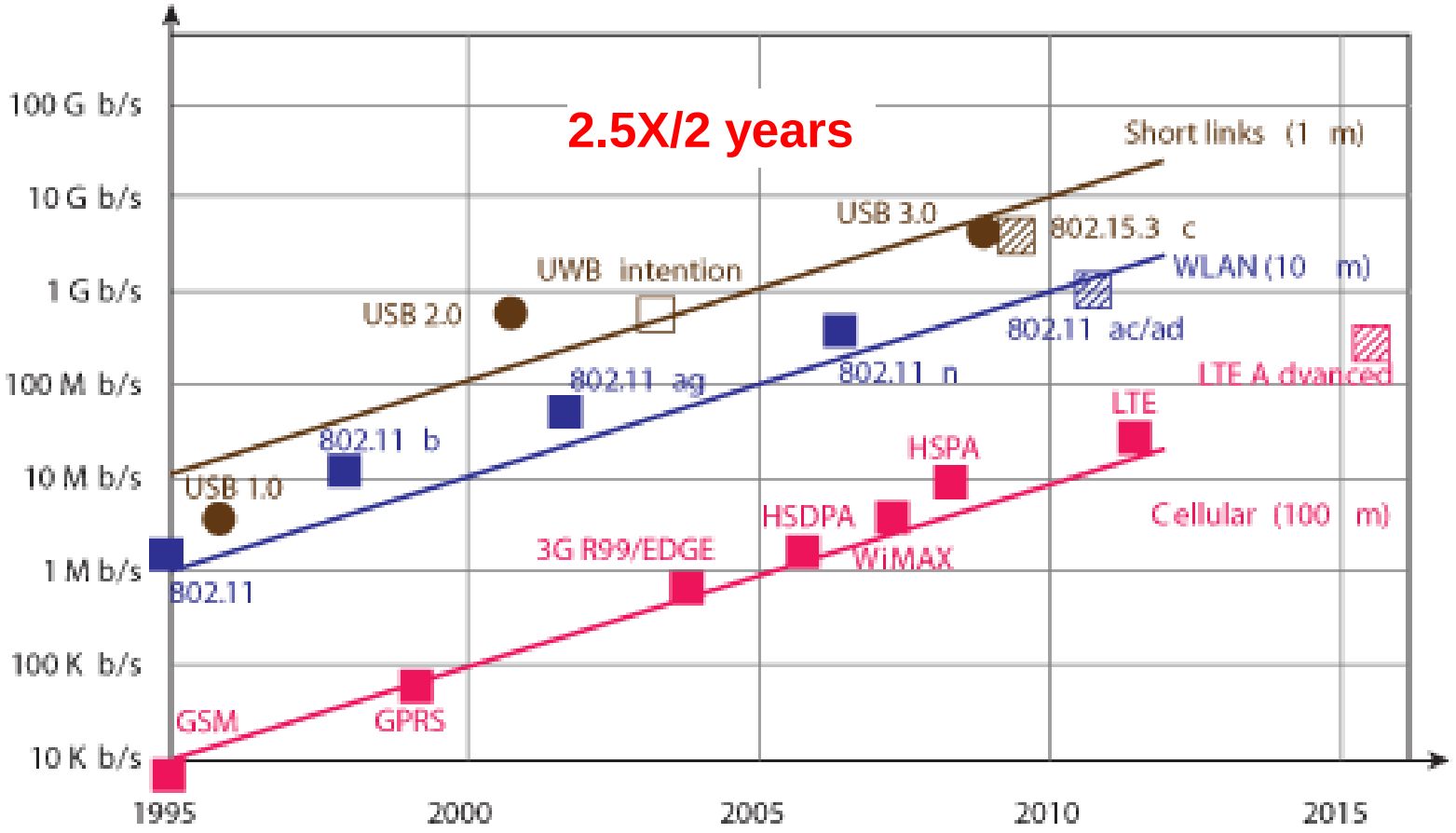
Similar Story in USB, WLAN and Wireless



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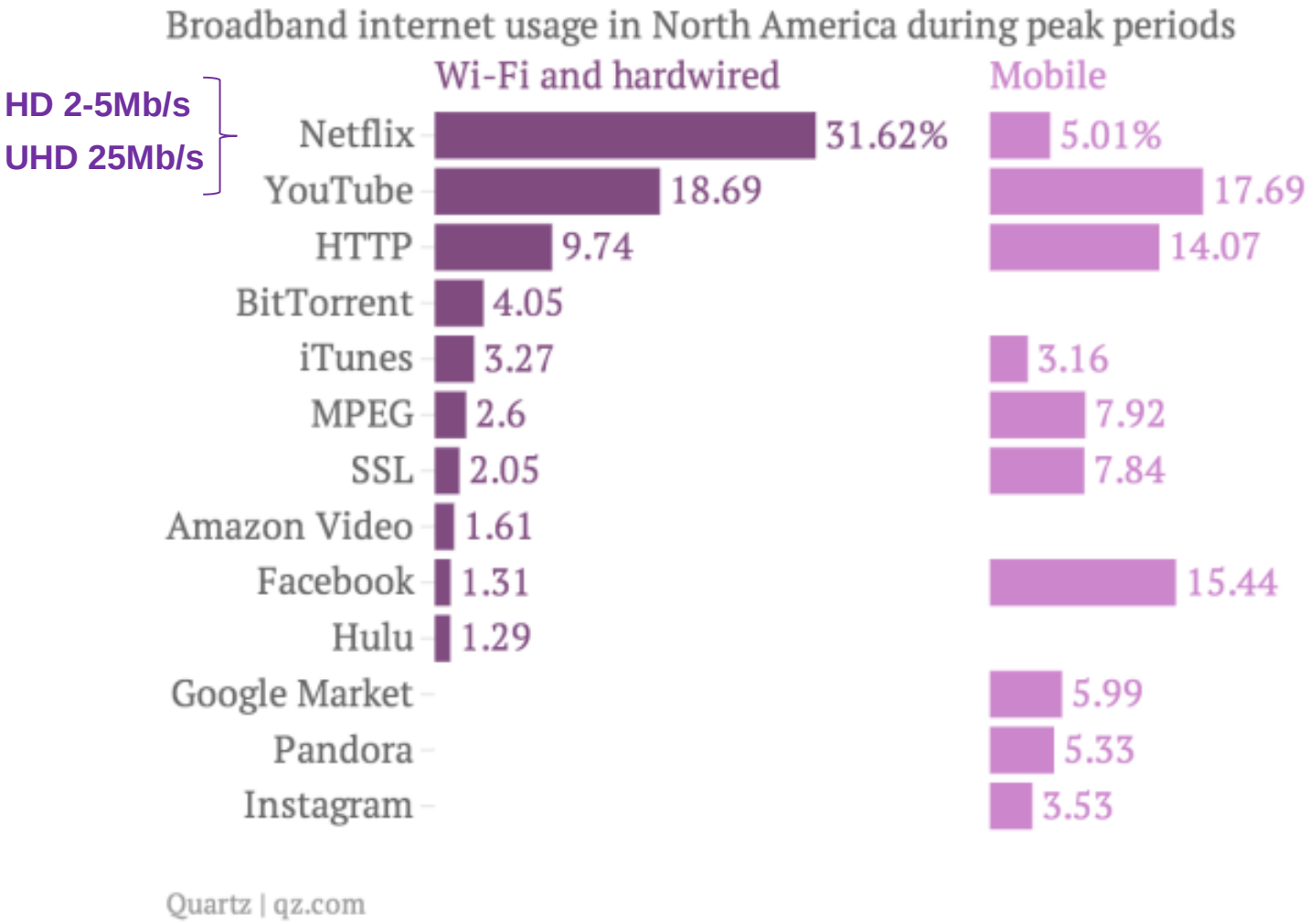
Driven by Streaming Video



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What is impact on FPGA

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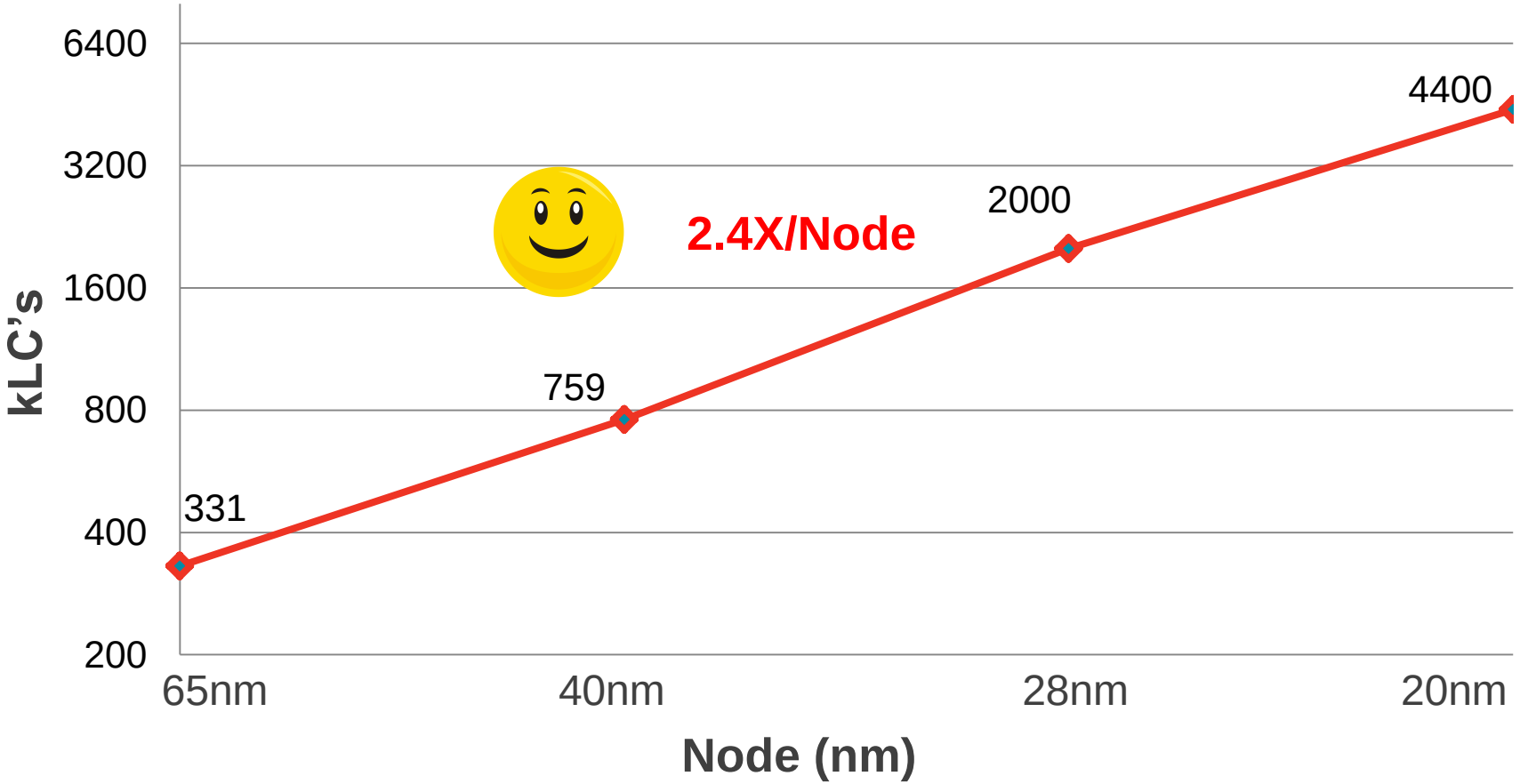
Maximum Density Of Xilinx FPGA By Node



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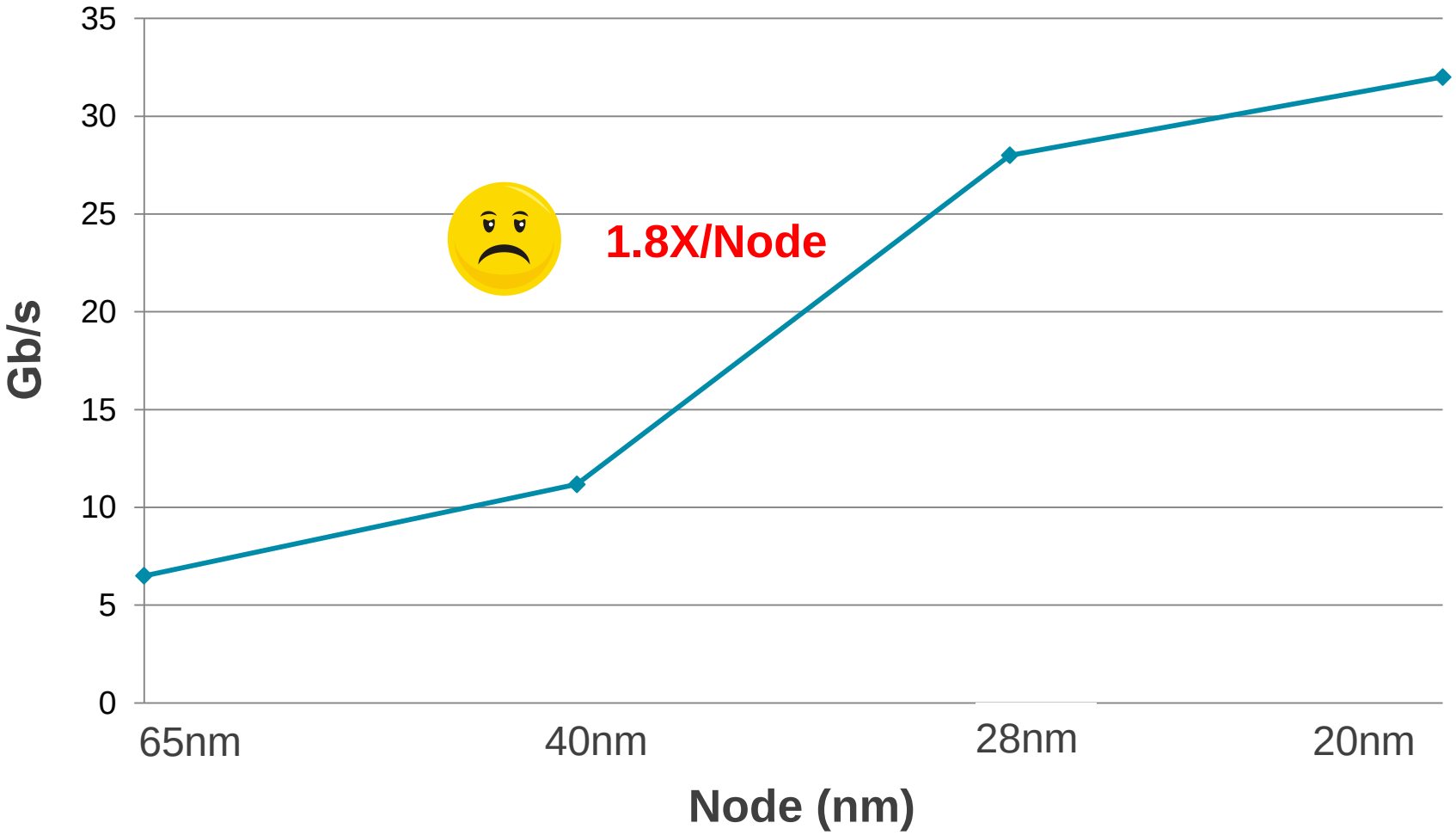
Maximum Xilinx SerDes Rate (by Pin)



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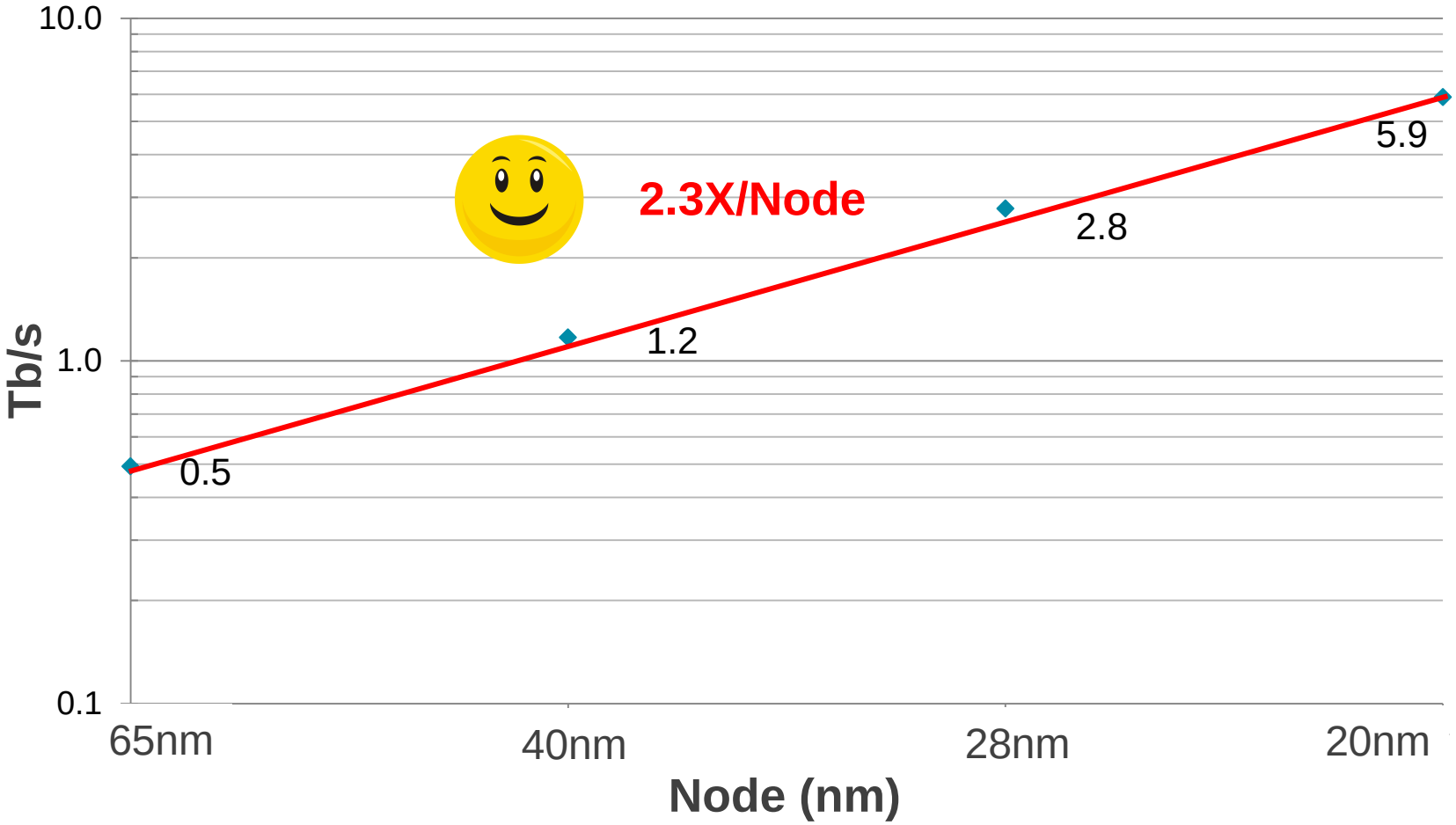
Aggregate Xilinx SerDes Bandwidth by Node



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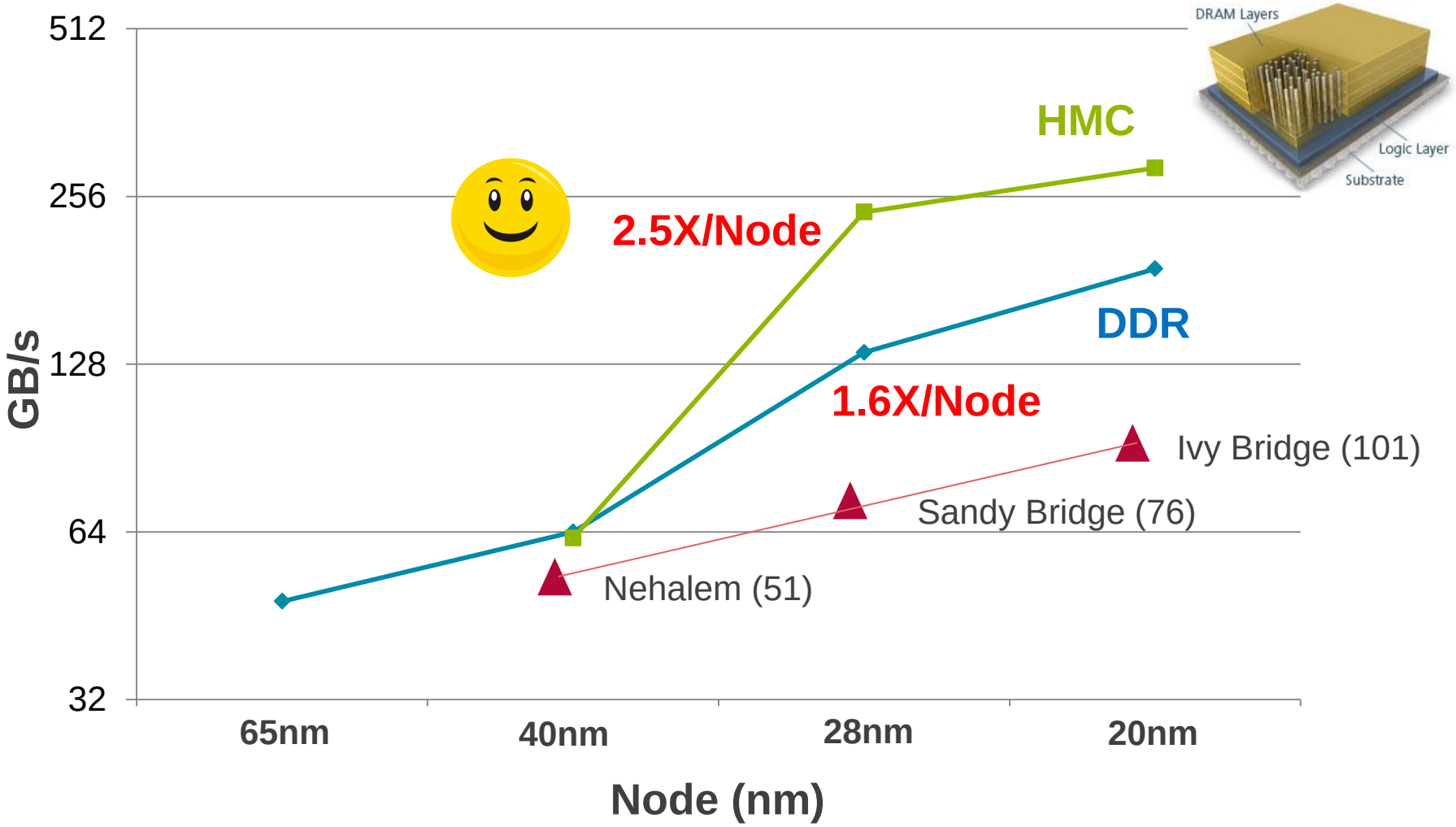
Aggregate Xilinx FPGA Memory BW by Node



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3-D Stacking, Providing More Silicon Area at Lower Cost and Lower Power

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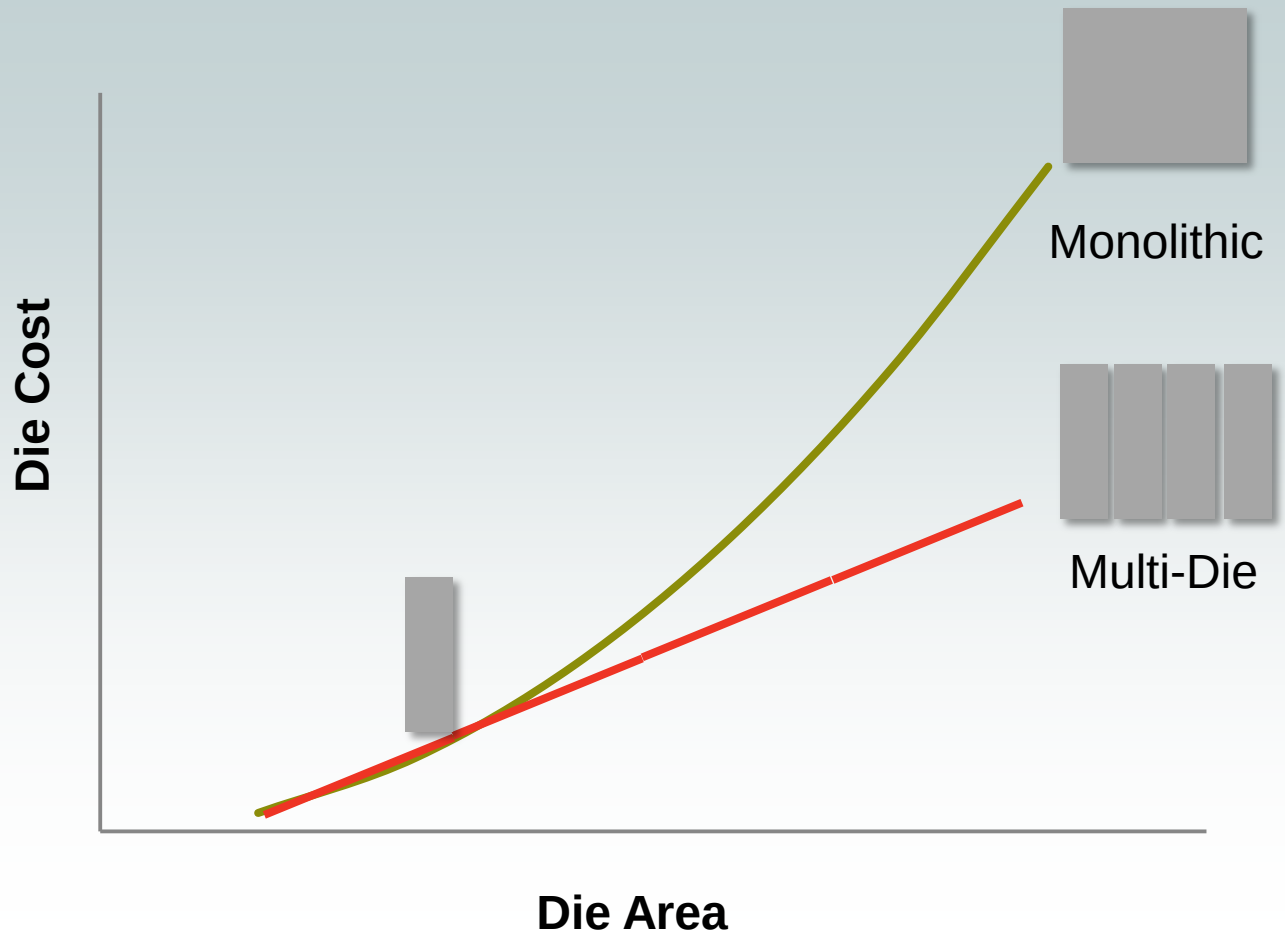
Cost Comparison: Monolithic vs Multi-Die

"Moore's Law is really about economics" *– Gordon Moore*



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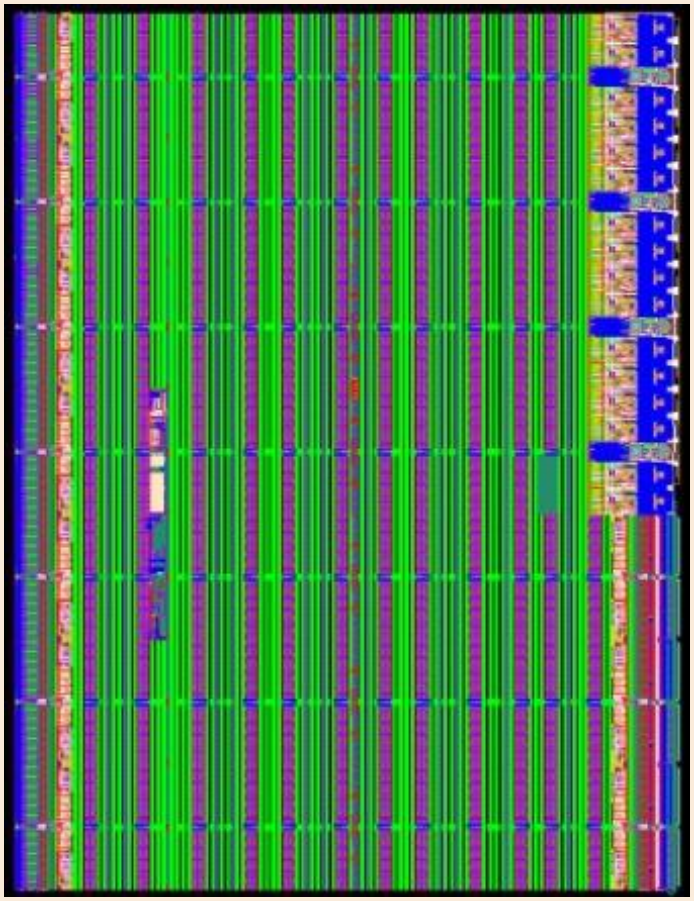
Why is First 3D Logic Product an FPGA?



- Natural partition using "long lines"
- Very low "opportunity cost"
- No 3rd party dependence
- "Size matters" to customers
- Compelling value proposition "next generation density in this generation technology"

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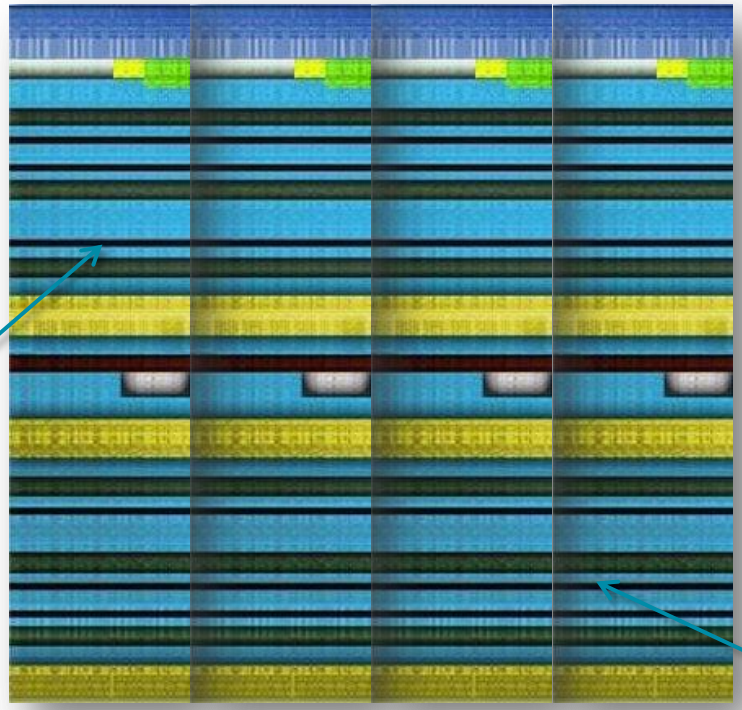
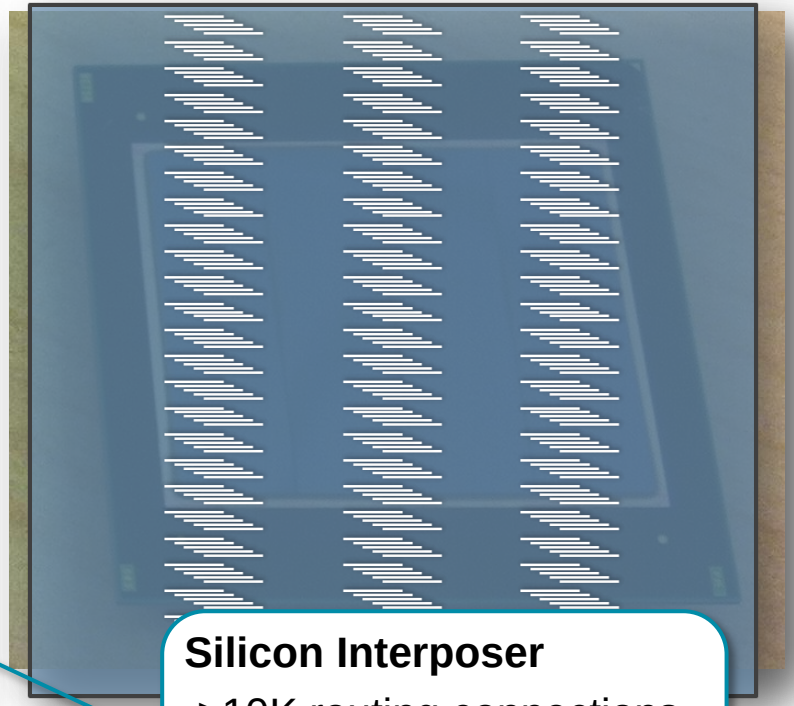
Virtex 2000T: Homogeneous Stacked Silicon Interconnect Technology (SSIT)



FPGA slice

FPGA Slices Side-by-Side



Silicon Interposer

>10K routing connections between slices

~1ns latency

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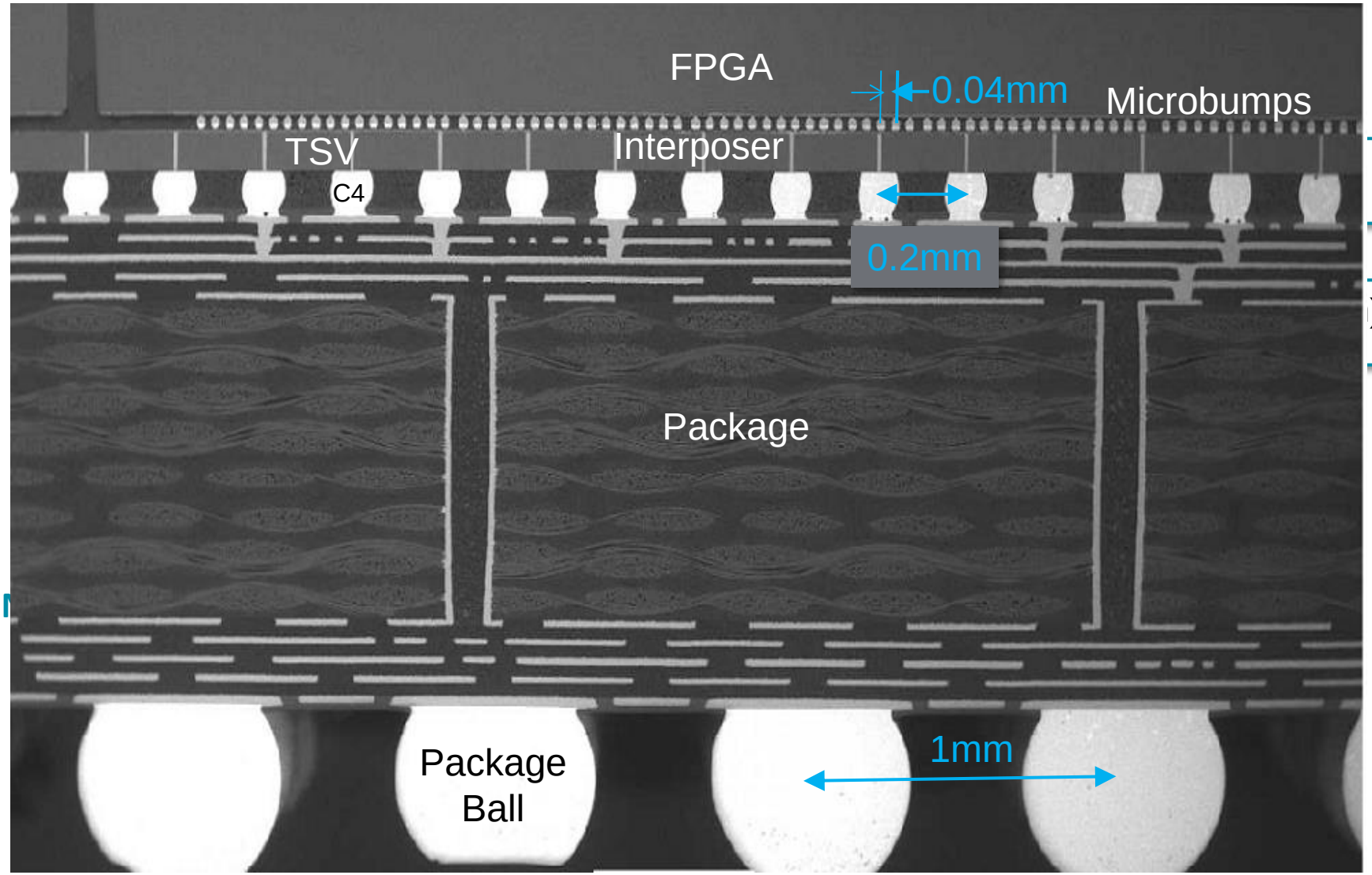
Elements of SSIT



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Interposer Optimizes Energy/Bit

Interconnects	Energy Efficiency (pJ/bit)
Inter-Die on Si Interposer [1]	0.4
Intra-Package MCM [2]	0.54
Inter Package (low loss cable)[3]	2.6
Short-Reach SerDes on PCB [4]	13.7

[1] Xilinx SSI technology
[2] 23.3, ISSCC 2013 (Poulton, Dally, *et. al.*)
[3] 23.2 ISSCC 2013 ((Mansuri et al)
[4] Pawlowski, Hot Chips 23

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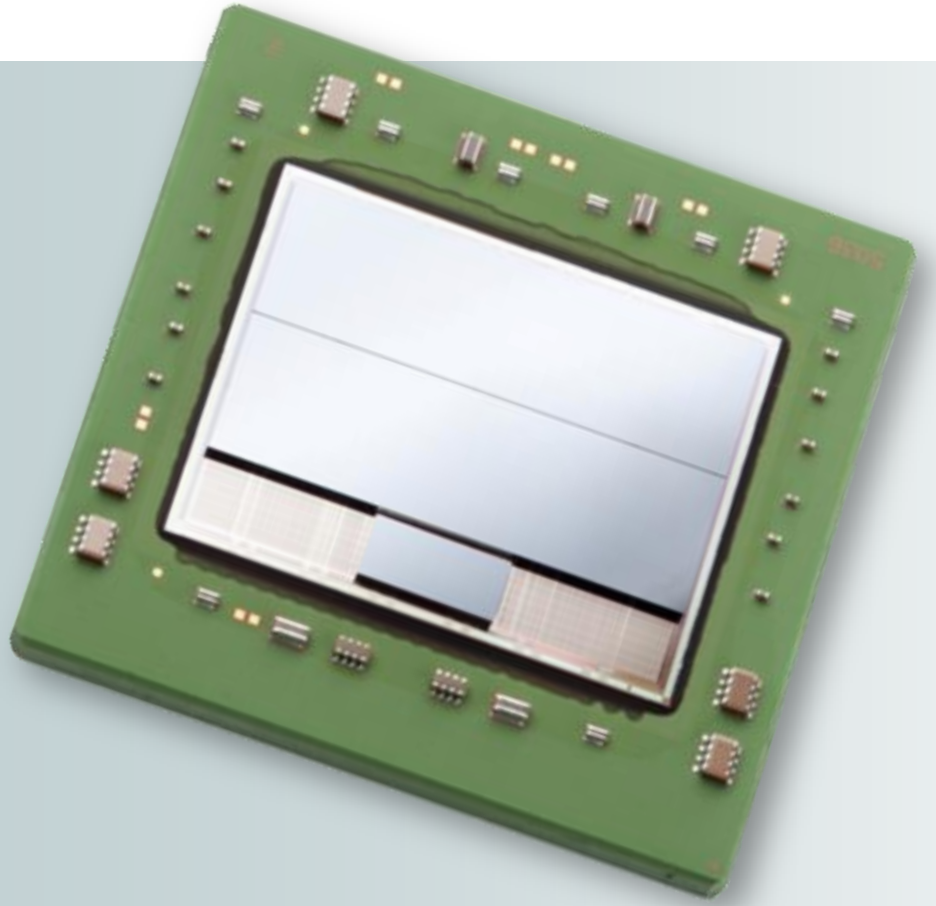
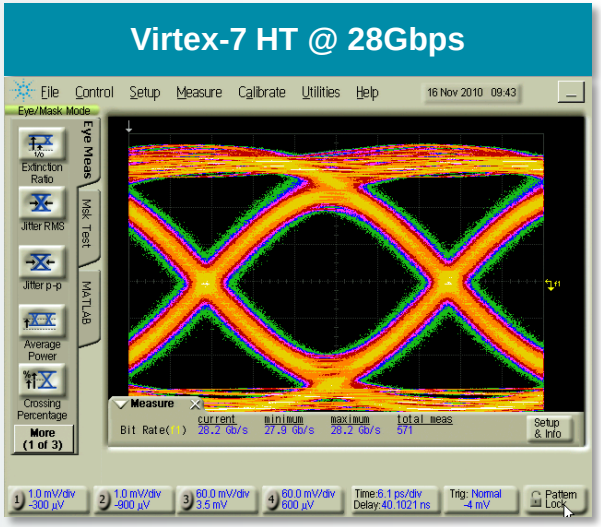
7V580T – Dual FPGA Slice with 8x28Gb/s SerDes Die





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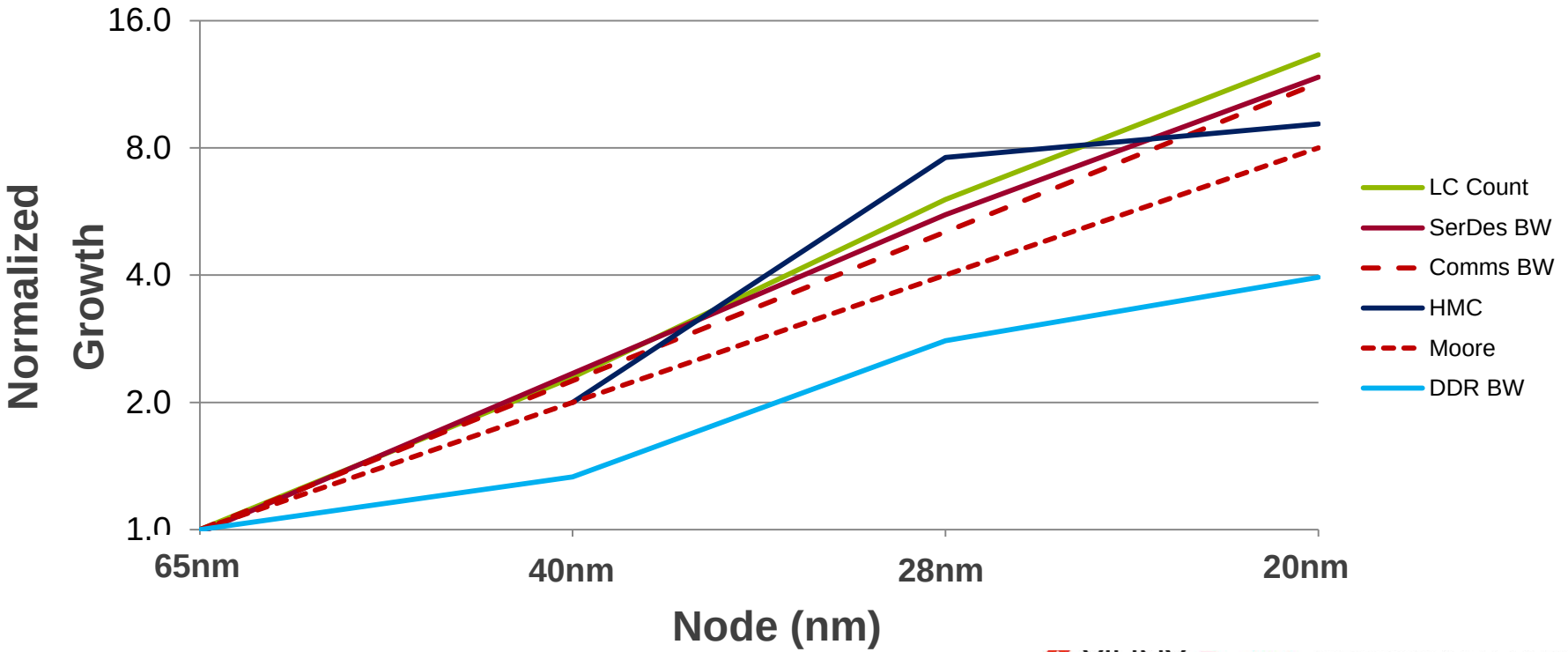
Takeaways

- Xilinx LC counts have exceeded Moore's Law and are keeping up with Communications requirements
- SerDes aggregate bandwidth is keeping up with Comms growth
- I/O (in particular DRAM) aggregate bandwidth is falling behind
  - Serial memory (HMC) is mitigating. Interposer based memory (HBM) will further mitigate.



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Future Will be More Interesting

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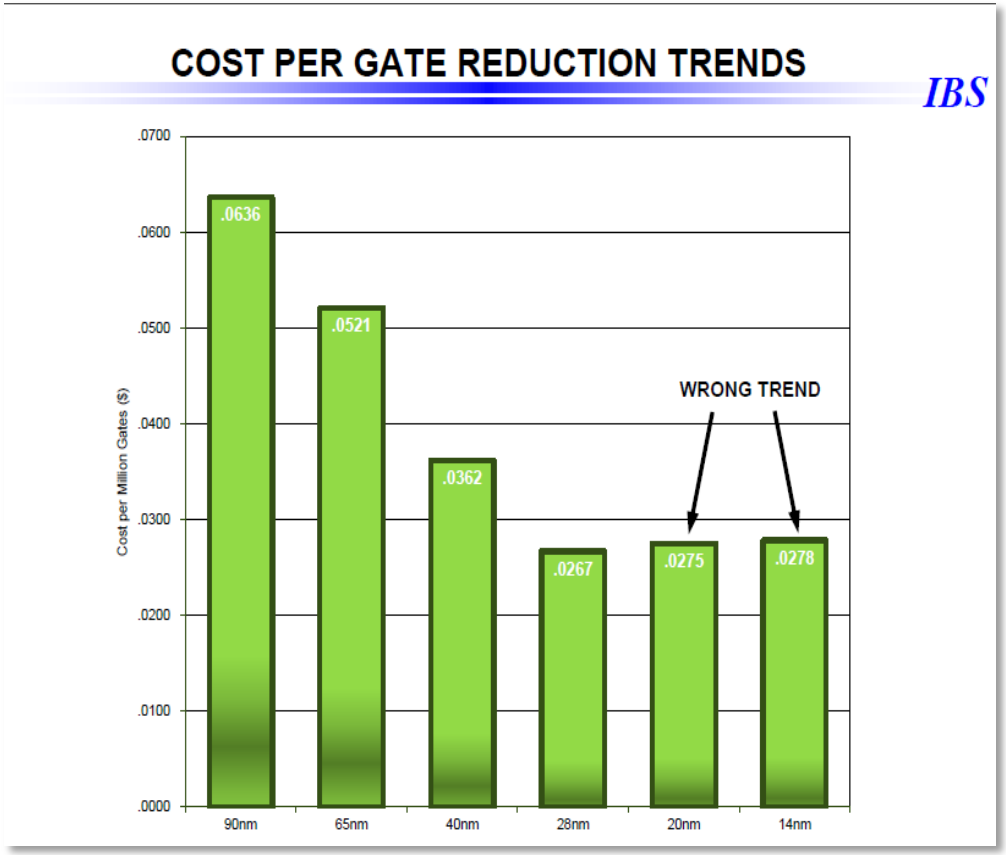
Industry Debates on Transistor Cost



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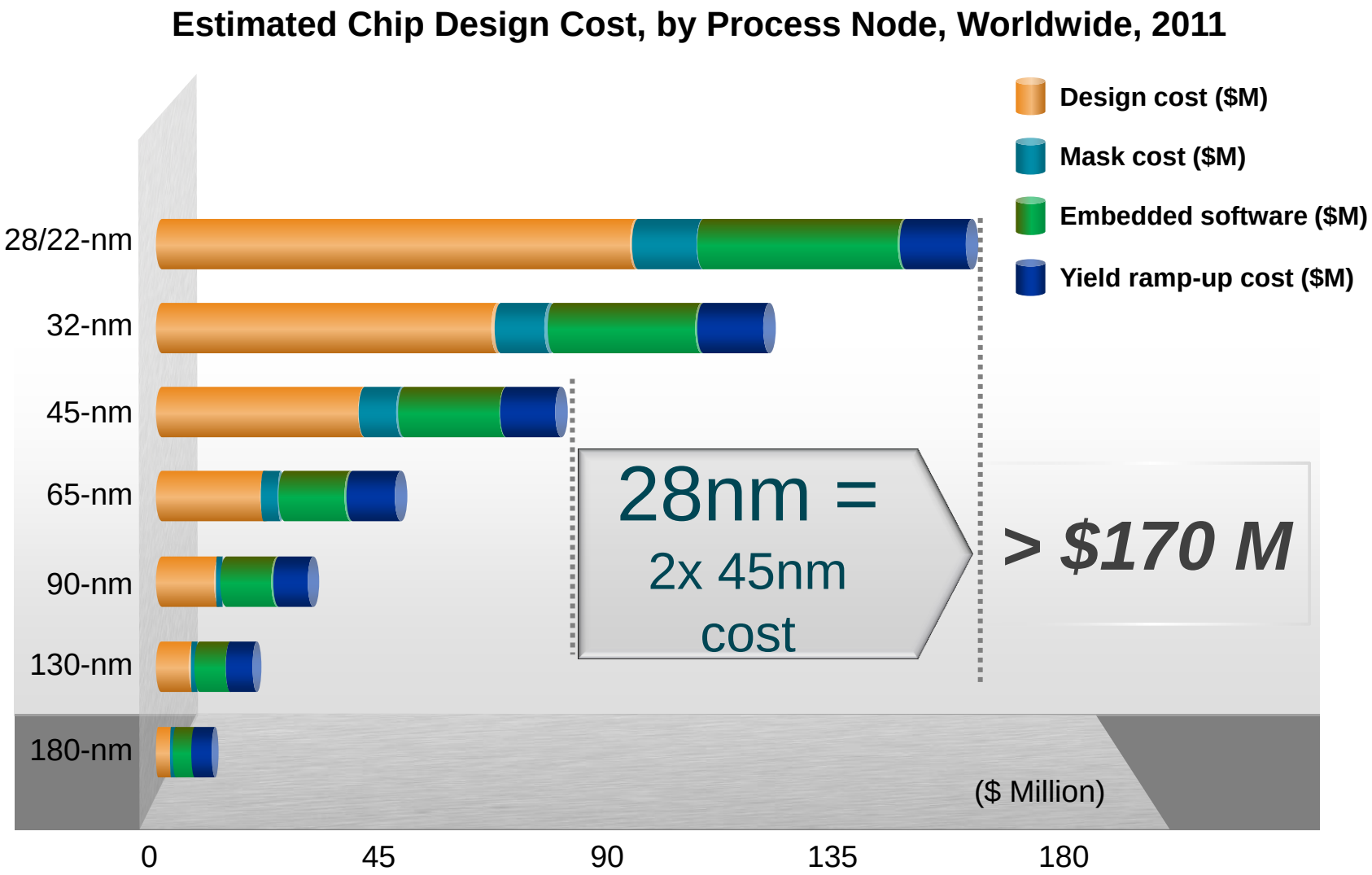
Design Cost



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Growing Challenge for ASIC & ASSP

>50% of Top 16 ASSP Vendors Losing Money

Communications ASSP Vendors	Operating Margin			
	2009	2010	2011	2012
A	21%	32%	26%	23%
B	16%	15%	5%	23%
C	12%	33%	31%	23%
D	19%	23%	26%	18%
E	2%	14%	13%	10%
F	-25%	-1%	8%	11%
G	15%	25%	18%	10%
H	12%	19%	10%	1%
I	-21%	6%	-1%	-23%
J	-21%	-2%	-11%	-33%
K	-5%	15%	-5%	-19%
L	-4%	2%	-6%	1%
M	-22%	-18%	-13%	-11%
N	-15%	-7%	-	-
O	-15%	1%	-18%	-24%
P	-11%	-6%	-47%	-98%

Source – Public reports, Xilinx estimates

- Eroding customer confidence in vendors
- High cost burden from over design for diverse needs
- No ability to differentiate or customize

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Trend Wireless : Scalable Platforms

Capacity

Indoor

Residential Femto

4-16 Users
<100mW

Home

Enterprise Femto

30-60 Users
<250mW

Office

Picocell

30-200 Users
<1W

Dense Indoor
(Malls, Transport Hubs)

Outdoor

Microcell

Urban Infill

~200 Users
<1-10W
Single Sector

Macrocell

Wide Area

~200 Users/ sector
20-100W
Multi-Sector

Macrocell + Active Antennas

Wide Area

2-3x Data Capacity of RRU

Coverage

- **Source ALU**

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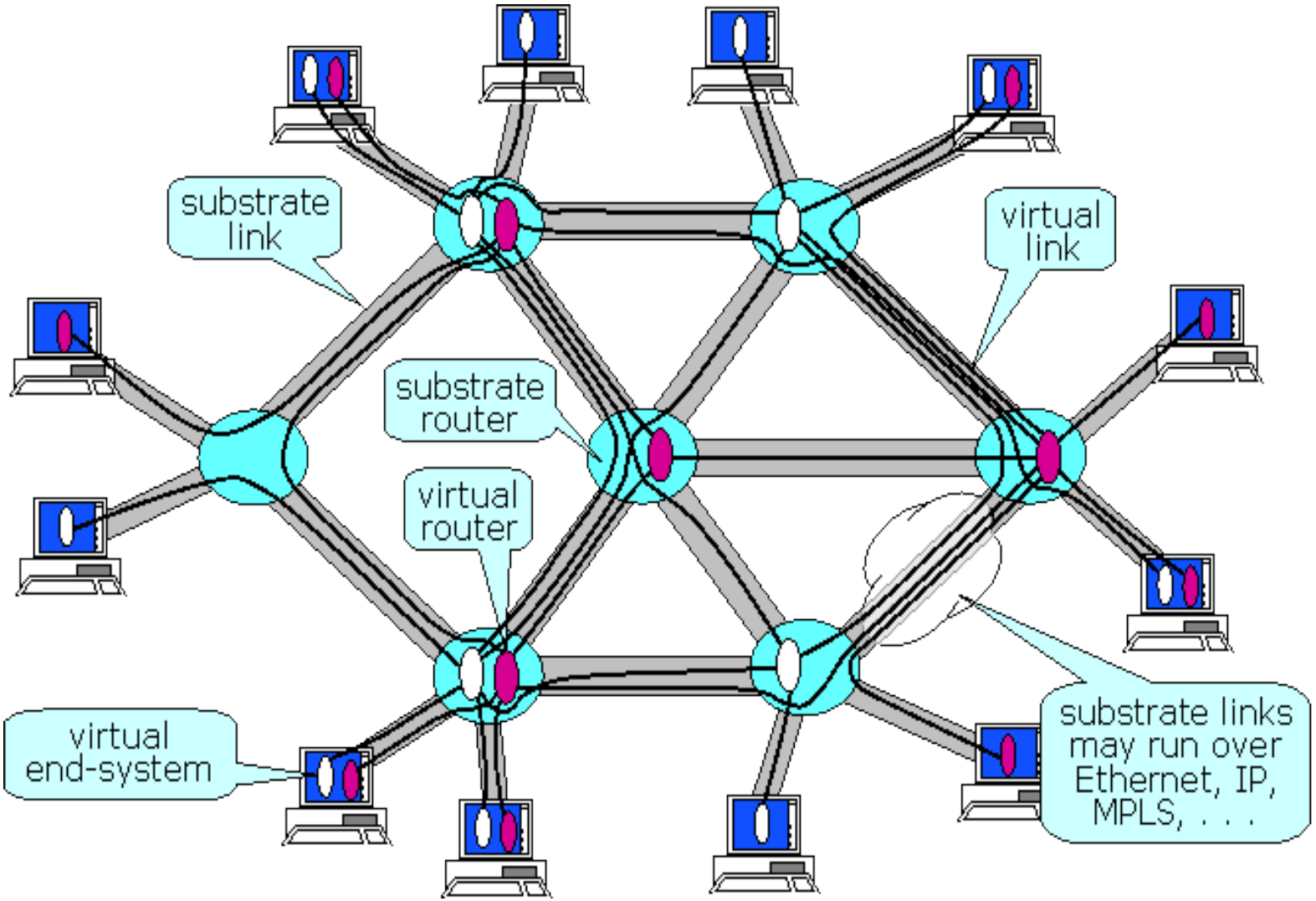
Trend Wired : Software Defined



From “Virtualizing the Net” by Jon Turner

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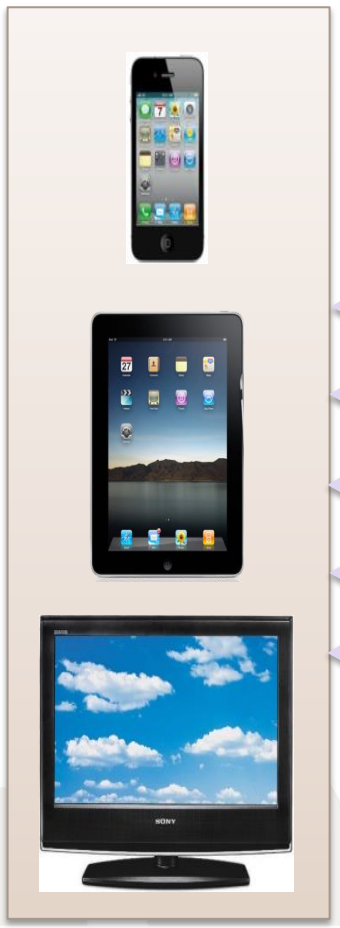
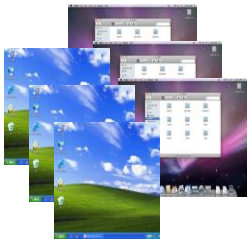
Trend Services : Different Figures of Merit



Latency (ms)



Computing

GB, Latency (s)

Storing

GB, BW (mean, var)

Streaming

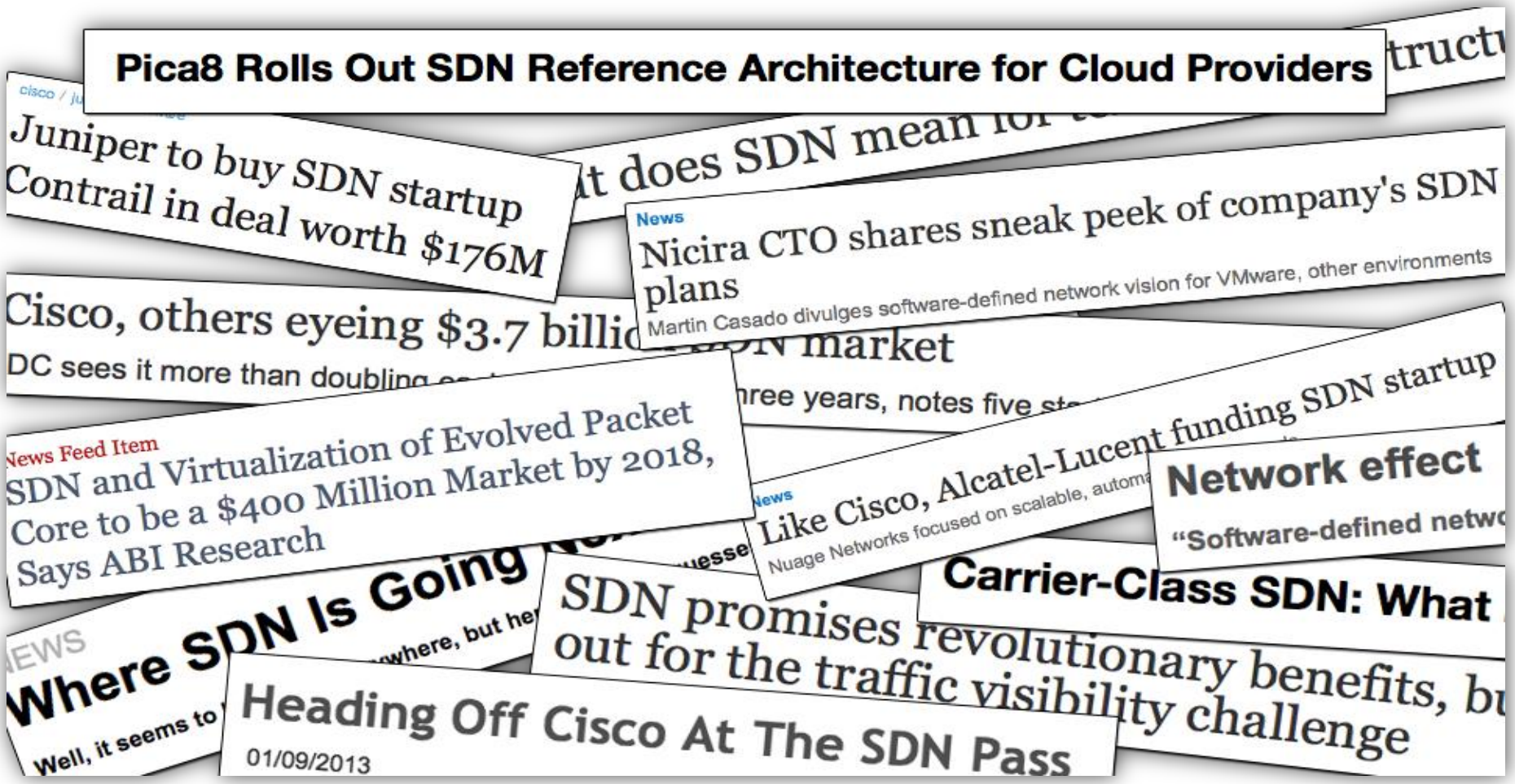
Gaming

GB, BW (mean, var)
latency (ms)

Communicating

Latency (ms), BW (mean)

Software Defined Networking gained massive industry mindshare



The best thing about OpenFlow or SDN, is that it's brought back a new hope to networking. Networking is cool again- Jayshree, CEO - Arista Networks

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Trend in Embedded : More Intelligence…Smart

SMART Data Center Revolution

New Opportunities to Control Costs and Increase Strategic Advantage…

MACHINES THAT UNDERSTAND

embedded VISION ALLIANCE

Smart wireless networks to the rescue

Carriers are turning toward more intelligent network management…

Smart Factories

For factory management in the future, it will become essential to strive to implement smart capabilities…

The Next Big, Digital Economy; 'Smart Energy'

The energy market is undergoing a major transformation…

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Trend Data Center : Scalability

Big Data

Increasing Volume, Velocity, and Variety

Low power

Reduce operation and cooling costs

Security

Both outside and inside

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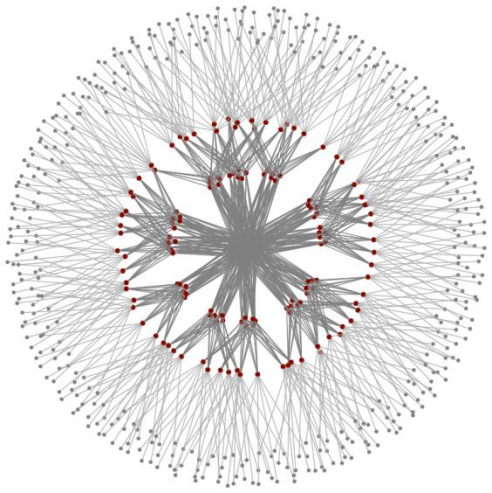
Impact of trends
(1) Networking

New network fabrics

- Faster, Fatter, and Flatter



Software defined networking

- Software control plane
- Hardware data plane

Content-aware networking

- Deep packet inspection
- Enhanced security

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Impact of trends
(2) Compute

ARM-based microservers

- Improved performance per watt

Hybrid SoC

- CPU+accelerators+fabric
- Cost and power reduction

Larger memory

- Hybrid NVRAM and DRAM
- Latency reduction

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Impact of trends
(3) Storage

Specialized functions

- Compression, encryption, memcached

Custom SSD controllers

- Higher performance
- Reduced latency

Data-aware storage

- Integrated database support
- Offload from processor

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Programmable & Smart Across All Markets

	All Programmable	Smarter
 **Wireless Comms**	• Multiple Spectrums • Multiple Standards (**LTE**, 3G) • Multiple Levels of QoS	• Self Organizing Networks (**SON**) • Cognitive Radio • Smart Antenna
 **Wired Comms**	• Network Function Virtualization (**NFV**) • Multiple Stds (400Gb etc.) • Dynamic QoS Provisioning	• Context Aware Network Services • Self-Healing Networks • **Video** Caching at the Edge
 **Data Center**	• Software Defined Networks (**SDN**) • Multiple Stds (FCoE, iSCSI ...) • Config Storage (SAN, NAS, **SSD**…)	• Data Pre-Processing & **Analytics** • Virtualized Resource Optimization • Intelligent **Appliances**
 **Embedded**	• Changing Resolutions (MPixel, Fps) • Emerging Video Stds (**UHD**, 8K/4K) • Evolving Video Processing Algorithms	• Object Detection & Analytics • Automotive Collision Avoidance • Industrial Machine **Vision**

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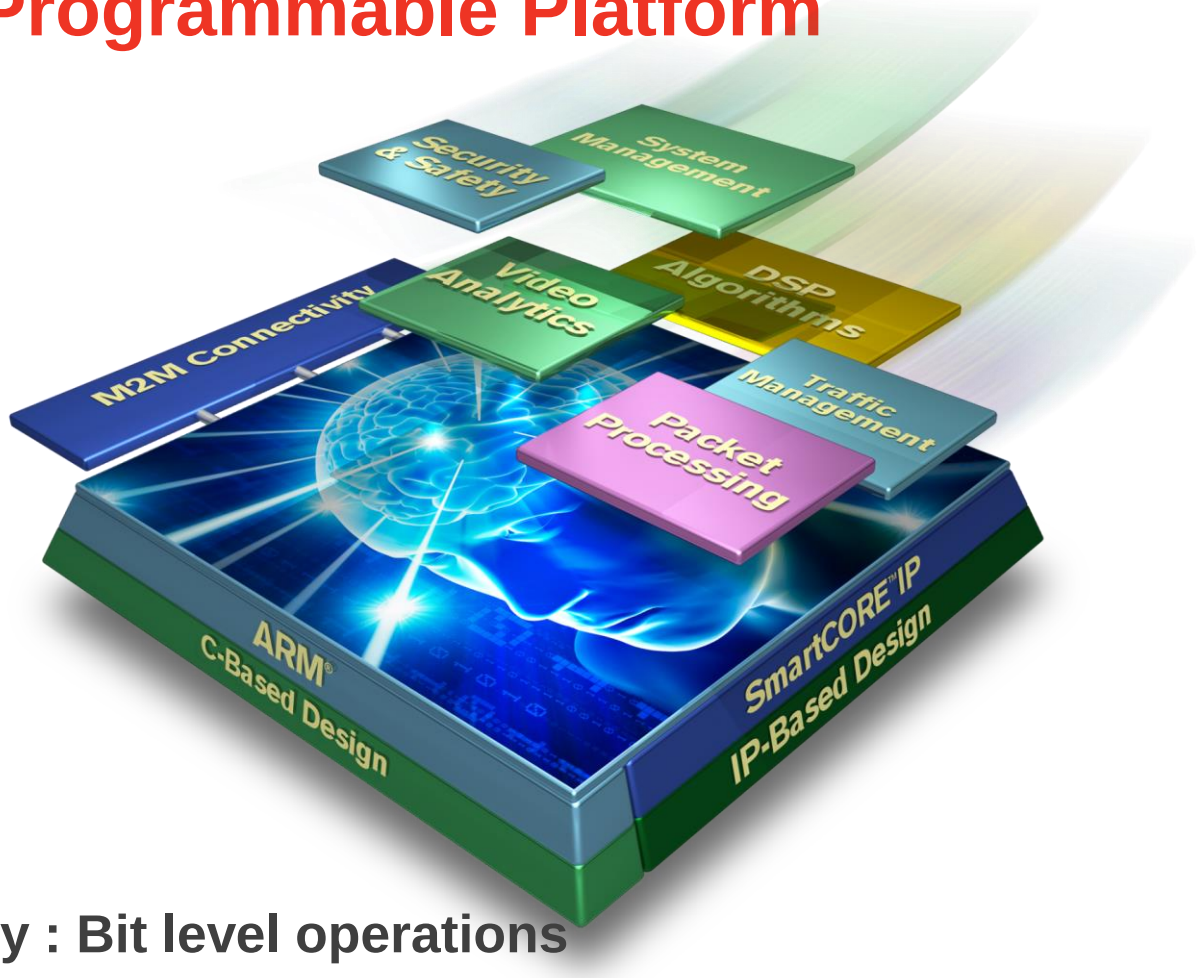
The All Programmable Platform



- Security : Bit level operations
- Packet Processing : Wide Datapaths
- DSP Processing : Pipelined Datapaths
- Graphics Processing : Parallel Micro-Engines
- System Management : Finite State machines

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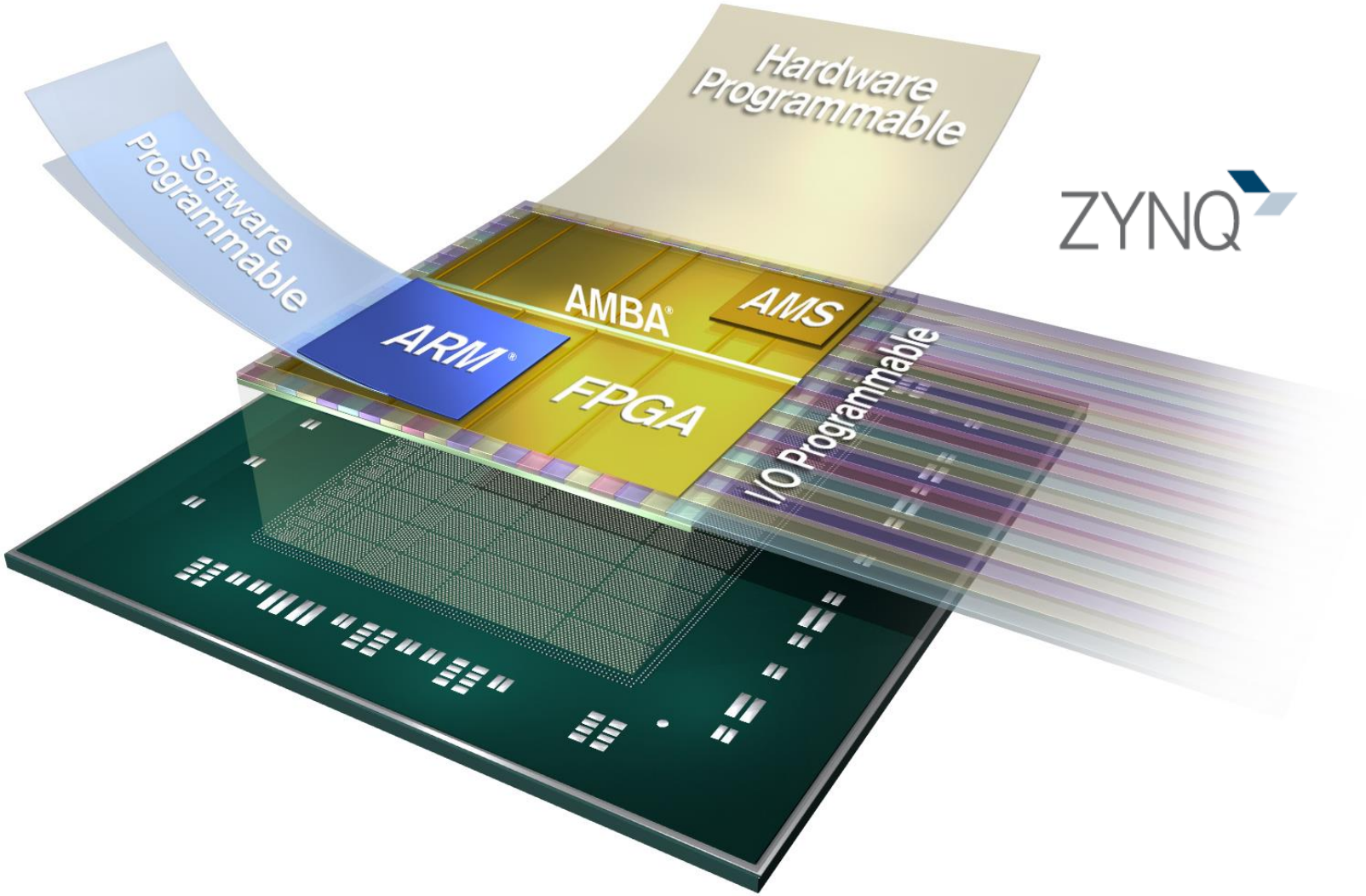
The Era of Heterogeneous Processing Unit



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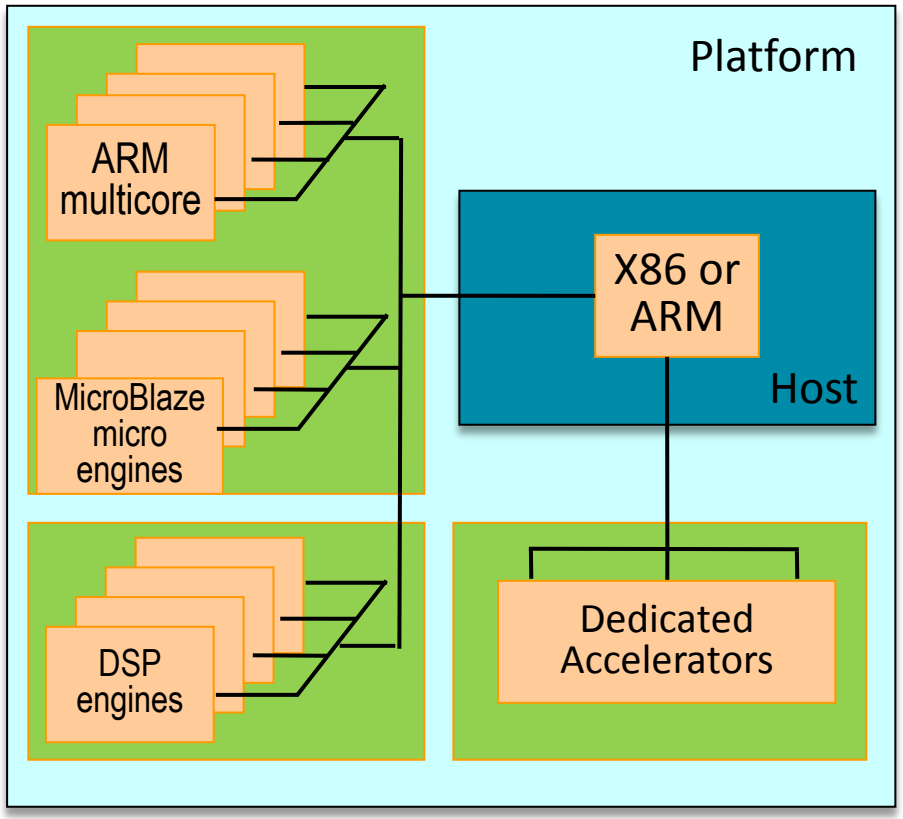
Programming the 'XSOC'

- X = Connected
- X = Scalable
- X = Parallel
- X = Heterogeneous
- X = Configurable
- X = Xilinx



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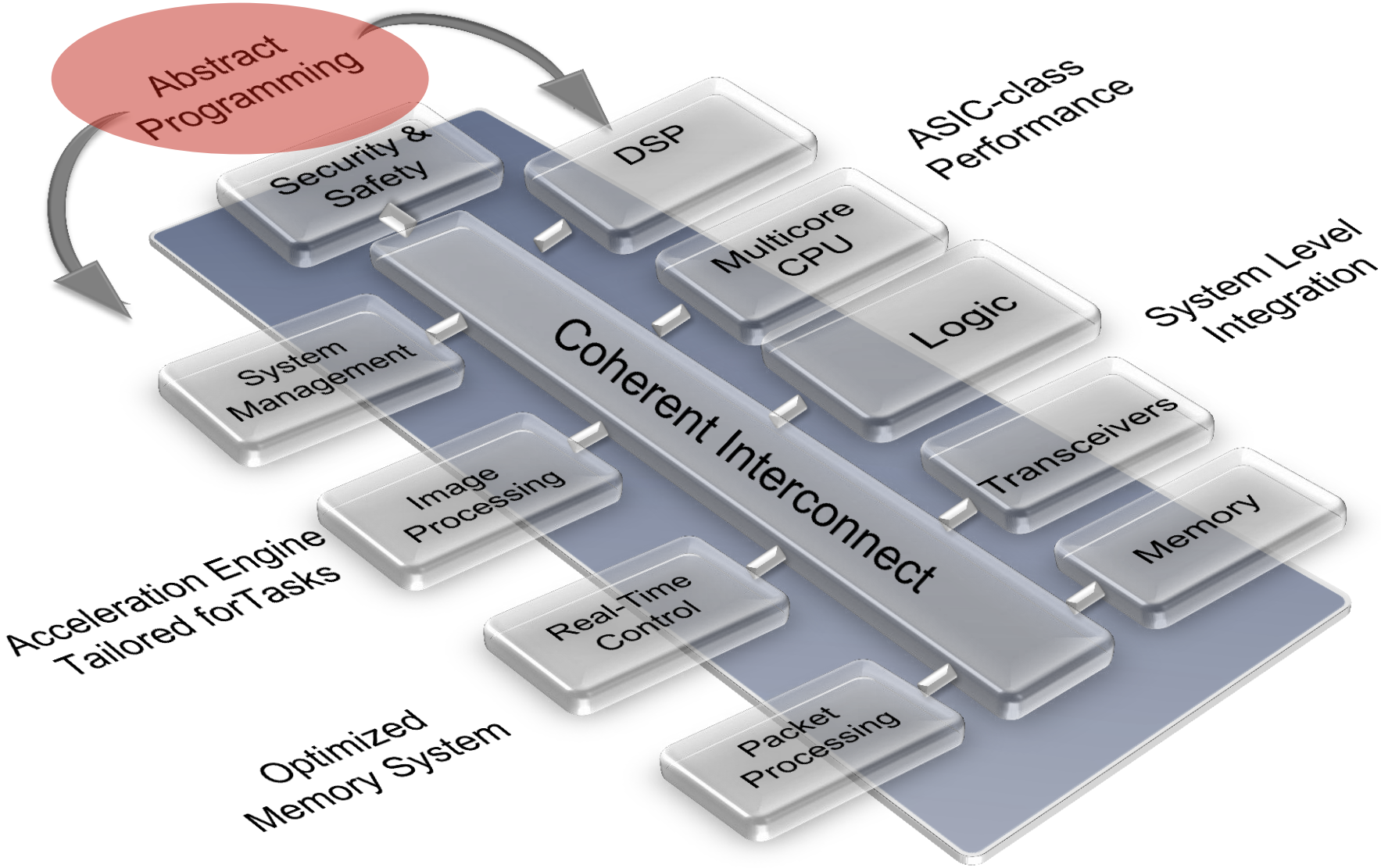
Delivering All Programmable XSOC

Heterogeneous Multi-Processing



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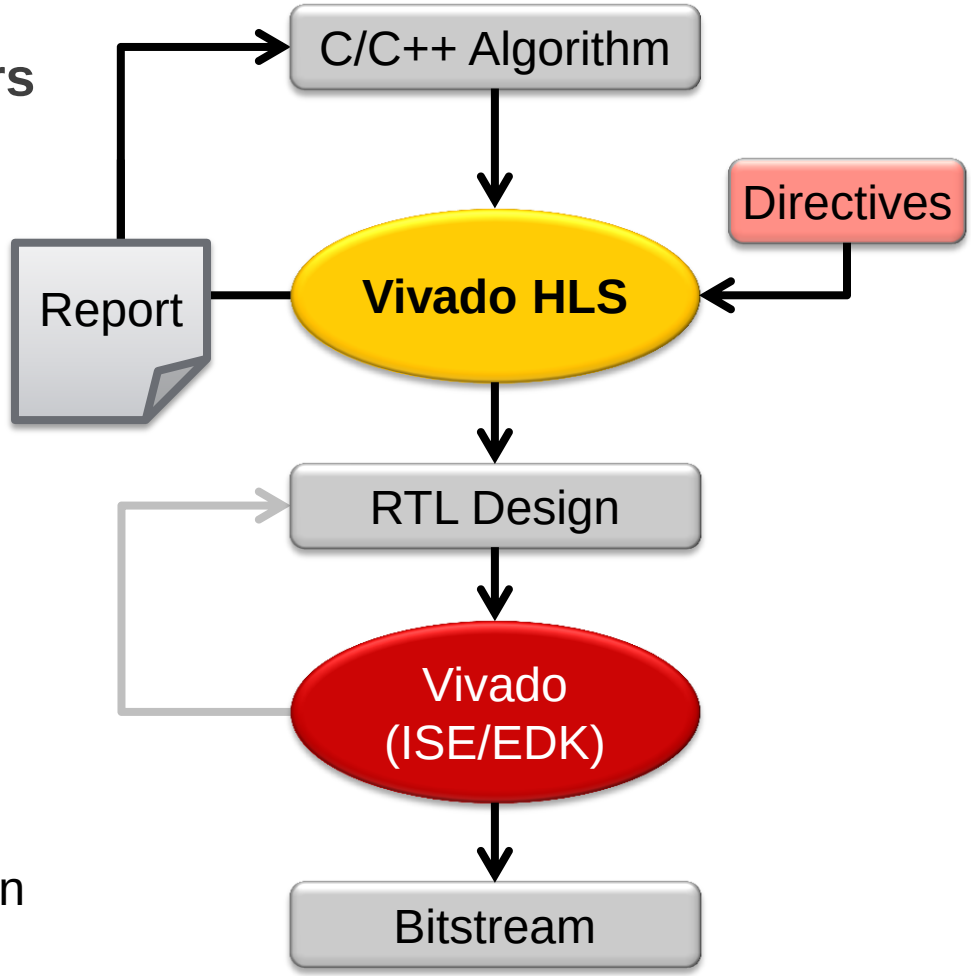
Programming Accelerators from C/C++

- **Enables software programmers to target Xilinx FPGAs**
  - Software-programmability
  - Portability: 7 series, Zynq
- **Delivers productivity increase for RTL designers**
  - C/C++ level verification and testbench reuse
  - Earlier area/latency reports
  - Software-driven design exploration



More Turns Per Day (Verification and Architecture Exploration)

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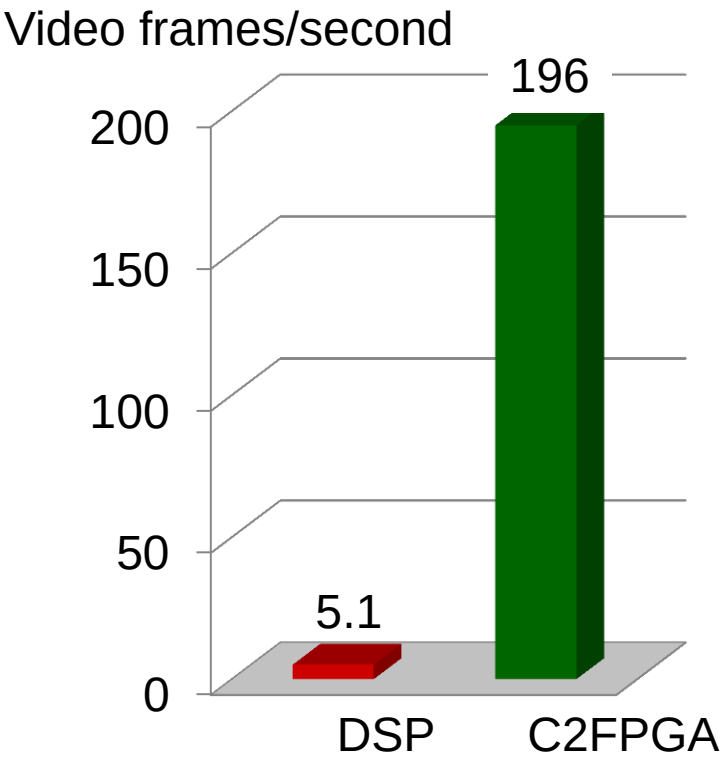
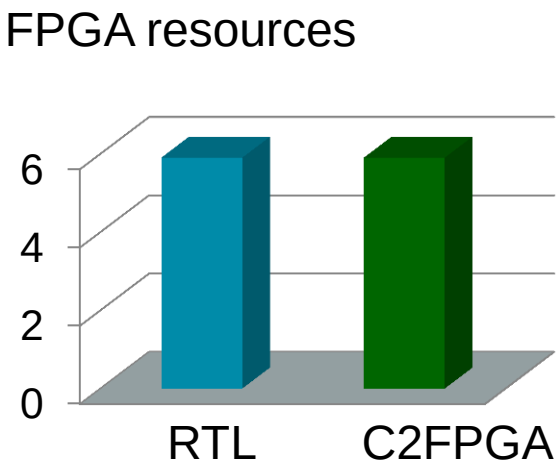
Quality of Results





FPGA: >38 times better performance than DSP video processor

QOR: C2FPGA equal to or better than RTL synthesis

Ease-of-use: C2FPGA 2x fewer lines of C code than DSP processor

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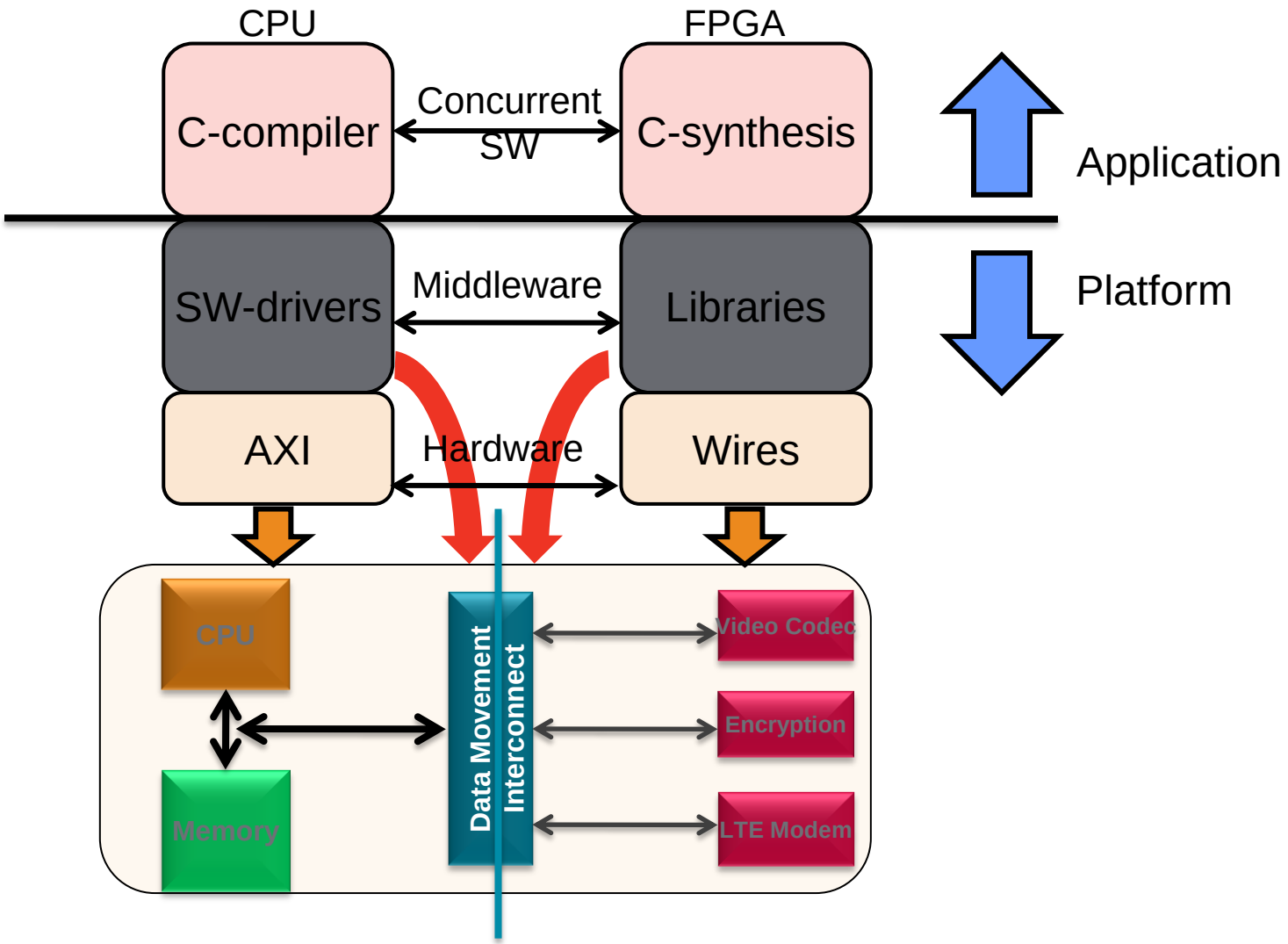
HW/SW Design Flow



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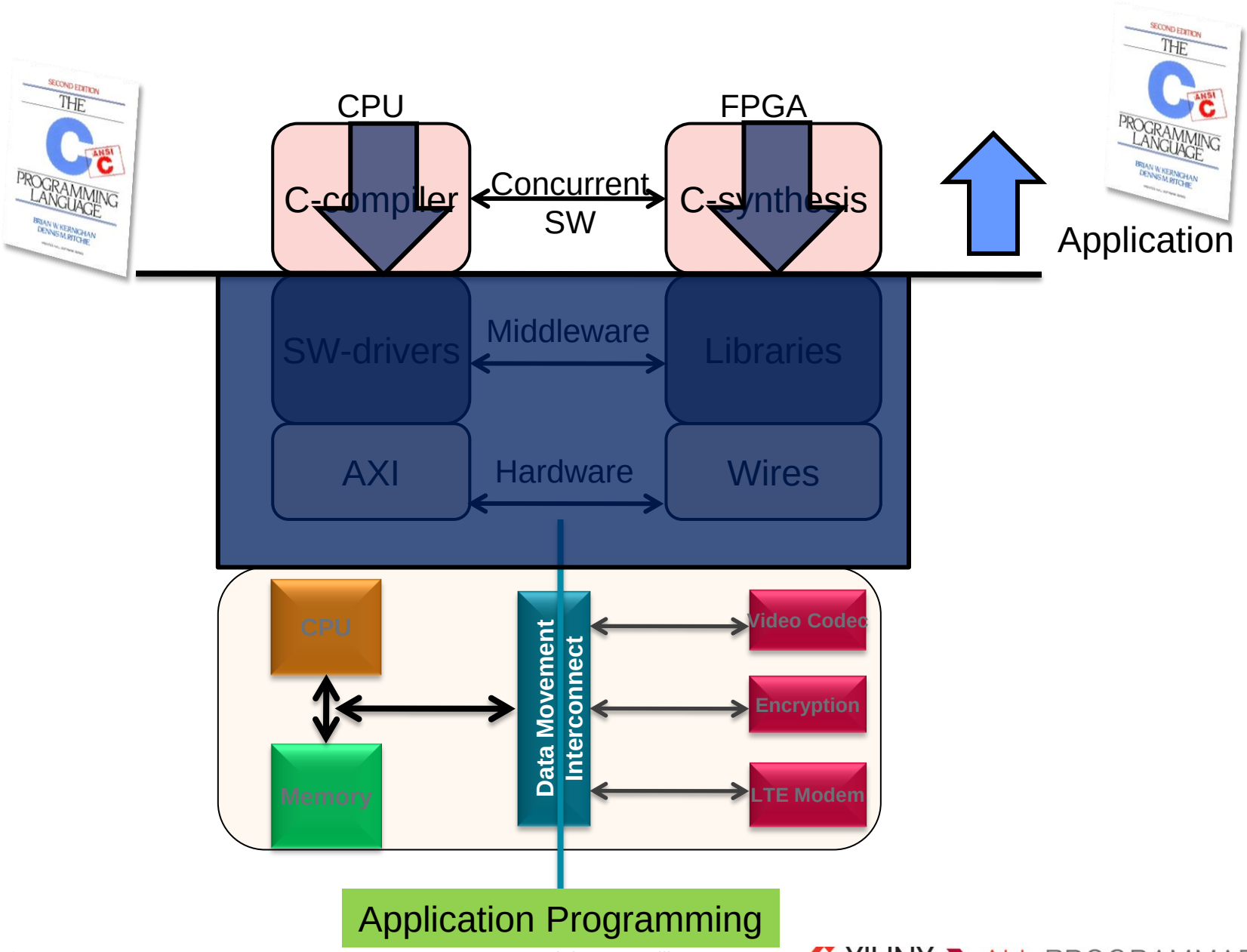
HW/SW Design Flow: SW Programmer View



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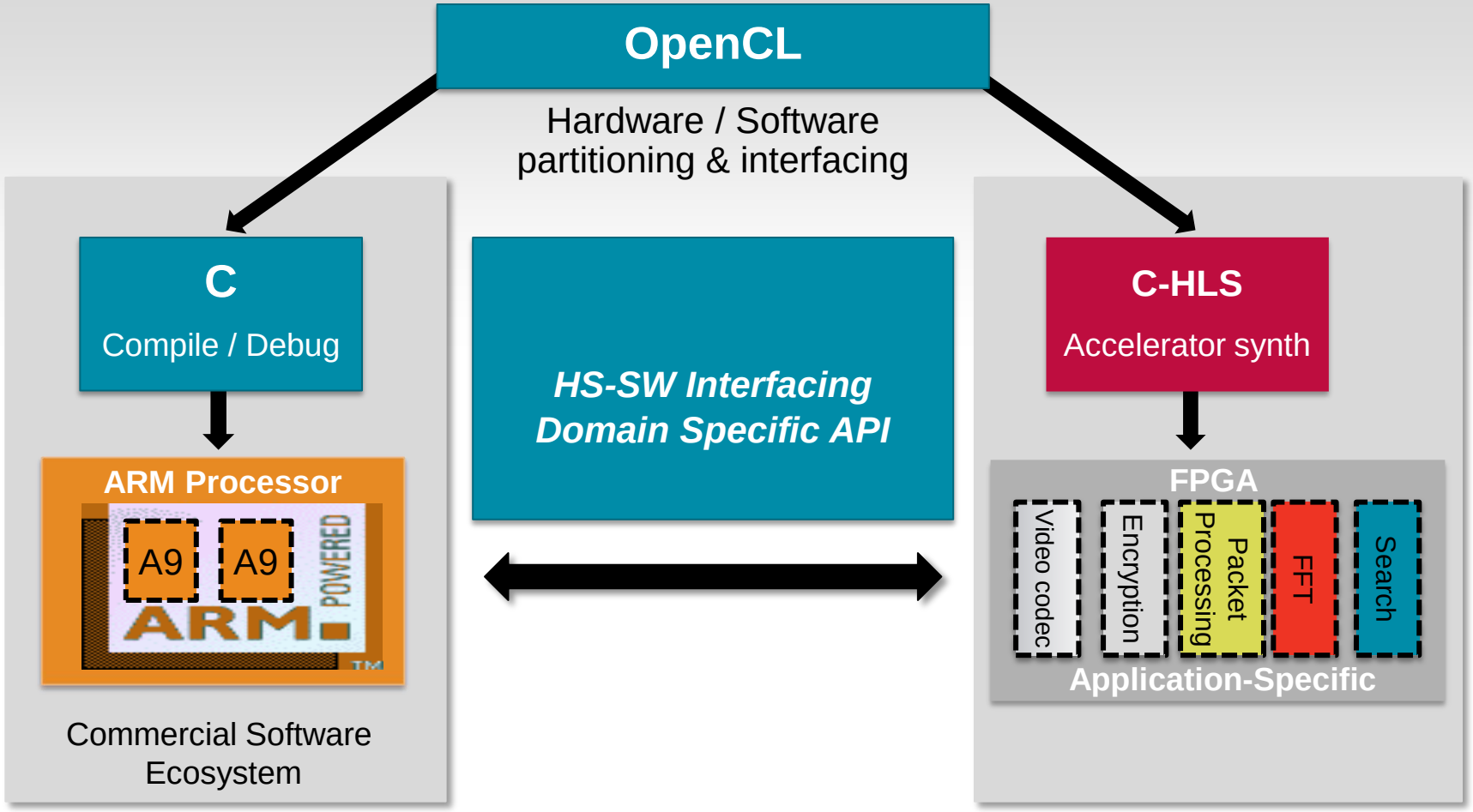
Towards Heterogeneous Multi-core



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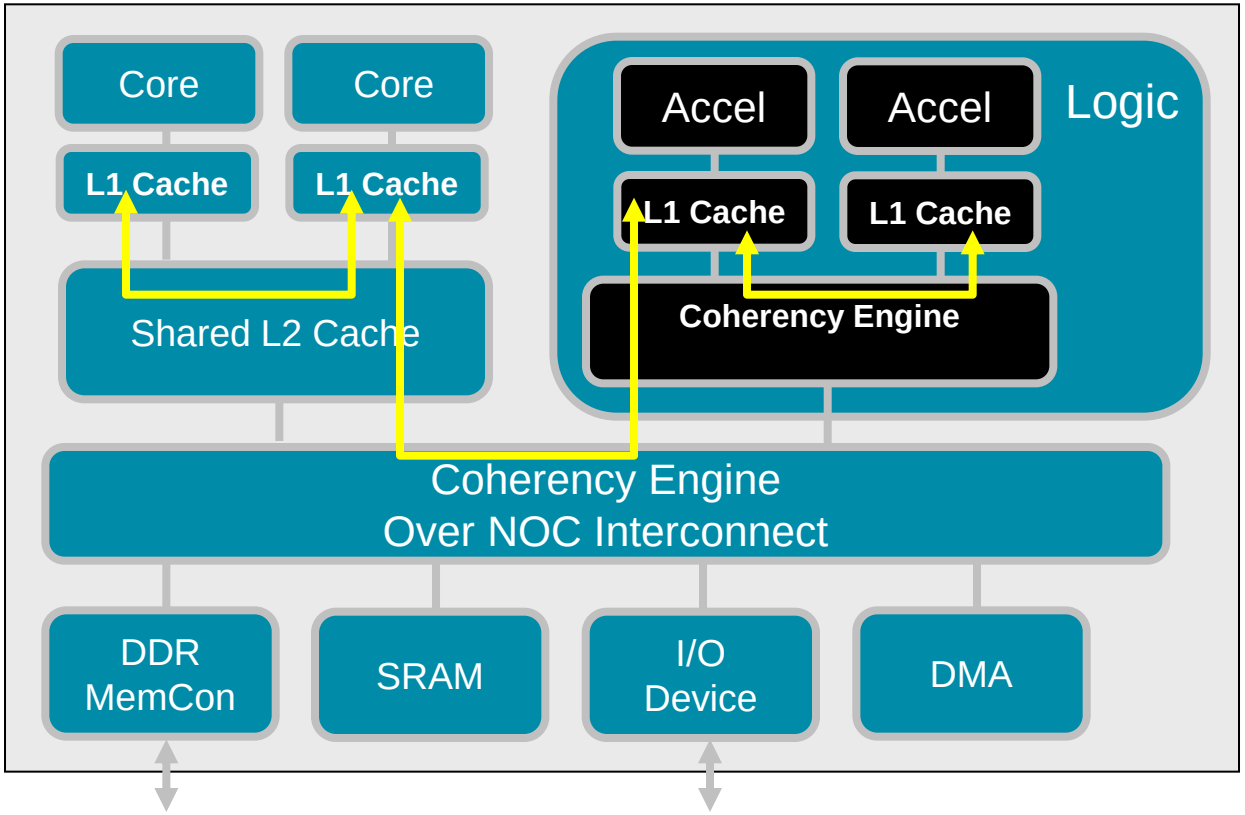
Programmable Platform: CPU + FPGA Peer Processing



Capabilities

- Coherent Caches for HW
- Coherent Caches for SW
- Coherency Management

Coherency Benefits:

- **Peer Processing**: Direct Cache-2-Cache data movement
- **Latency**: Very low latency access to CPU (FPGA) data
- **Usability**: No SW cache flush needed

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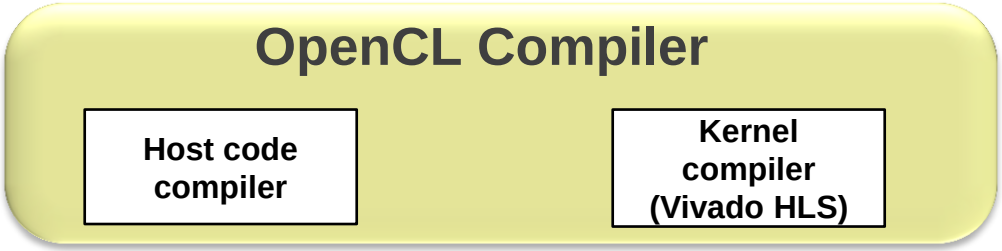
OpenCL Domain Specific Platforms

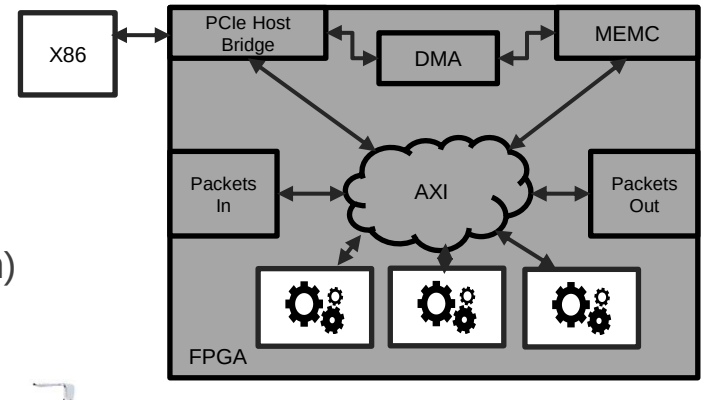
OpenCL SDK

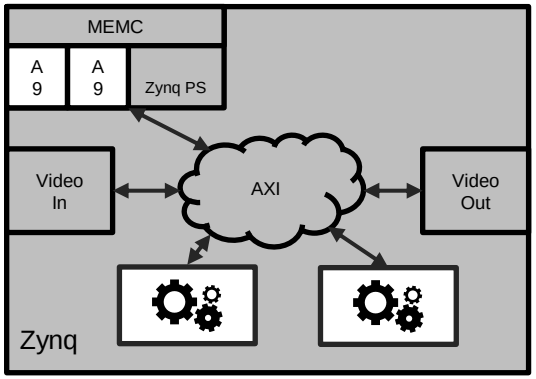
(Application Programming)



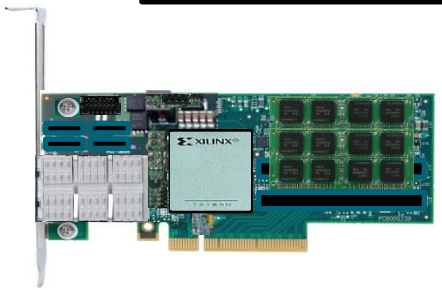
Base Systems

(Domain Customization)





FPGA Boards



Alphadata

QPI

ZED board

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Conclusions

- **More transistors, more performance, lower power**
- **Architecture Innovations to create Value**
  - Connectivity
  - Granularity
  - 3D Integration
- **All Programmable Platforms : heterogeneous and scalable**
  - Programmable IO, Memory, Interconnect, DSP, Micro
- **New Programming Abstractions that support**
  - Parallelism
  - Heterogeneity

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Now is a great time to be a design engineer!

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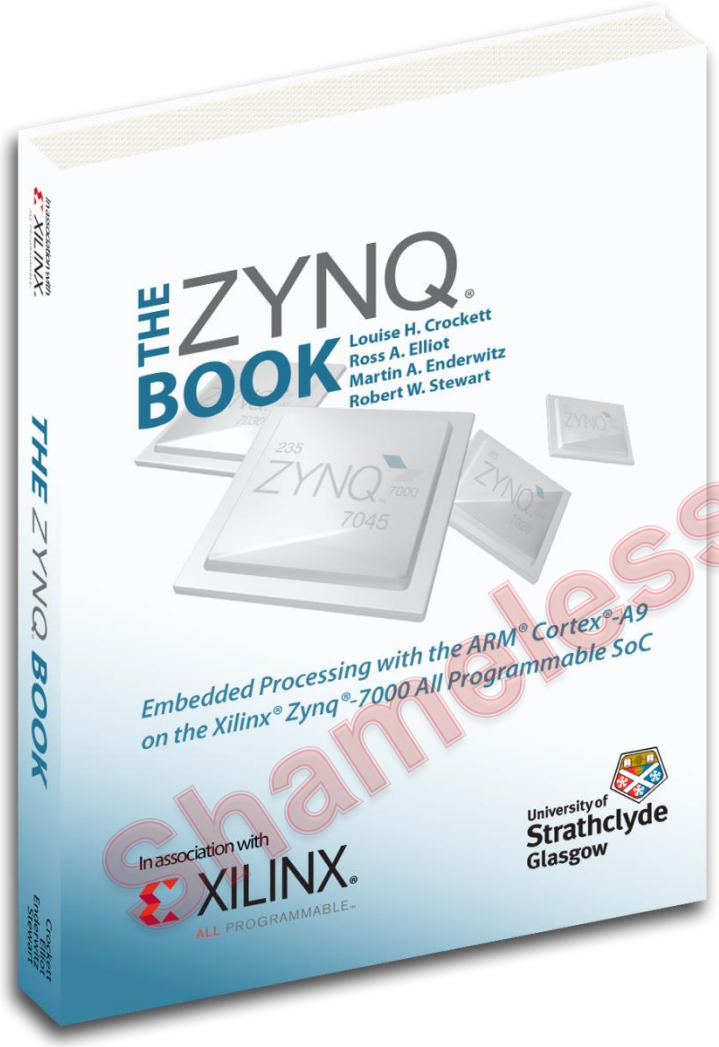
The Zynq Book

Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq All Programmable SoC



- **Hands-on introduction to Zynq for:**
  - Technical/non-technical managers
  - Hardware/software engineers
  - Academics and students

- **Book divided into three main sections**

1) High level introduction to Zynq

- What is it?
- What can I do with it?
- How do I use it?

2) Technical overview

- Embedded system, Zynq, AXI, IP design, HLS, System Design (Vivado)

3) Operating systems for Zynq

- Background, Linux overview, Linux on Zynq

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Free PDF of The Zynq Book

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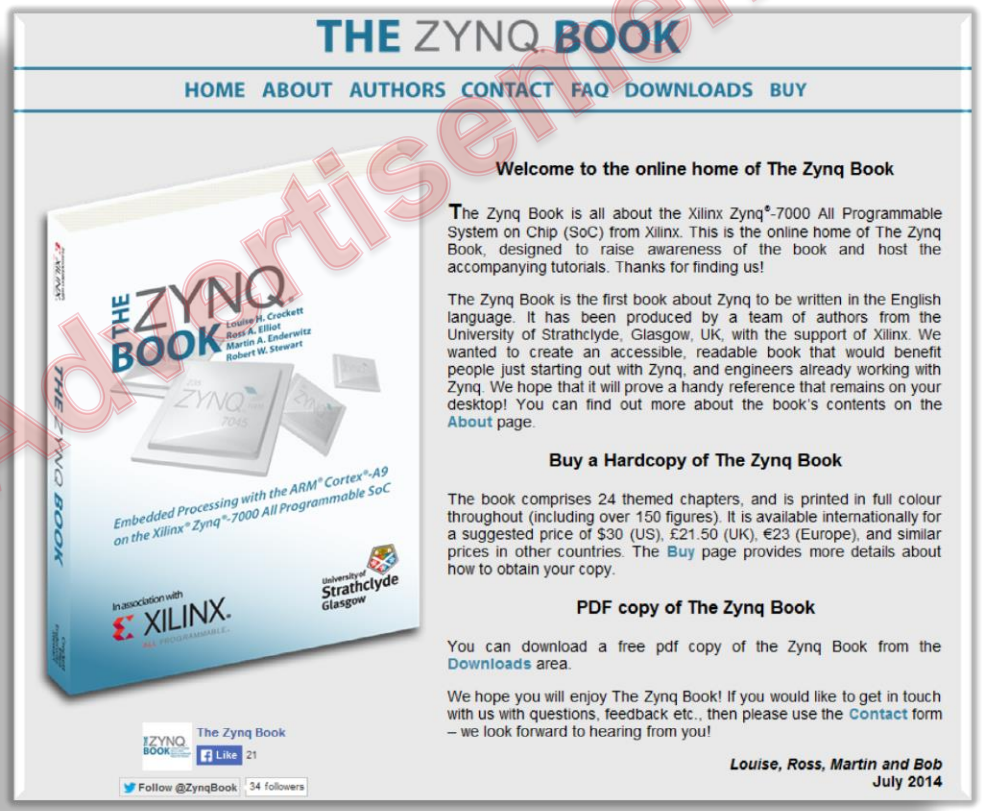

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