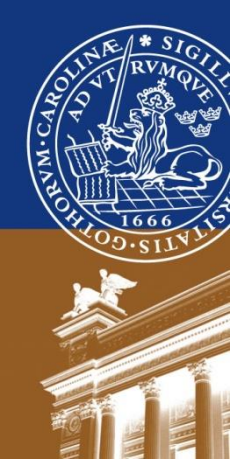


2014 SoS Workshop
Mixed-Signal IC Design

Presented by Pietro Andreani

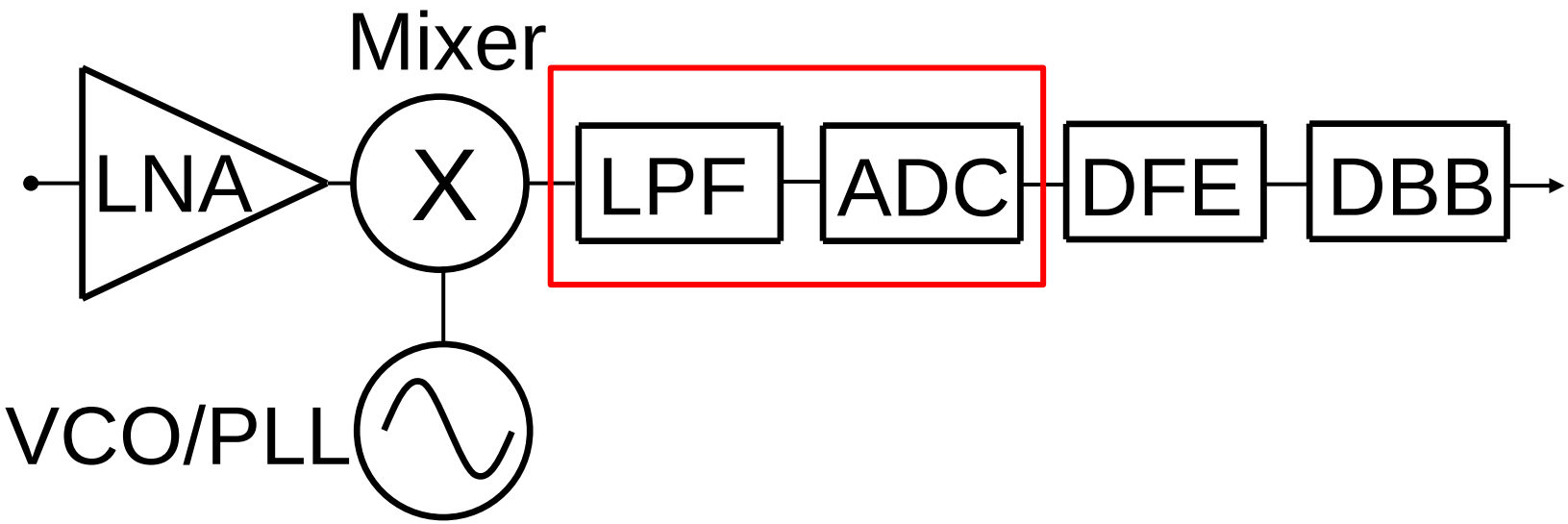
Department for Electrical and Information Technology
Lund University

Work performed in 2013-2014

- Filtering CT ΔΣ ACSs for LTE
  - Mattias Andersson
- An ultra-low-power CT ΔΣ ADC with SAR quantizer
  - Dejan Radjen (simulations)
- CT ΔΣ ADC for LTE
  - Xiaodong Liu (not shown)
- A digital PLL
  - Ping Lu (simulations)
- Two class-D VCOs
  - Luca Fanori
- A reconfigurable wideband VCO
  - Ahmed Mahmoud (not shown)

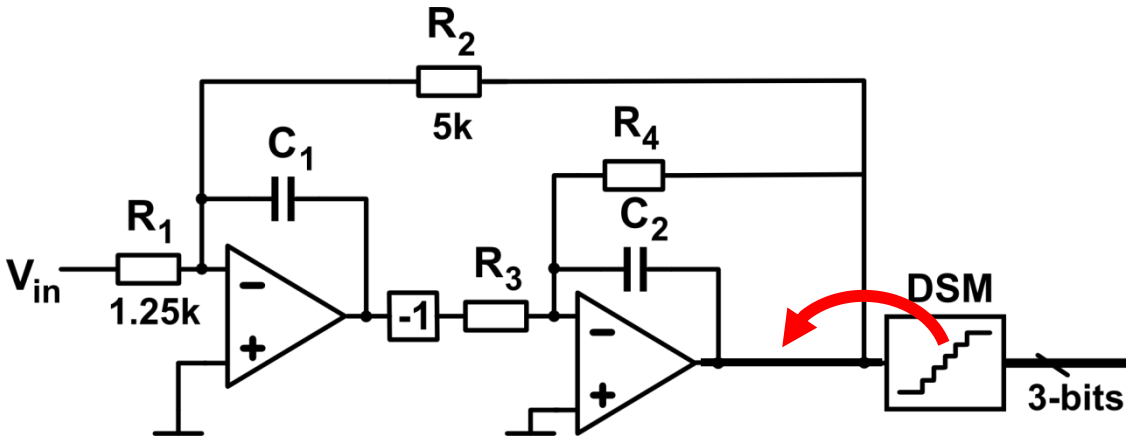
Merging LPF and ADC

Mattias Andersson



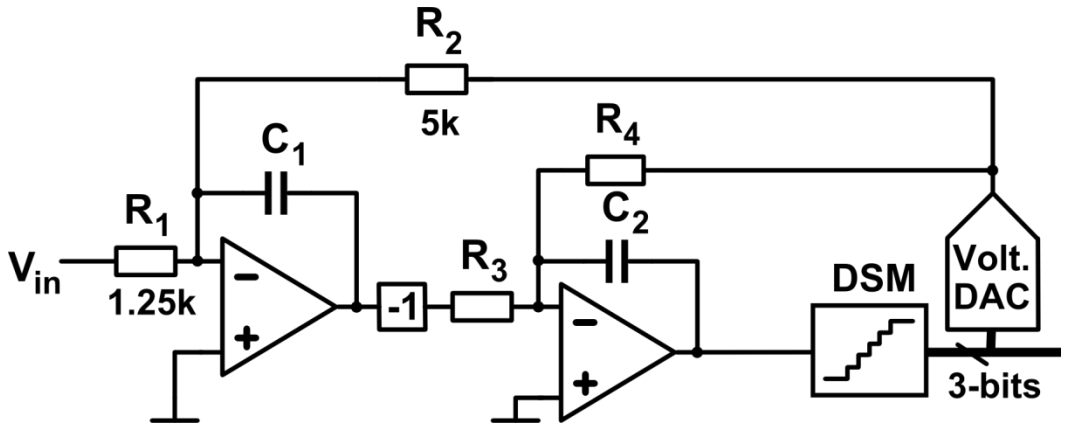
Channel-Select Filter + CT ΔΣ ADC

Tow-Thomas
2nd-order CSF



Noise from DSM is 2nd-order shaped by global feedback

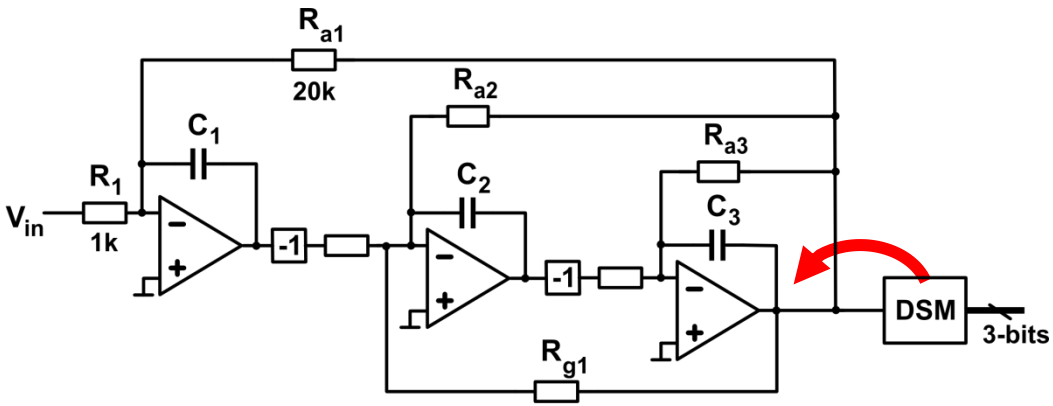
ESSCIRC ’13
SoS workshop ’13



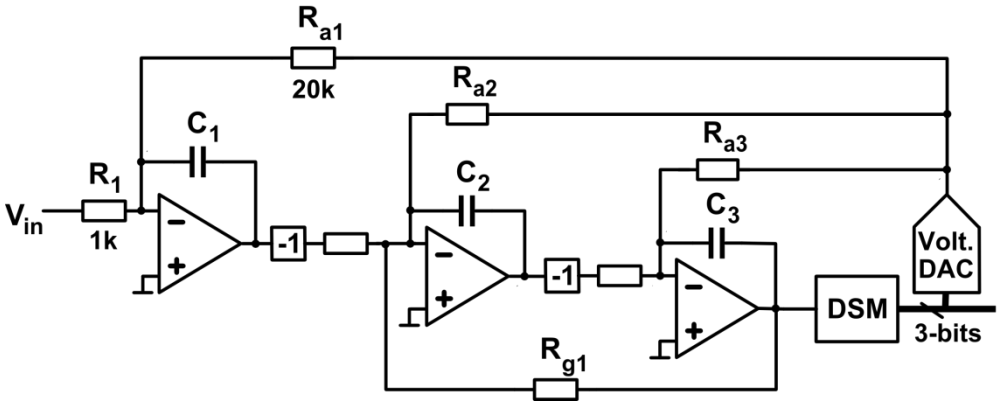
Improved Version: Filtering CT ΔΣ ADC Supporting LTE 2x20MHz

3rd-order CSF

2nd-order DSM

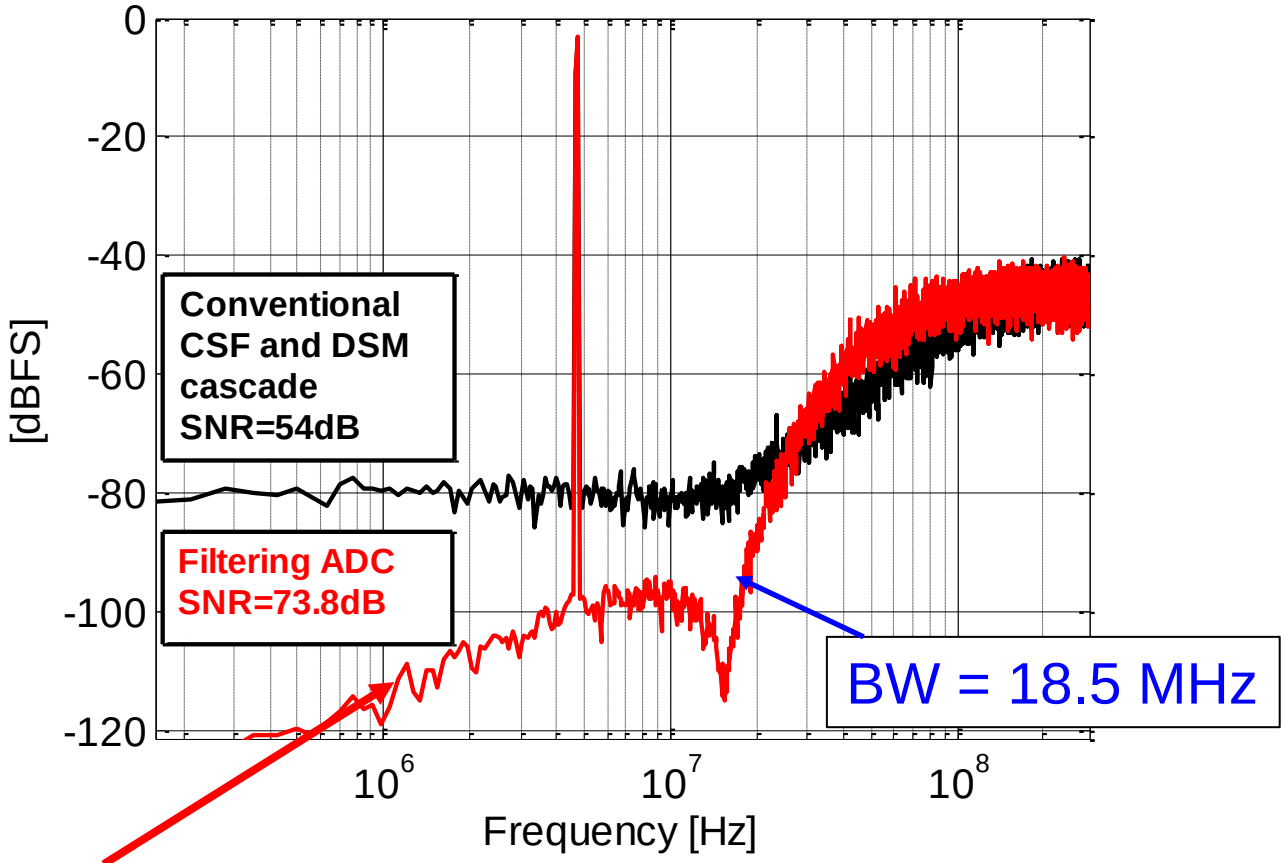


JCCS July 2014



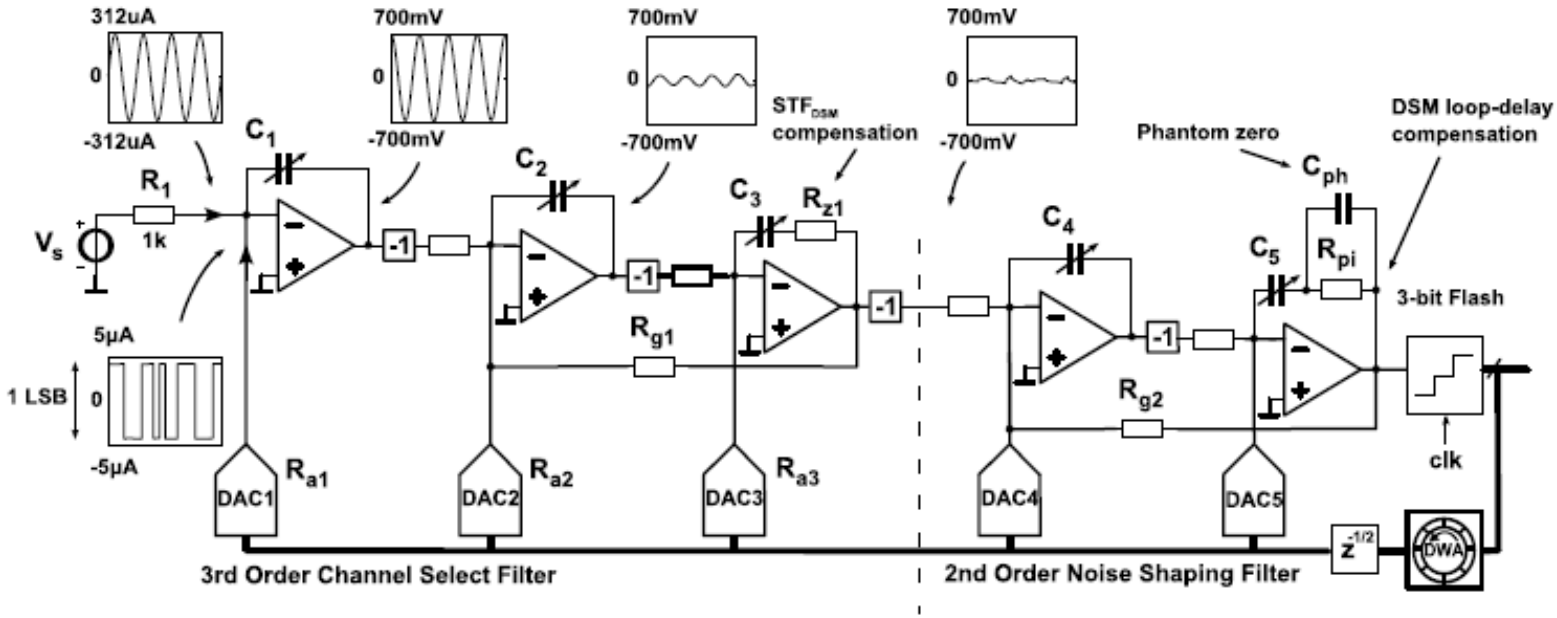
Noise from DSM shaped by three zeroes in CSF

Simulation with white noise at DSM input



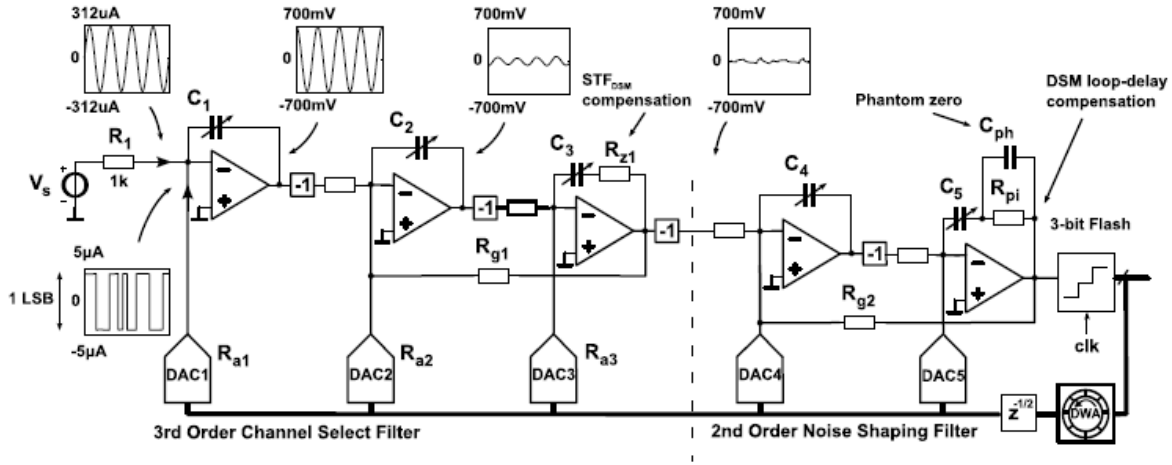
DSM noise suppressed by three zeroes → 19dB gained!

Filtering ADC



- 3rd-order Chebychev CSF, 9.0/18.5 MHz BW
- 2nd-order DSM, 3-bit DACs, f_s=288/576 MHz

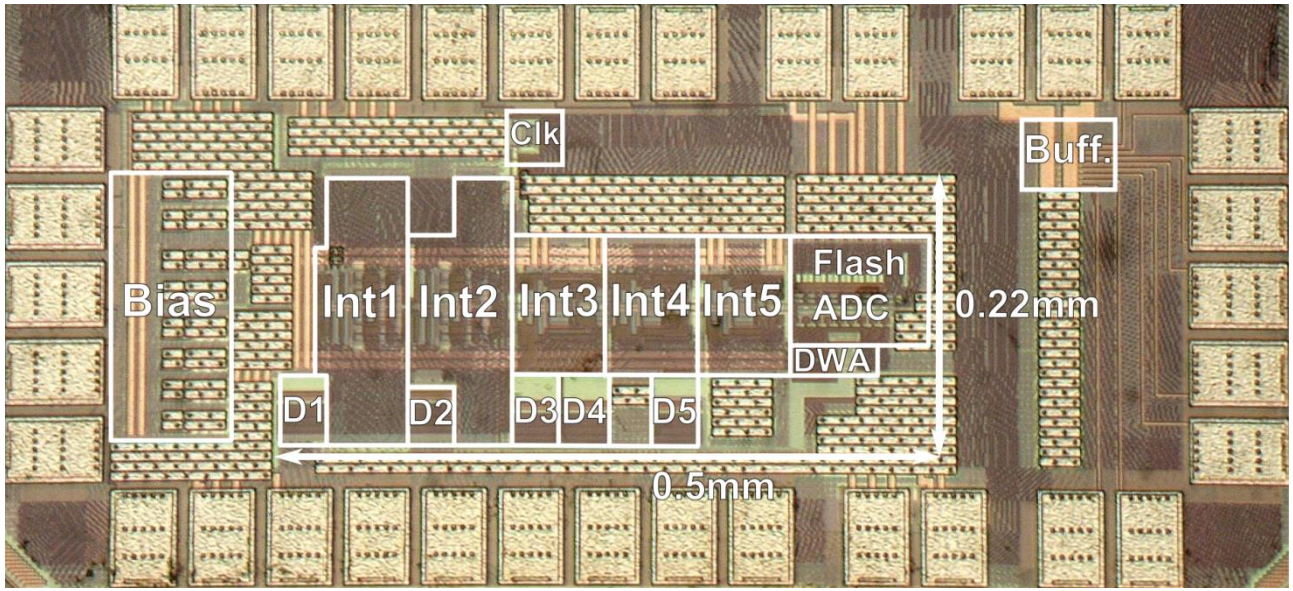
Filtering ADC vs plain ΔΣ ADC



Topologically identical! – However:

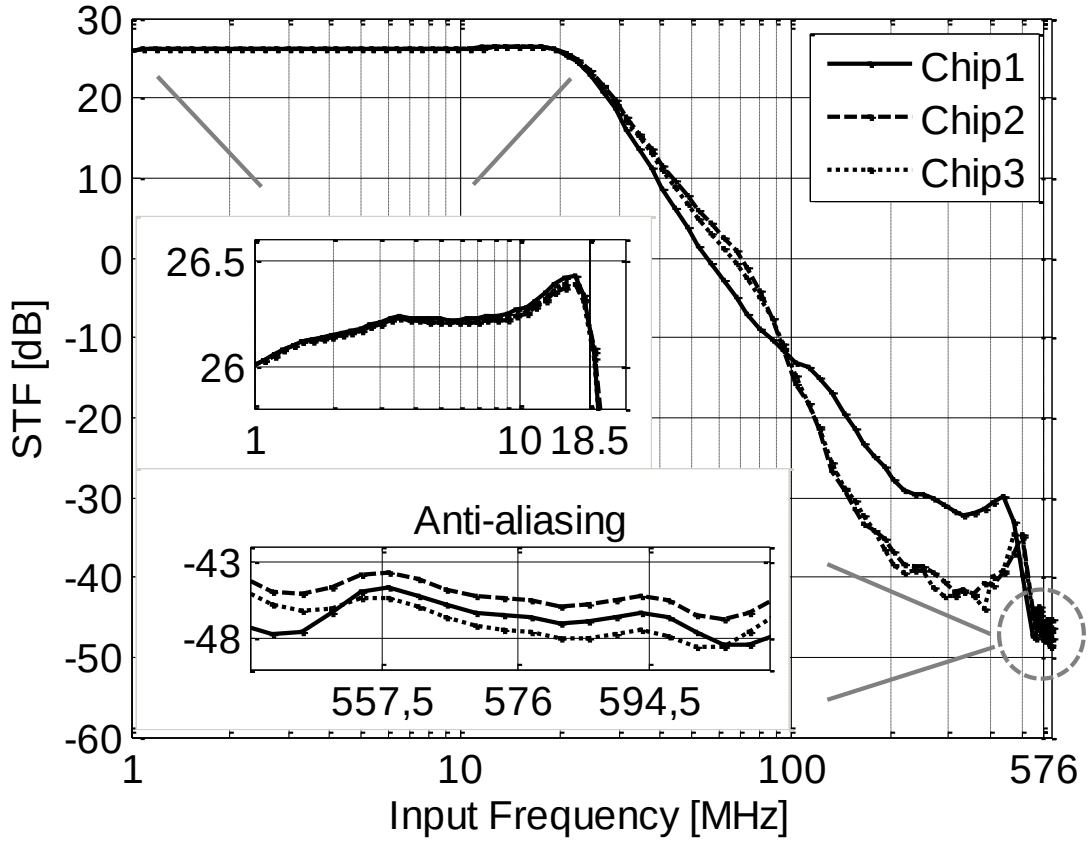
- 5th-order DSM
  - 5 poles at high frequencies to maximize SQNR
- Filtering ADC:
  - 2 poles at low frequencies for filtering
  - 3 poles at high frequencies for SQNR

Chip photograph

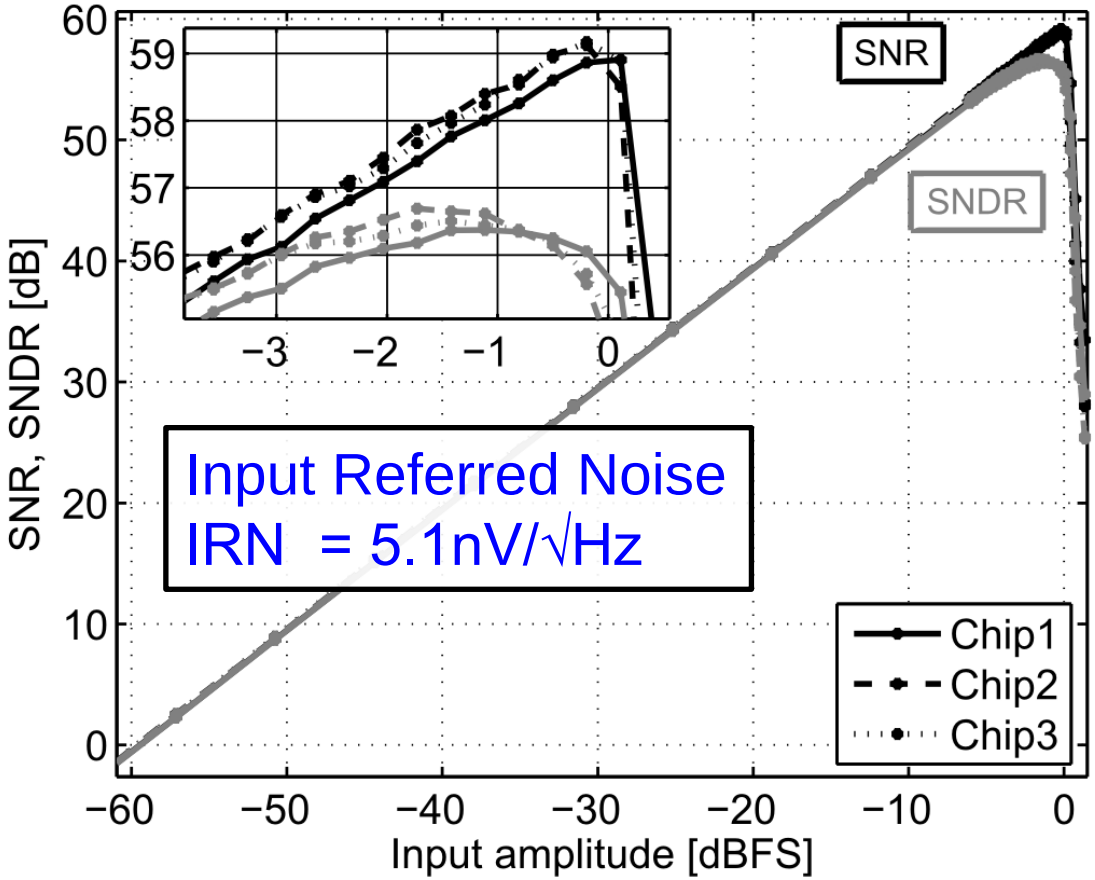


- ST 65nm CMOS
- V_{dd}=1.2V, I_{dd}= 9.4mA (11.3mW)
- f_s=288MHz, BW=9MHz
- Core area 0.5x0.22mm^2

Signal Transfer Function in 2xLTE20

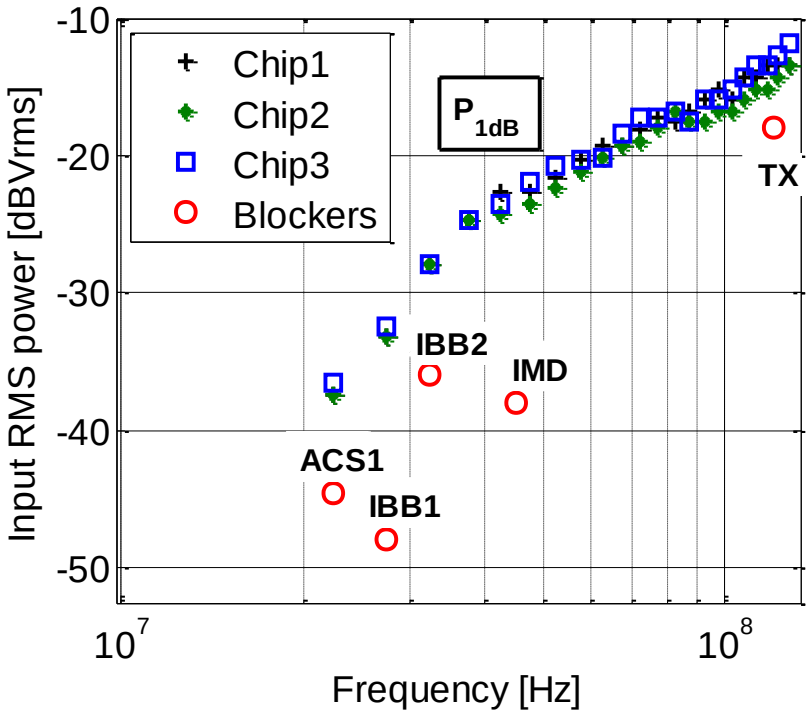


SNR and SNDR in 2xLTE20

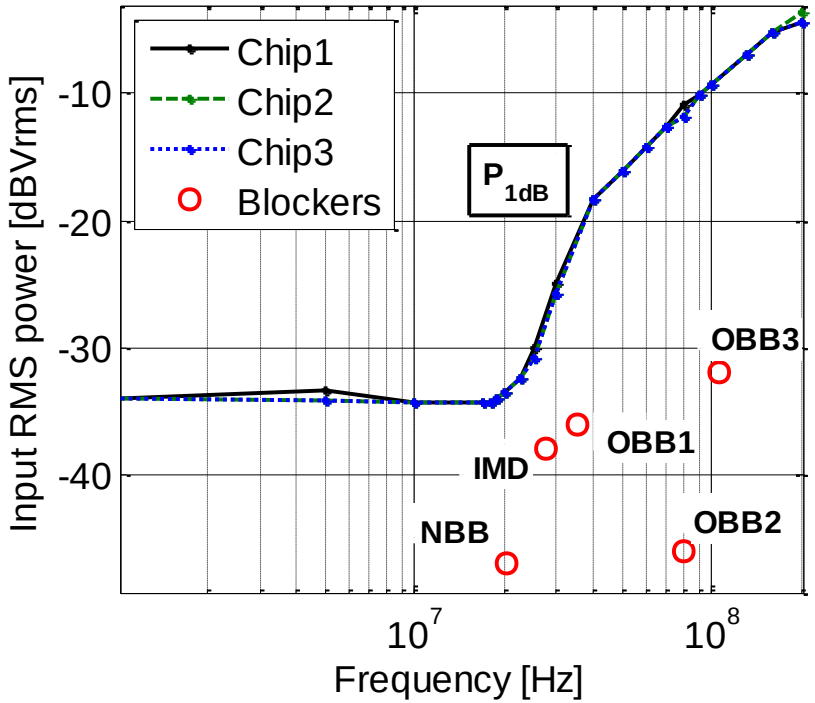


Tolerance to blockers, 2xLTE20

5MHz SC-FDMA blockers



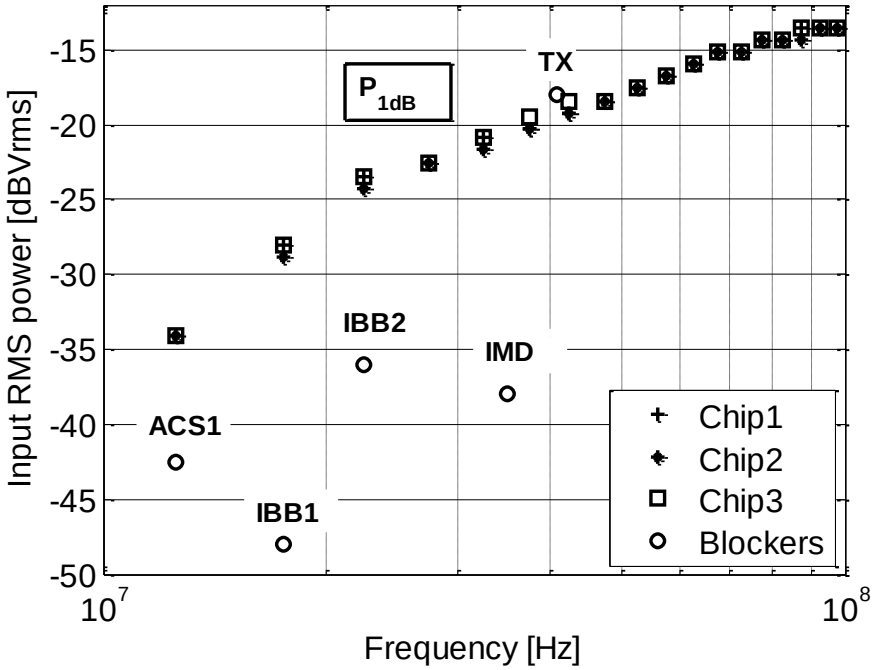
CW blockers



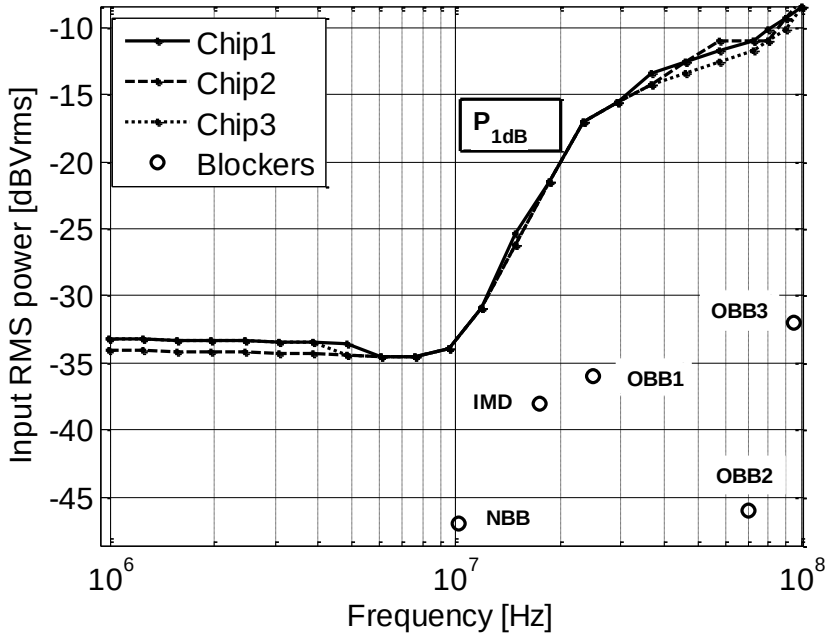
- P_{1dB} vs. blockers (P_{1dB} = blocker power for which in-band noise increases by 1dB)
- Assuming 10mS front-end and -54dB TX-to-RX in duplexer

Tolerance to blockers, LTE20

5MHz SC-FDMA blockers



CW blockers



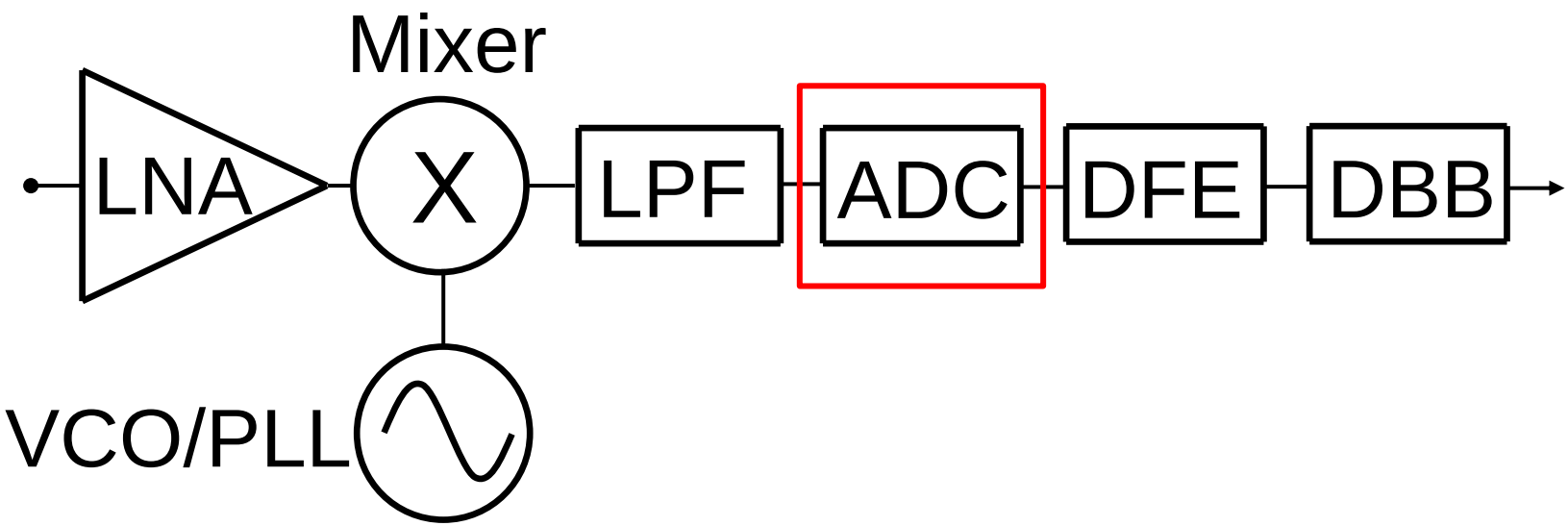
- P_{1dB} vs. blockers
- Assuming 10mS front-end and -54dB TX-to-RX in duplexer

State-of-the-art in filtering ADCs

Parameter	**Paper V**	**Paper IV**	Philips ISSCC'04	Sosio ESSCIRC'11	Rajan ISSCC'14
fs (MHz)	**576**	**288**	64	405	256
BW (MHz)	**18.5**	**9**	1	6	2
SNDR (dB)	**56.4**	**68.4**	59	74.6	74.4
Filter order	**3**	**2**	1	2	2
Avg. IRN in BW ($nV/\sqrt{Hz}$)	**5.1**	**8.1**	280	–	40
Gain setting (dB)	**26**	**12**	0	–	0
In-band IIP3 (dBV_{rms})	**-8.5**	**11.5**	19	–	24
Out-of-band IIP3 (dBV_{rms})	**20**	**27**	–	–	34
f_{-3dB} (MHz)	**25.0**	**16.9**	3	–	4
Power (mW)	**7.9**	**11.3**	2	54	5
Tech. (nm)	**65**	**65**	180	90	130
Vdd (V)	**1.2**	**1.2**	1.8	1.2-1.8	1.4
DR at BW×4 (dB)	**82**	**80**	65	90	90.5
FOM1 at BW×4 (fJ/c.)	**21**	**77**	700	180	45
FOM2, OOB IIP3 (aJ)	**4**	**7**	–	–	15

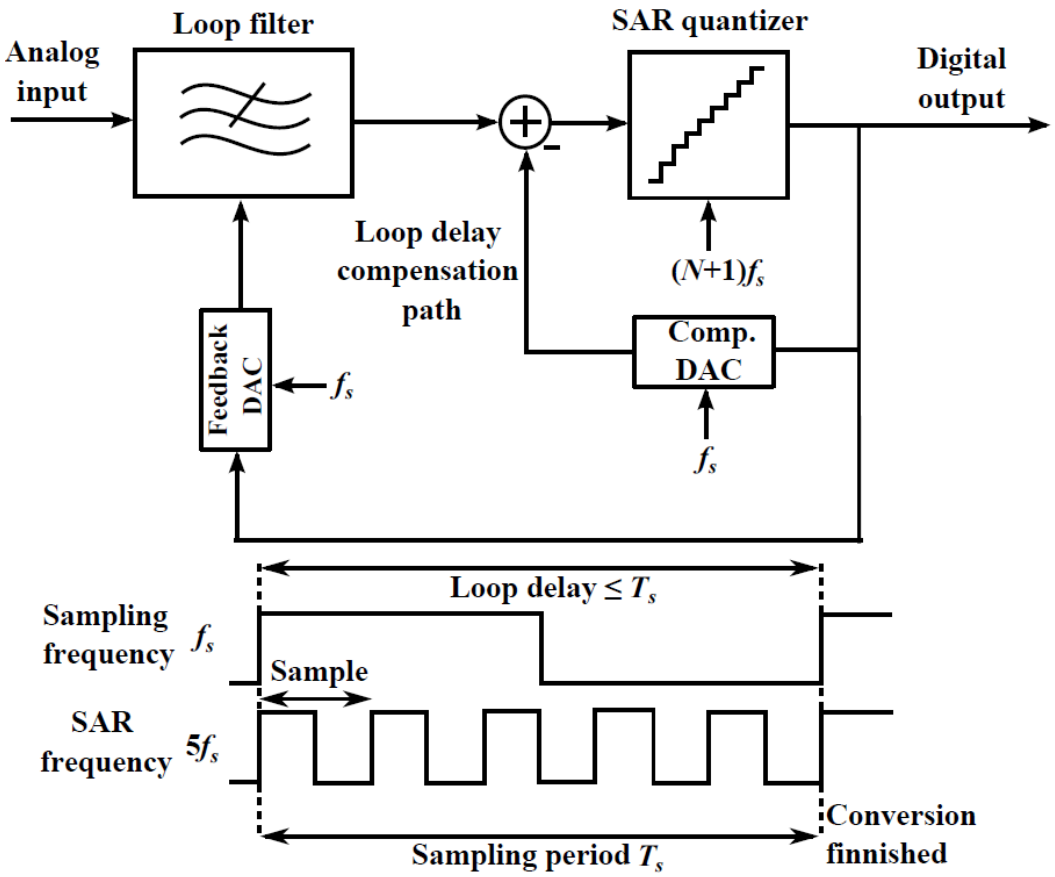
A 2nd-order CT ΔΣ modulator with an SAR quantizer

Dejan Radjen



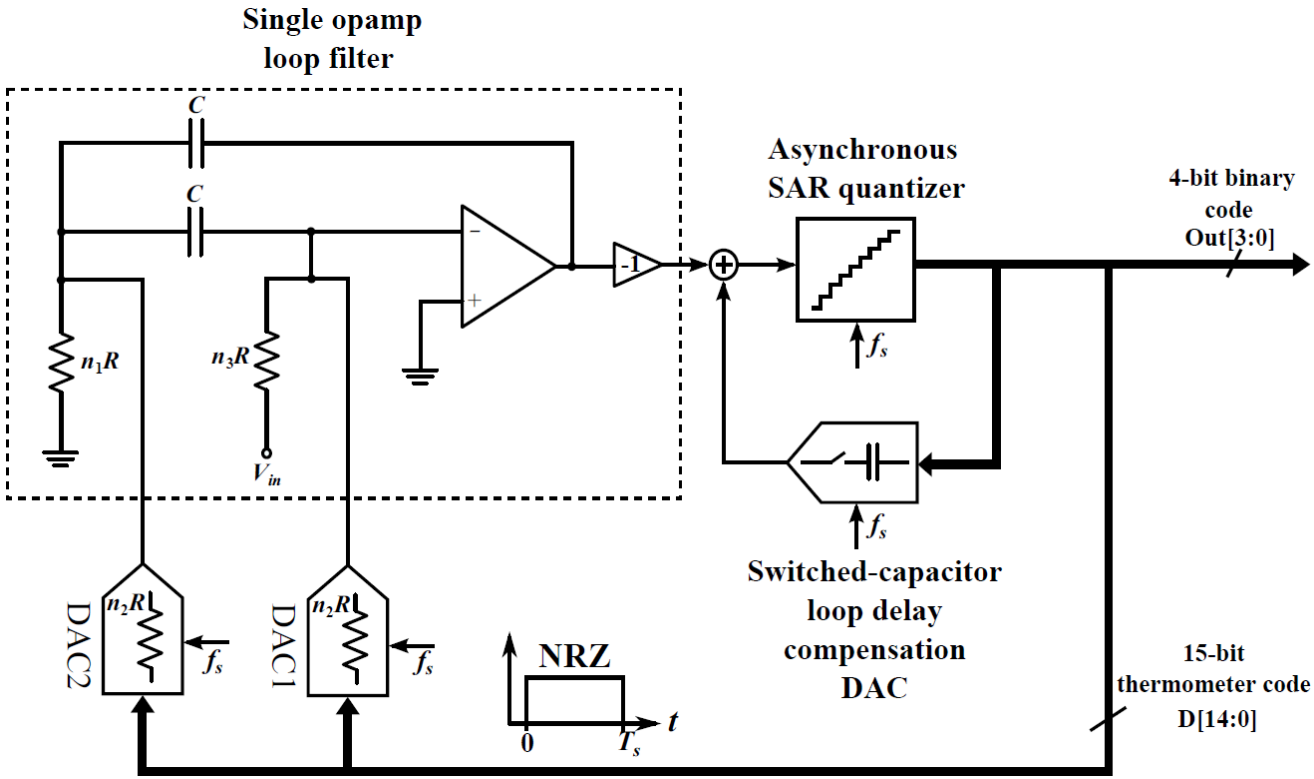
Part of a large SSF project, ”Wireless Communication for Ultra Portable Devices (UPD)”, lead by Prof. Henrik Sjöland

Architecture of ΔΣ modulator



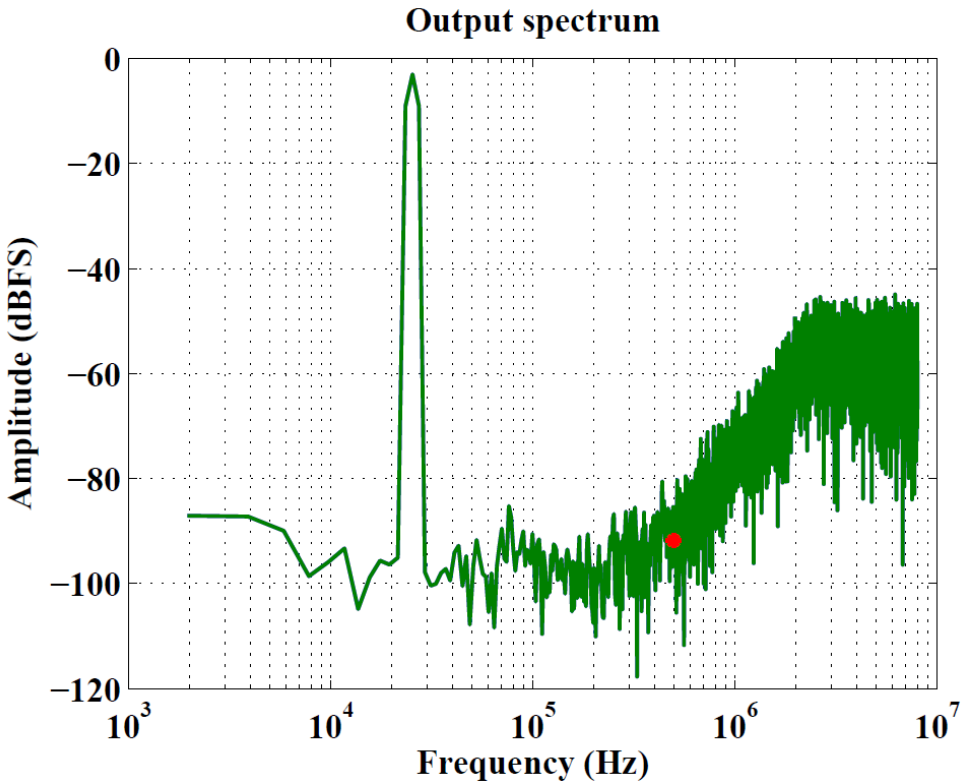
- ΔΣ modulator with a 4-bit SAR quantizer
- SAR more power efficient than standard flash quantizers
- Generation of clock at $5f_s$ avoided with asynchronous control

Details of ΔΣ modulator



- 2nd-order loop filter with single opamp to save power
- Resistive feedback DACs with NRZ pulses

Simulation results

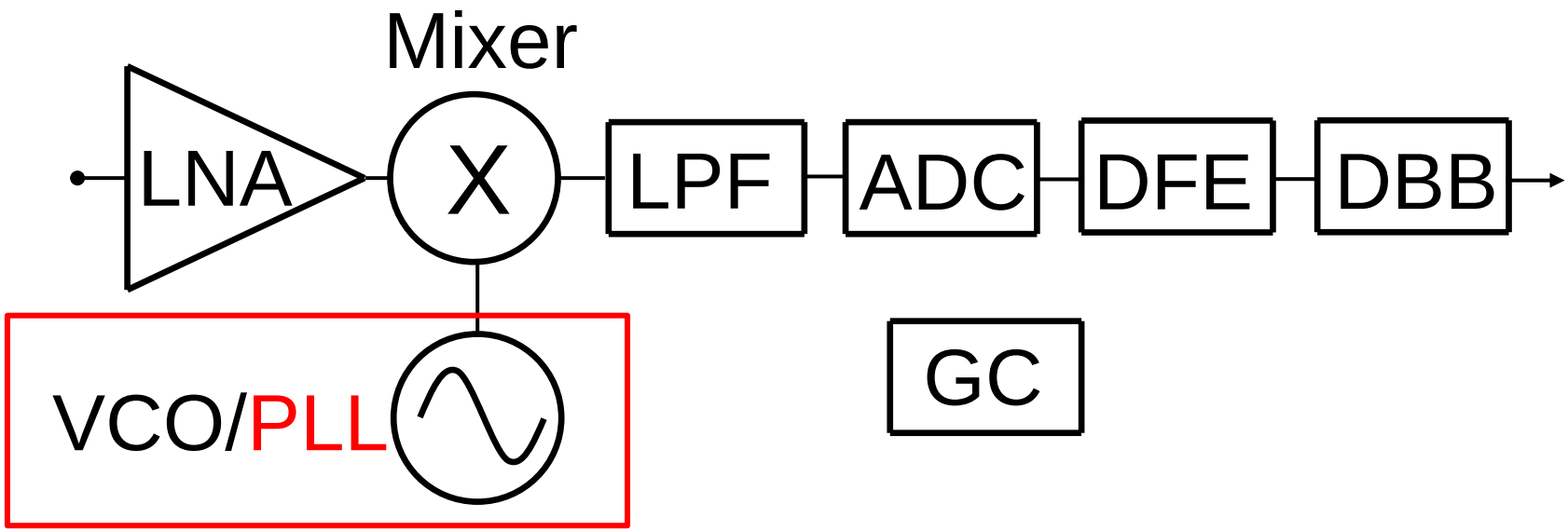


Performance summary	
Parameter	**Simulated performance**
Technology	65 nm CMOS
Supply voltage	800 mV
Signal bandwidth	500 kHz
Maximum input amplitude	200 mV differential
Clock frequency	16 MHz
SNDR	65 dB
Power consumption	69 µW
Figure of merit	47 fJ/conv

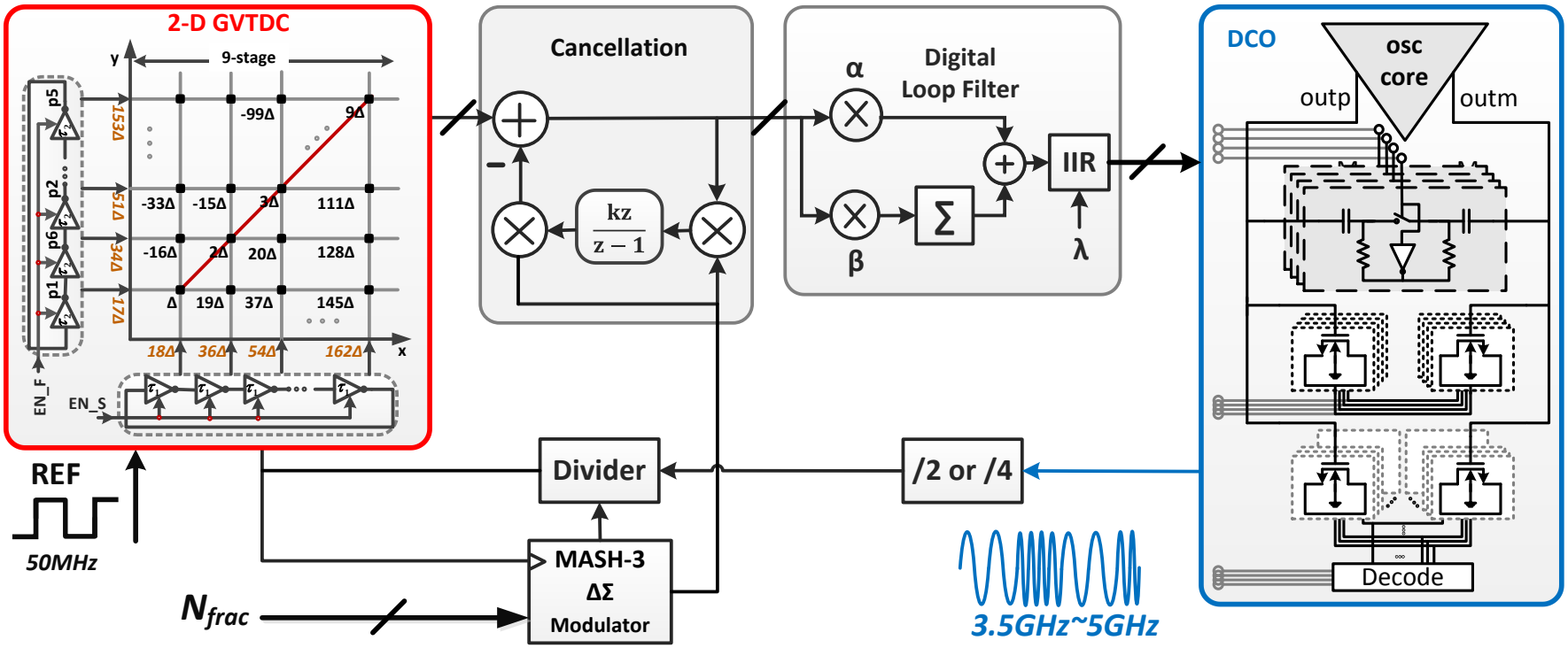
- Unfortunately, unstable in real life due to impact of layout parasitics
- Redesign ongoing

Digital PLL

Ping Lu



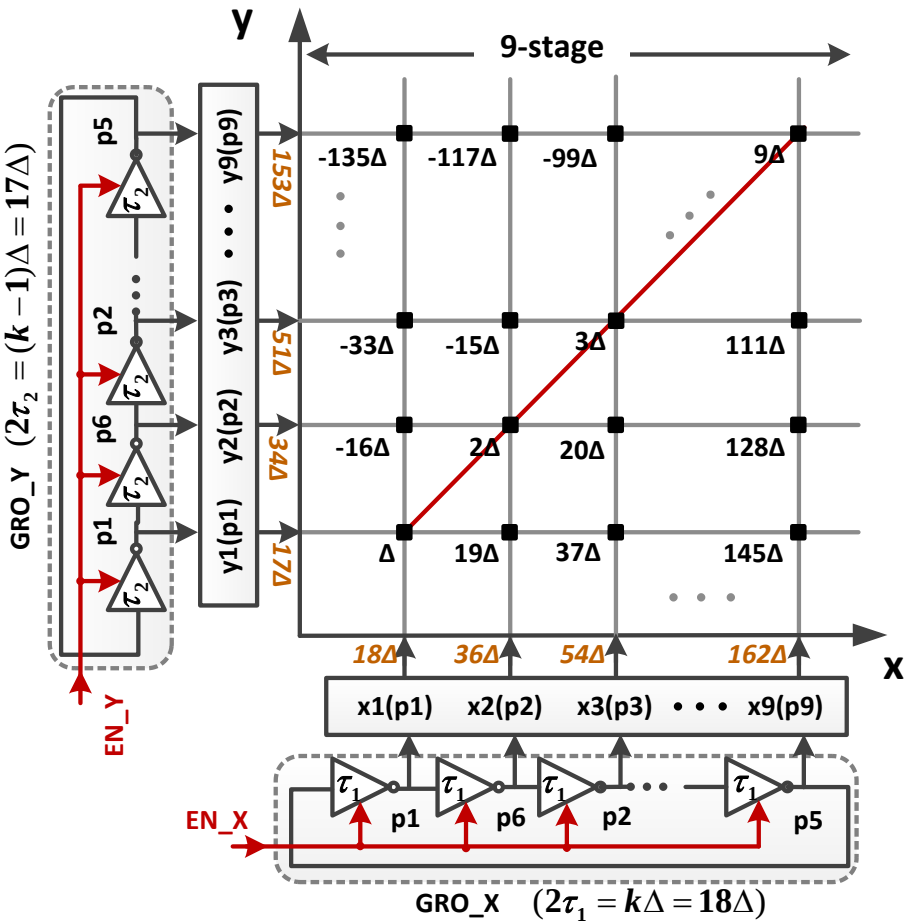
Digital PLL


2-D GVTDC
9-stage
y
x
p5
p2
p6
p1
EN_F
EN_S
153Δ
51Δ
34Δ
17Δ
-99Δ
9Δ
-33Δ
-15Δ
3Δ
111Δ
-16Δ
2Δ
20Δ
128Δ
Δ
19Δ
37Δ
145Δ
18Δ
36Δ
54Δ
162Δ
Cancellation
kz
z − 1
Digital
Loop Filter
α
β
Σ
IIR
λ
DCO
osc
core
outp
outm
Decode
REF
50MHz
Divider
/2 or /4
MASH-3
ΔΣ
Modulator
Nfrac
3.5GHz~5GHz

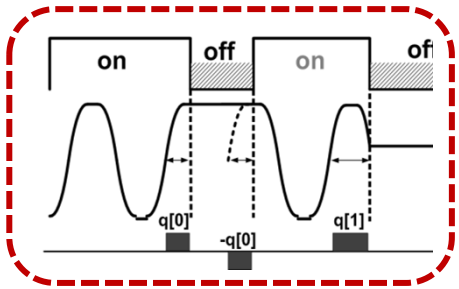
Time-to-digital converter (TDC)

2-D gated-ring-oscillator (GRO) Vernier TDC

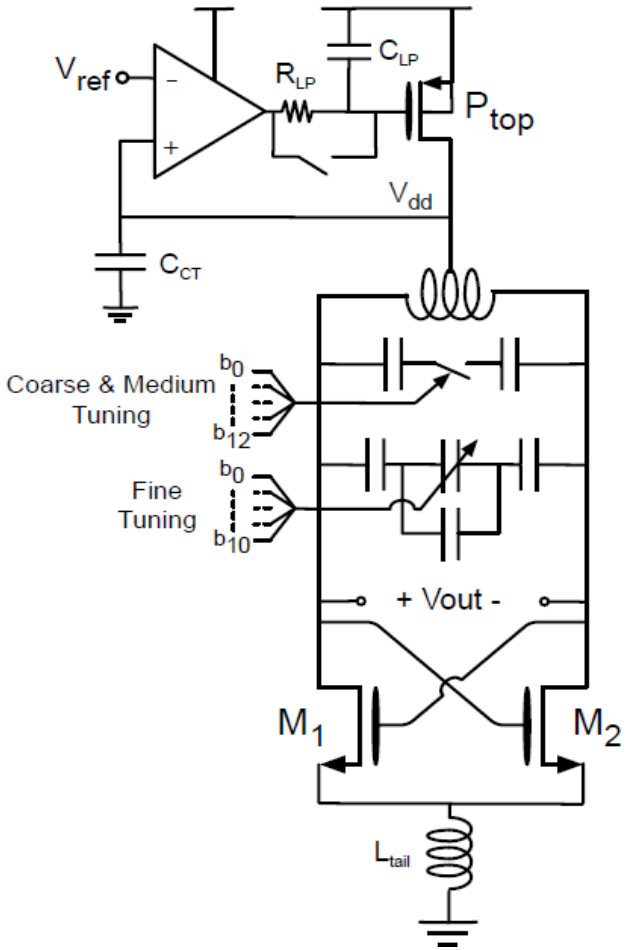
RFIC 2013

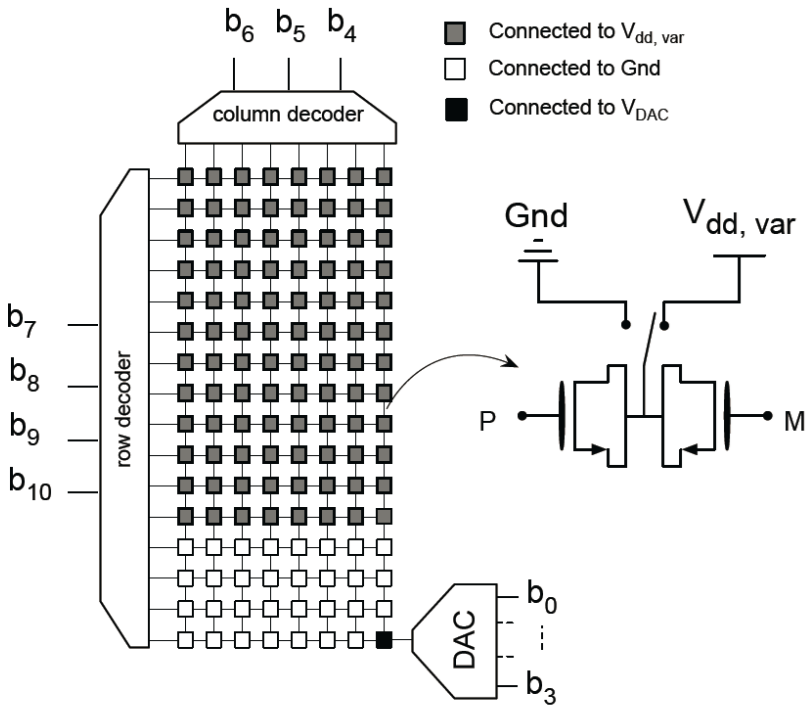


- **GRO → shaping of quantization noise**
- **2-D → large detection range, low latency**

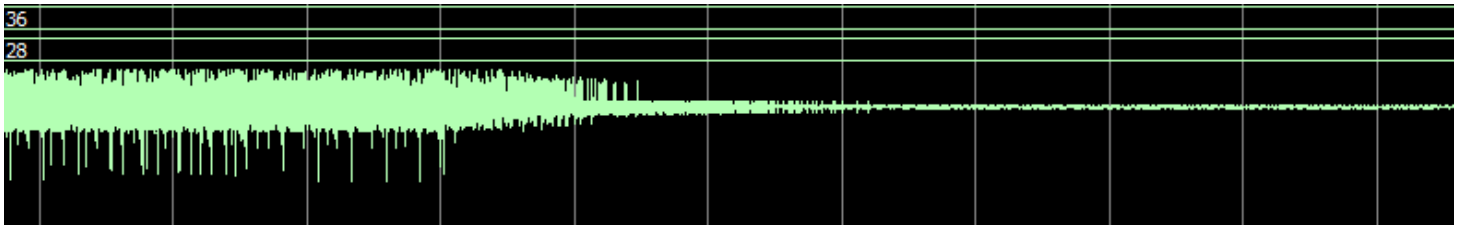


Class-D DCO


V_{ref}
R_{LP}
C_{LP}
P_{top}
V_{dd}
C_{CT}
Coarse & Medium Tuning
b_0
b_{12}
Fine Tuning
b_0
b_{10}
+ Vout -
M_1
M_2
L_{tail}

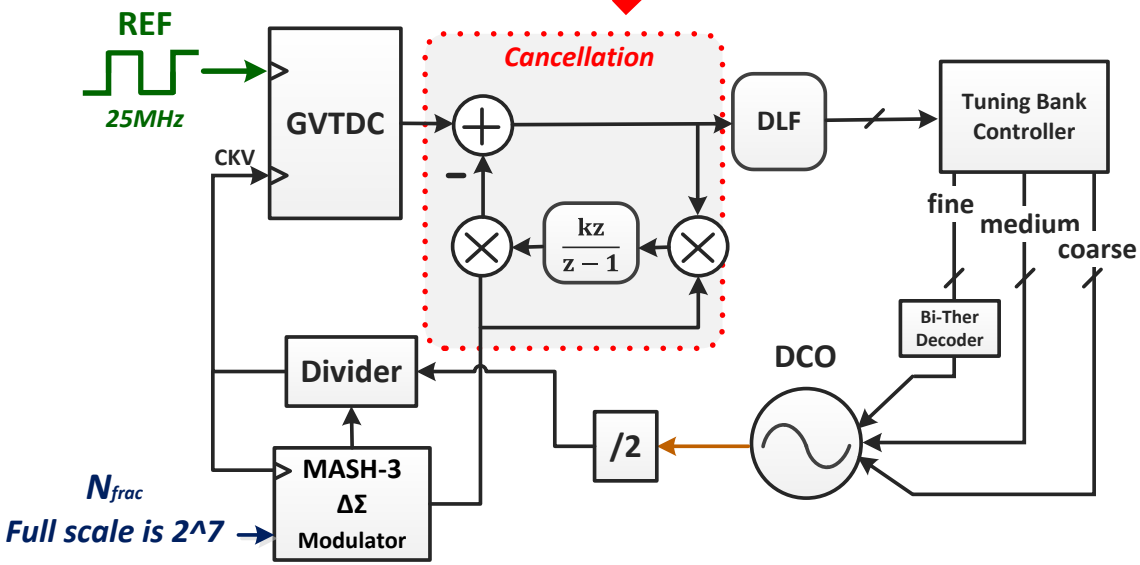

b_6 b_5 b_4
column decoder
Connected to $V_{dd, var}$
Connected to Gnd
Connected to V_{DAC}
b_7
b_8
b_9
b_{10}
row decoder
Gnd
$V_{dd, var}$
P
M
DAC
b_0
b_3

Noise cancellation

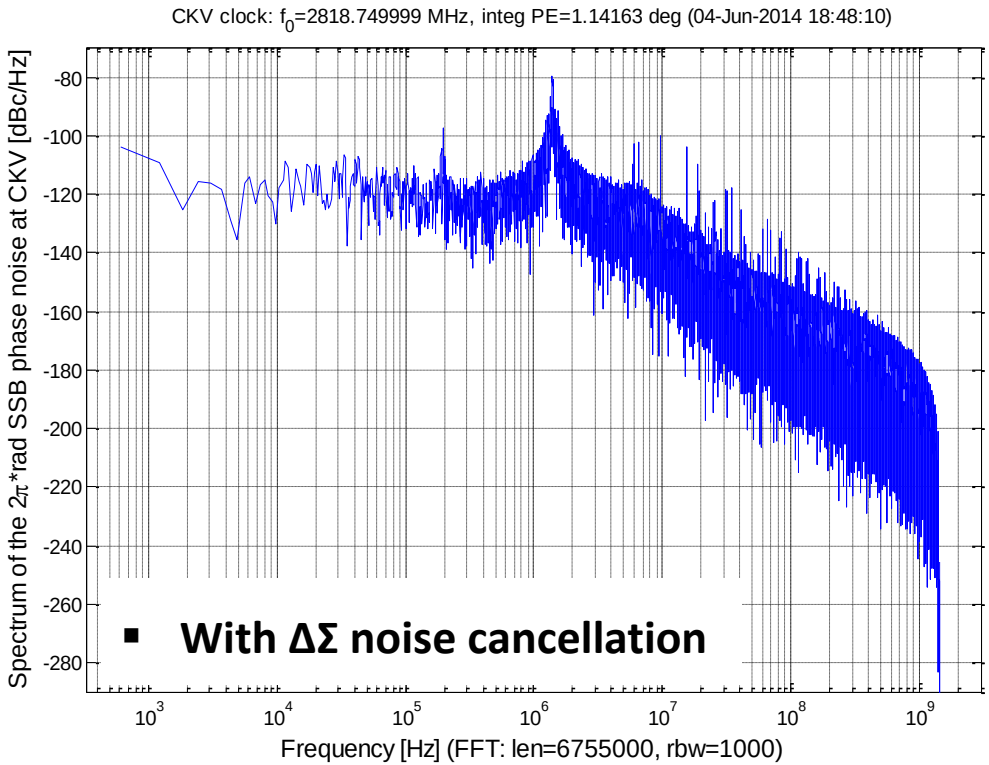


Cancellation off

Cancellation on

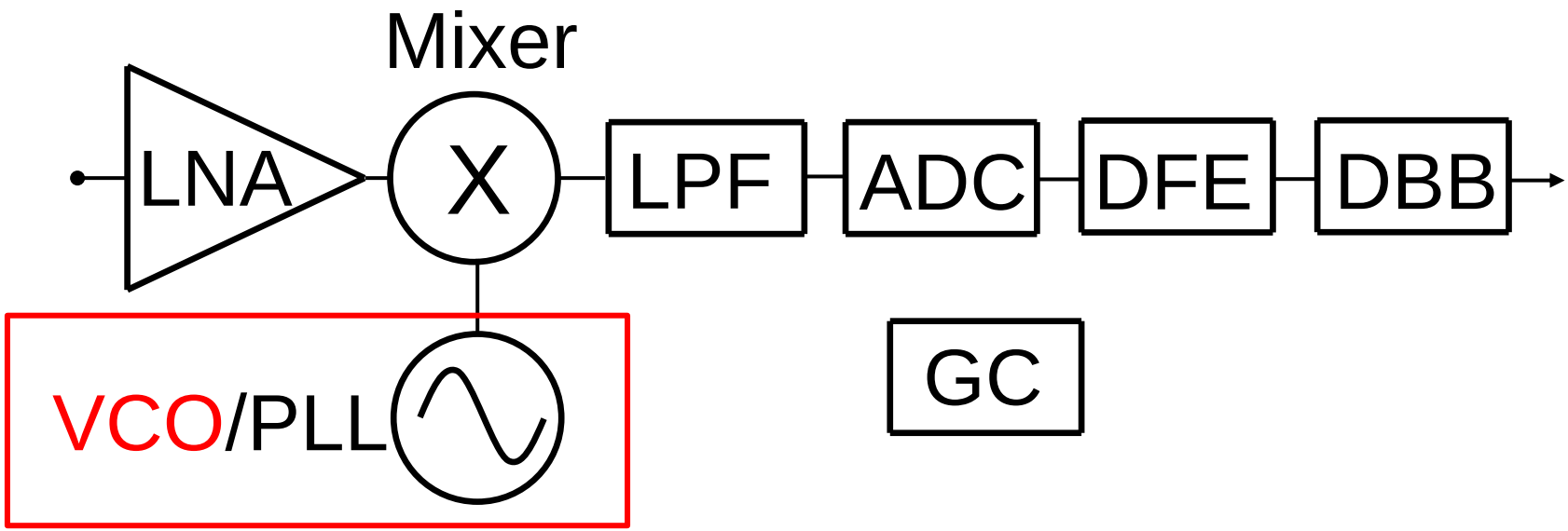


Phase noise simulations



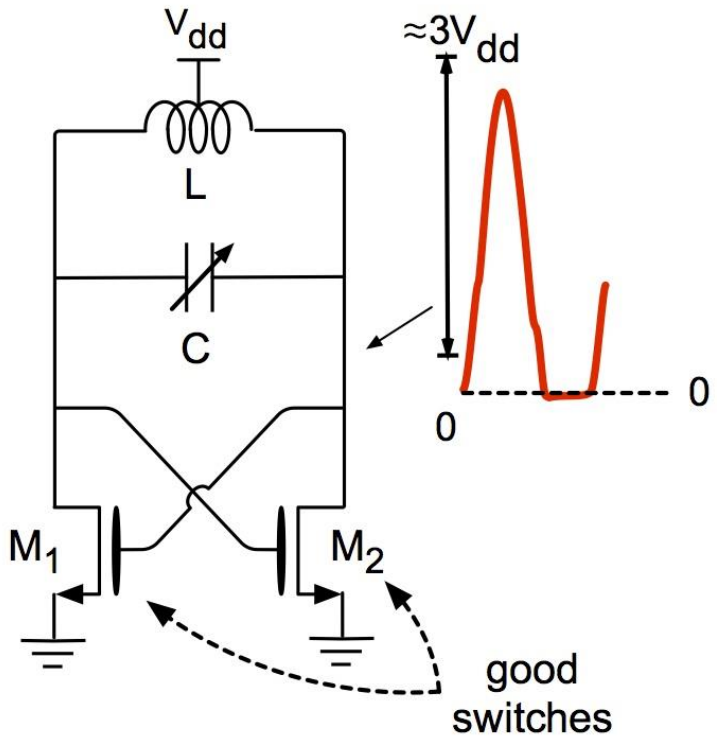
- BW=1.1MHz
- Noise cancellation strongly reduces quantization noise
- Waiting for IC to return from fab

VCOs



Luca Fanori &
Thomas Mattsson
(Ericsson)

Prior art: class-D oscillator

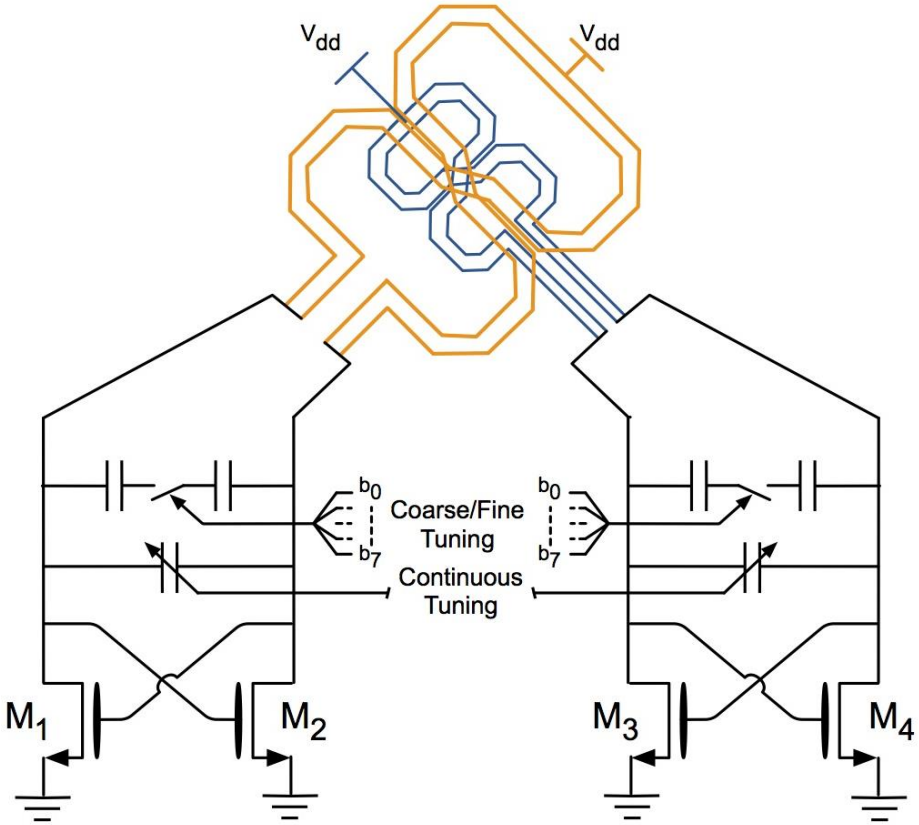


ISSCC 2013, JSSC Dec. 2013

- Amplitude A ≈ $3V_{dd}$, efficiency > 90%
- Excellent switches available in nm CMOS
- Suitable for very low V_{dd}

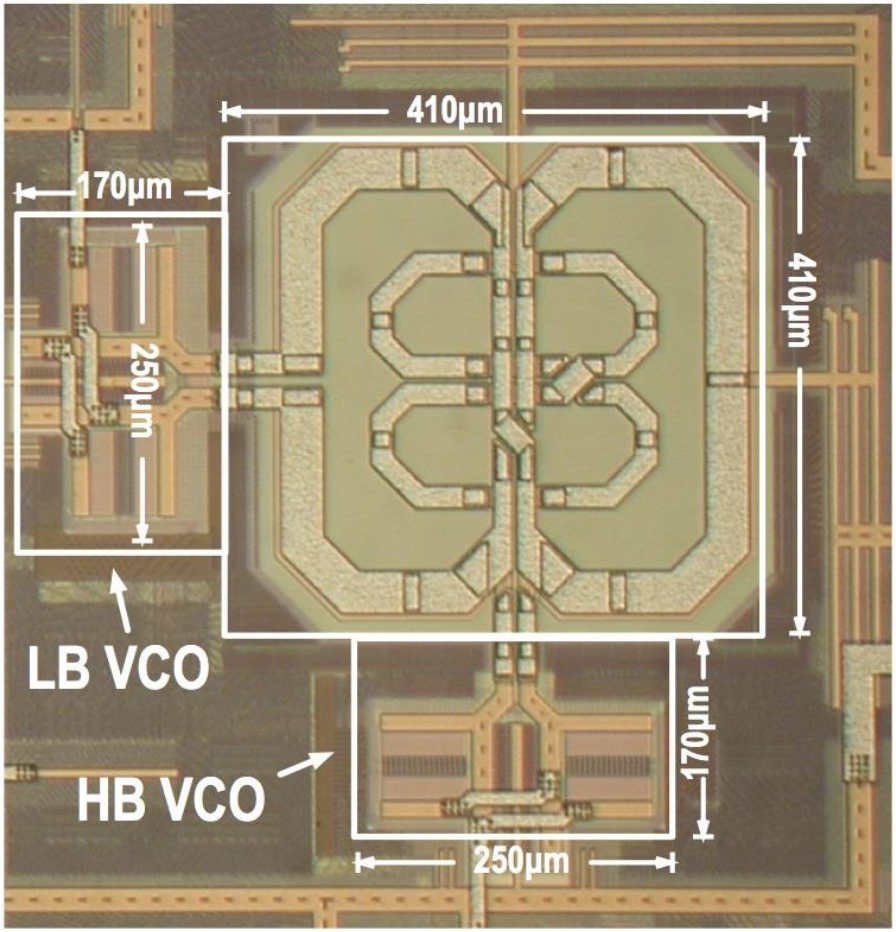
1st VCO: dual-core VCO with TR > 1 octave

ISSCC 2014



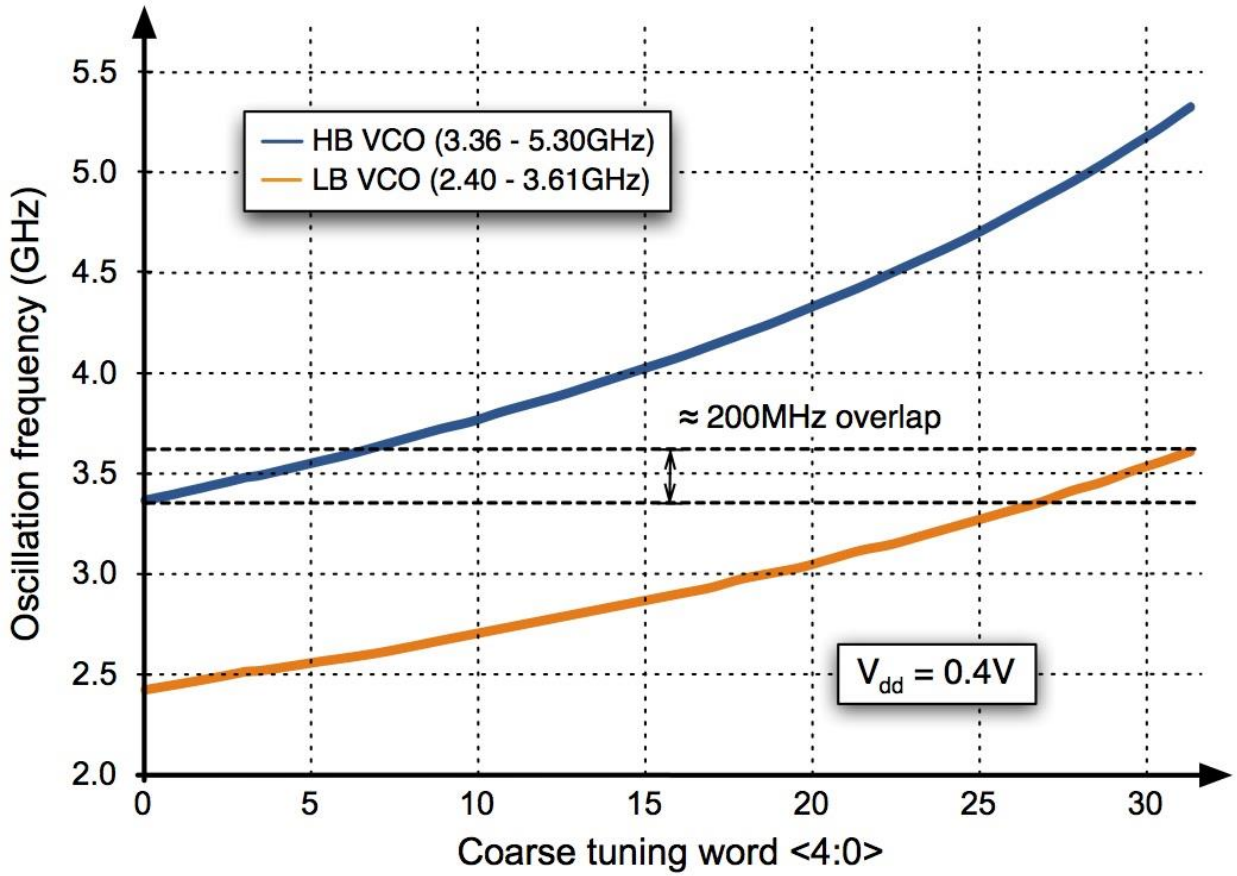
- Orthogonal 8-shaped inductor → no magnetic field between coils
- Very wide tuning range with small inductor area
- Class-D → low voltage supply, high performance

Chip photograph

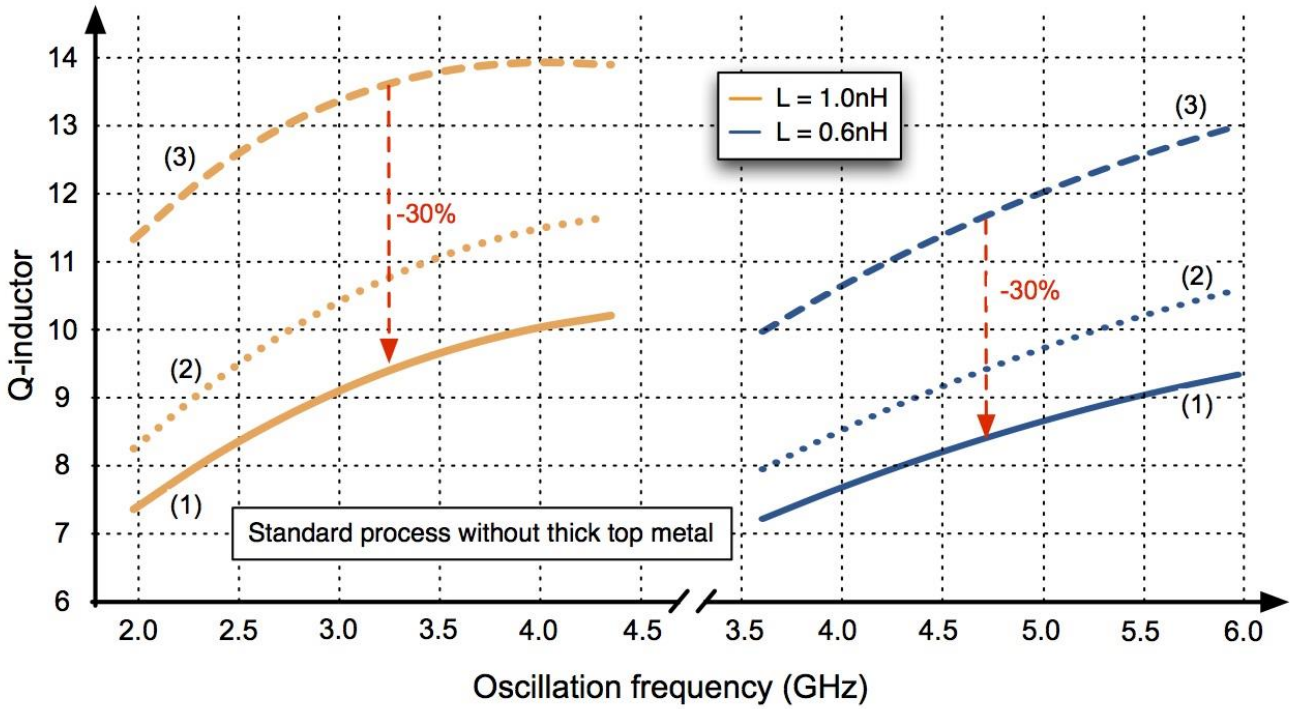


- 65nm CMOS process without thick metal
- Inductors: 1nH and 0.6nH
- Overall tuning range: 2.4-5.3GHz (75%)
- 0.33mm^2 active area
- Voltage supply: 0.4-0.5V

Tuning range



Q vs. frequency

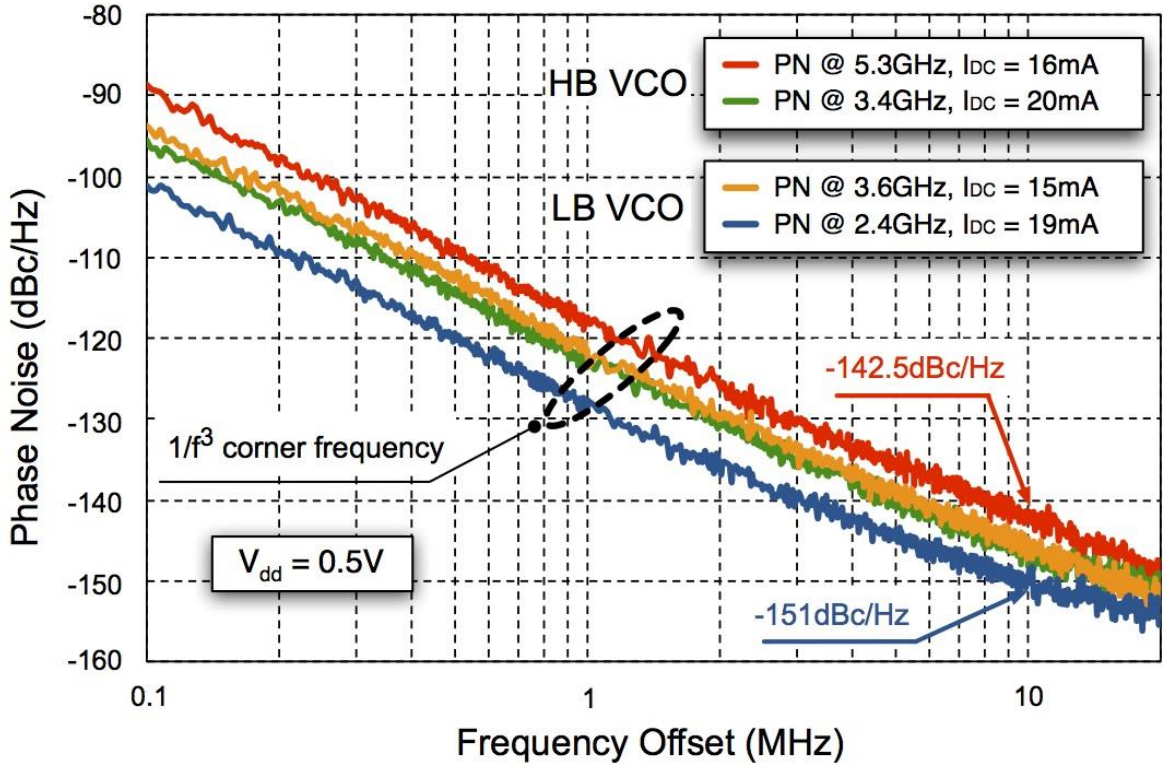


(1) Actual design

(2) Other inductor removed (difference < 10%)

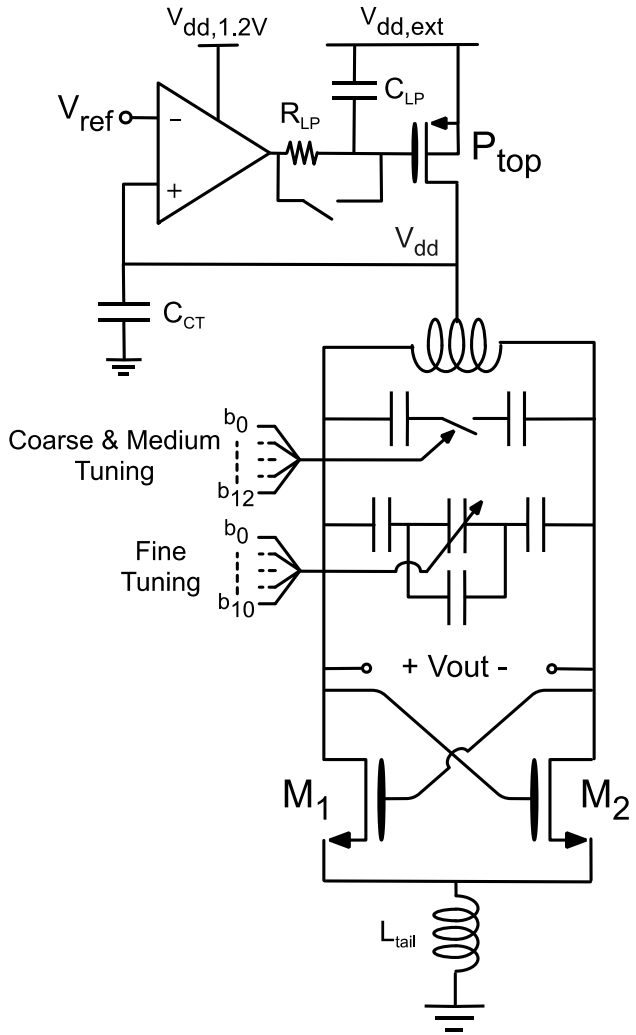
(3) Inductor optimized for standalone VCO

Phase noise at V_{dd} =0.5V



- FoM ≈ 188/189dBc/Hz across the tuning range
- $1/f^3$ noise corner frequency between 0.7MHz and 1.5MHz

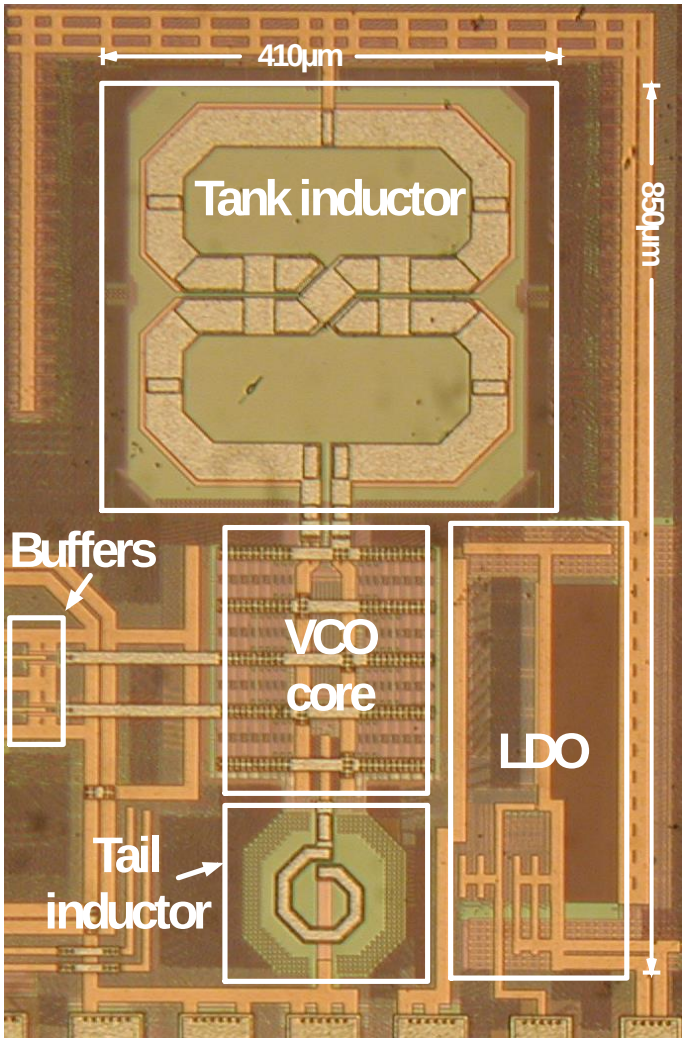
2nd VCO: class-D VCO with on-chip LDO



ESSCIRC 2014

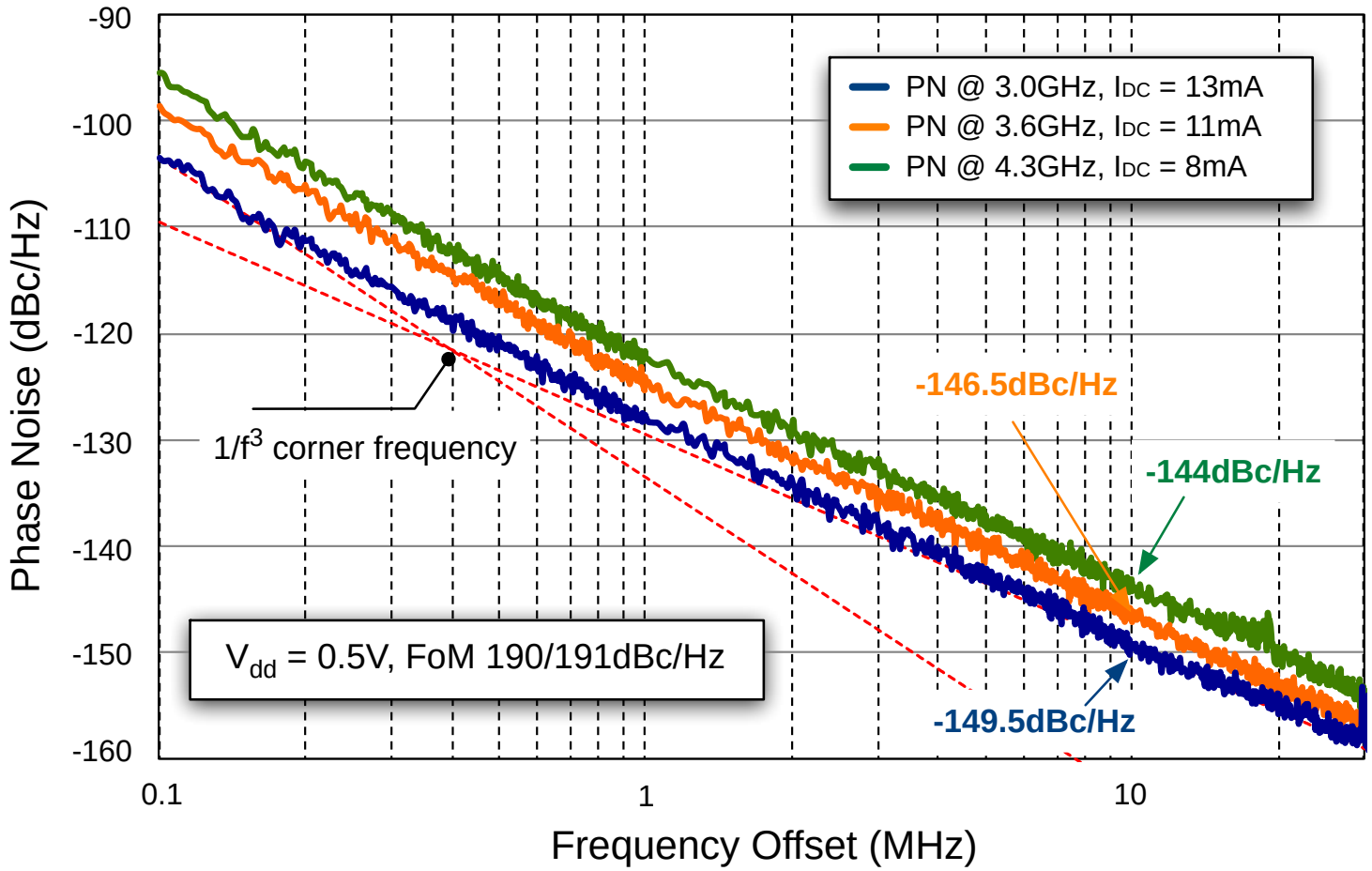
- P_{top} gate follows P_{top} source above f_{LP} → spurs and noise from $V_{dd,ext}$ are rejected
- Narrow-band op-amp → negligible op-amp impact on phase noise

Chip photograph



- 65nm CMOS with thick top metal
- 0.9nH inductor
- Q_{ind} = 14, Q_{tank} = 11 @ 4GHz
- Tuning range: 3.0 – 4.3GHz
- Area: 850µm × 410µm
- V_{dd} = 0.4-0.5V
- $V_{dd,ext} = V_{dd} + 200mV$

Phase noise at V_{dd} = 0.5V



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LUND UNIVERSITY