Internet of Everything (IoE)

Need end-to-end energy efficiency
Moore’s Law scaling

Continued benefits from Moore’s Law

More, better transistors
More cores

14nm Trigate
2014
Dynamic platform control

Deliver best user experience under constraints
Near Threshold Voltage (NTV) computing
NTV IA processor

Technology: 32nm High-K Metal Gate
Interconnect: 1 Poly, 9 Metal (Cu)
Transistors: 6 Million (Core)
Core Area: 2mm²
IA-32 Core
Logic
Scan
ROM
L1$-I L1$-D
Level Shifters + clk spine
1.1 mm
1.8 mm

I/O Area
5 mm
5 mm

JTAG
PLL
I/O Area
IA-32 Core
I/O Area
NTV design techniques

Narrow muxes  No stack height > 2

Robust level converters

Modified Register File Cell (L1$)

Robust Flop Topologies

Multi-corner design optimizations (SCL)

Variation-aware design 2X min Z, 40% lib cells used
NTV IA – powered by solar cell!
Power performance measurements

32nm CMOS, 25°C

Total Power (mW)
Frequency (MHz)

Logic Vcc / Memory Vcc (V)

3MHz 2mW
100MHz 17mW
500MHz 174mW
915MHz 737mW
Power components

- **Logic Dynamic Power**: 81%
- **Logic Leakage Power**: 11%
- **Memory Dynamic Power**: 53%
- **Memory Leakage Power**: 15%

Vcc-max (Super-Threshold)
- Logic Vcc: 1.2V
- Memory Vcc: 1.2V

Vcc-opt (Near-Threshold)
- Logic Vcc: 0.45V
- Memory Vcc: 0.55V

Vcc-min (Sub-Threshold)
- Logic Vcc: 0.28V
- Memory Vcc: 0.55V
Minimum energy operation

32nm CMOS, 25°C

4.7X

Energy/Cycle (nJ)

Logic Vcc / Memory Vcc (V)
NTV and variability

32nm CMOS, 25°C

Leakage Comparison

- Slow: 1.0X
- Medium: 2.5X
- Fast: 7.5X

Energy/Cycle (pJ)

- Slow: 16%
- Medium: 22%
- Fast: 30%

Frequency (MHz)

- Slow: 18%
- Medium: 22%
- Fast: 28%

32nm CMOS, 25°C
Voltage-frequency margins

![Voltage-frequency margins diagram](image)
Dynamic adaptation & reconfiguration

Adapt & reconfigure for best power-performance

Dynamic Control Unit
- Voltage Control
- Frequency Control
- Configuration Control

Processor

Sensors
- Thermal Sensor
- Voltage Sensor
- Current Sensor
- Aging Sensor

Change V
Change F
Reconfigure
Dynamic V & F adaptation

Environment-aware dynamic adaptation

- Adapt F/V to V/T change → reduce V/T margin
- Adapt F/V to aging → reduce aging margin

Prototype chip in 90nm

Source: Intel
Resilient platforms

Resiliency for performance, efficiency & reliability

Resiliency framework

- Applications
- Programming System
- OS
- VM
- Firmware
- Microcode
- Microarchitecture
- Circuit & Design

Resilient platform features

- Error detection
- Fault diagnosis
- Fault confinement
- Error correction
- System recovery
- System adaptation
- System reconfiguration

Less error rate
Less recovery overhead
Less silicon overhead
Resilient & adaptive core

- Technology: 45nm CMOS
- Die Area: 13.64 mm²
- Core Area: 0.39 mm²
- Core $F_{\text{MAX}}$: 1.45GHz at 1.0V
- Core Power: 135mW at 1.0V

Diagram:

- CLOCK GENERATOR
  - PLL
  - Duty Cycle
  - Error Control Unit
  - Adaptive Clock Control

- CORE
  - 16KB I$\$
  - 16KB D$\$
  - PC
  - DE
  - RA
  - EX
  - MEM
  - X
  - WB
  - RF

- refclk

- JTAG

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Performance & efficiency gains

Input Image

Output Image: Resiliency ON

Output Image: Resiliency OFF

Conventional
EDS
TRC

Throughput (BIPS)
Total Energy (mJ)

10% V_{cc} Droop

Throughput Gain (%)
edgedetect linkedlist bubble

Application

22% 41% 10% V_{cc} Droop
Integrated voltage regulators

**Conversion**
- Area efficient
- Scalable
- Persistent rail

**Distribution**
- Lower loss
- Higher fidelity
- Simpler

**Control**
- Fast & efficient
- Load adaptive
- Independent rails

![Efficiency Graph](chart.png)
Fully integrated VR
Energy efficient interconnects

Energy Eff. (pJ/bit)

Channel Loss @ Symbol rate (dB)

Green = Intel (research)

Optical I/O

Driver

Laser

Modulator

PIN Diode

Receiver

Fiber

TIA
Memory capacity & bandwidth
Neuromorphic computing
End-to-end efficiency for IoE

- Extreme Energy Efficiency
- Fine-Grain Power Management
- Efficient Memory Subsystem
- Self-Aware Computing Operation
- Programming for Extreme Parallelism

System-Wide Breakthroughs Needed Across the Board