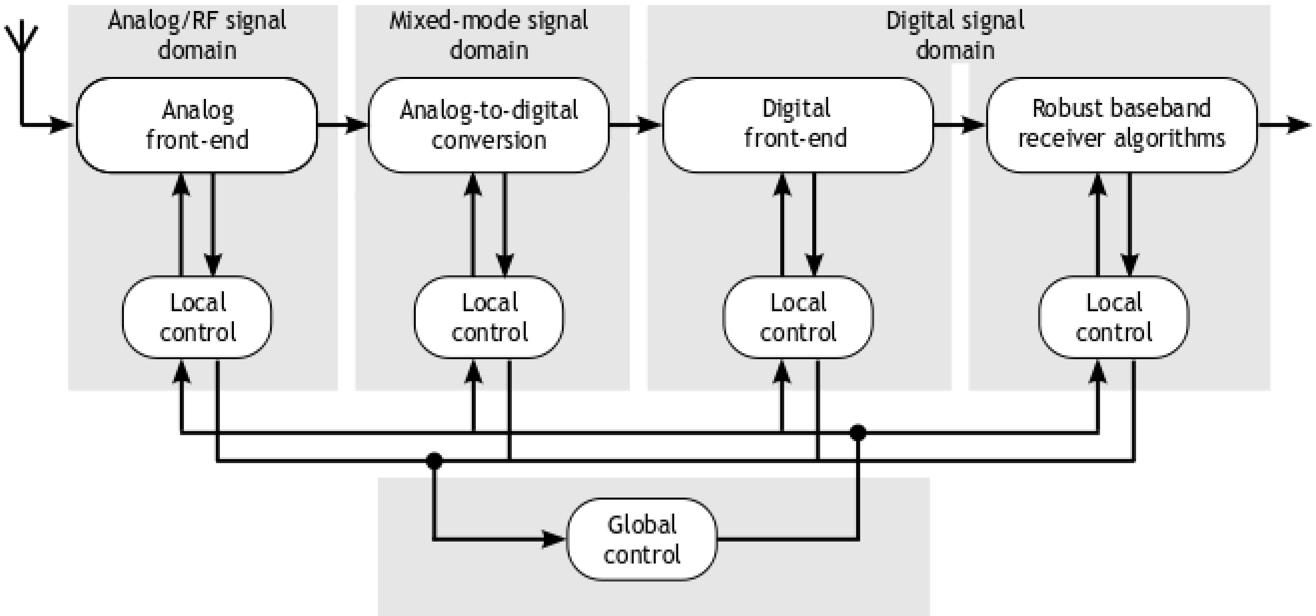
Digitally Assisted Radio Evolution – DARE

Pietro Andreani

Department of Electrical and Information Technology
Lund University, Sweden

The DARE Concept



Focus on 4G radio receiver and frequency generation

Notable Results

- LNAs and front-ends
- Channel-select filters
- A/D converters
- VCOs, TDCs, PLLs
- Digital base-band
  - Channel estimation
  - MIMO decoder
  - Linearity enhancement

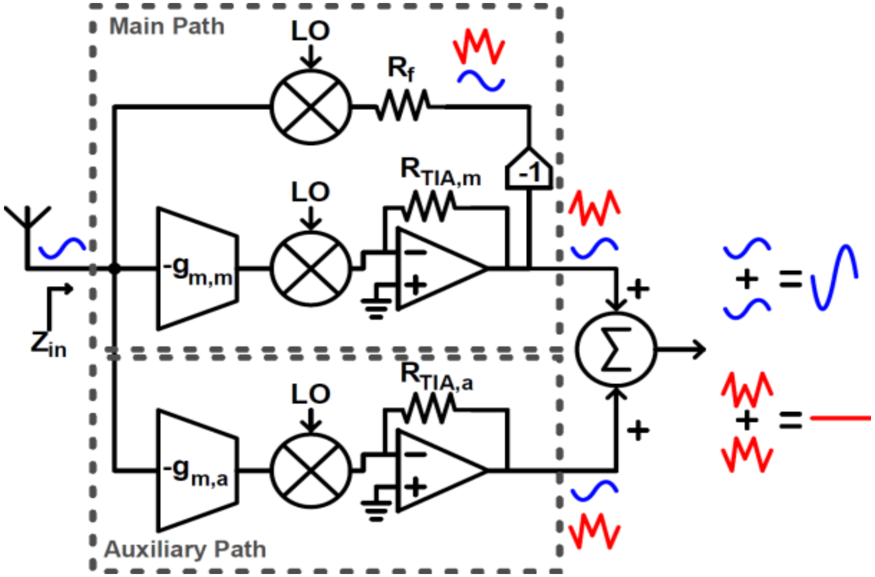
Swedish Foundation for Strategic Research

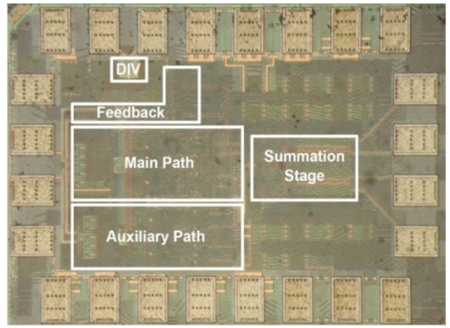
Research Team, 2010 – 2016

Anders Nejdel

LTE Receiver Front-End – I

A Noise Cancelling 0.7-3.8 GHz Resistive-Feedback Receiver Front-End in 65 nm CMOS





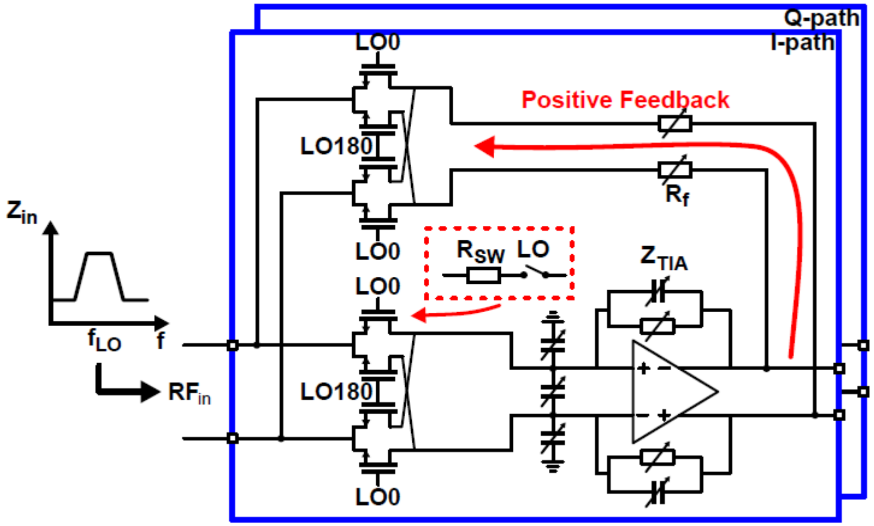
- Feedback phase can be tuned for complex Z_S
- Programmable g_m

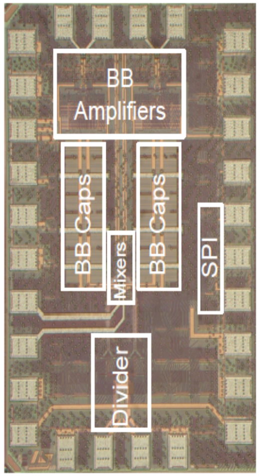
RFIC 2014
JSSC 2015

LTE Receiver Front-End – II

Anders Nejdel

Mixer-first receiver front-end with positive feedback





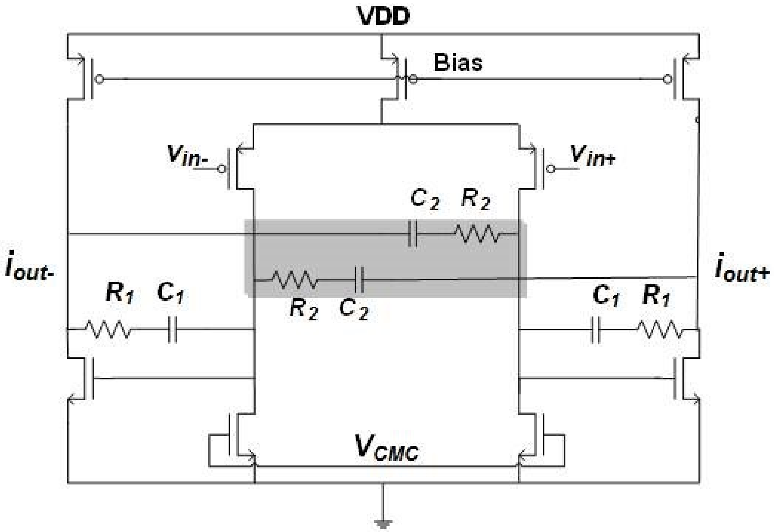
- Increase input impedance at f_{LO}
- R_f used to control loop gain to match input

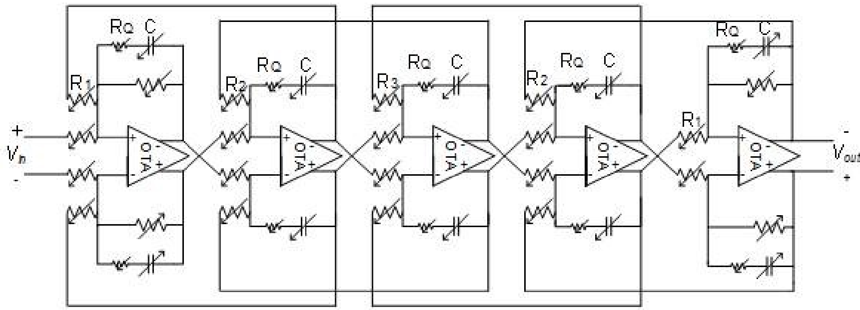
RFIC 2015

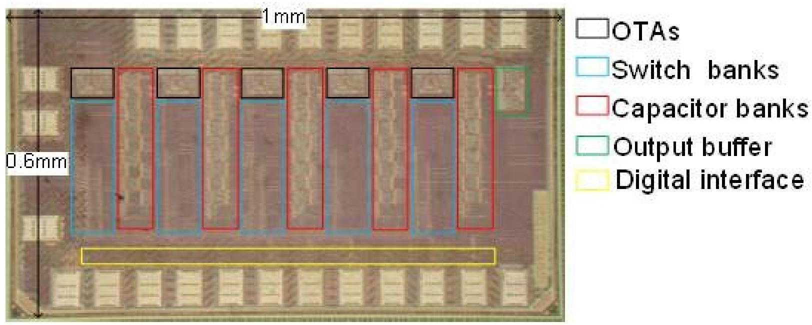
Mohammed Abdulaziz

Frequency Compensation Technique for OTAs

- 5^{th} order active-RC Chebyshev filter → requires very fast OTAs





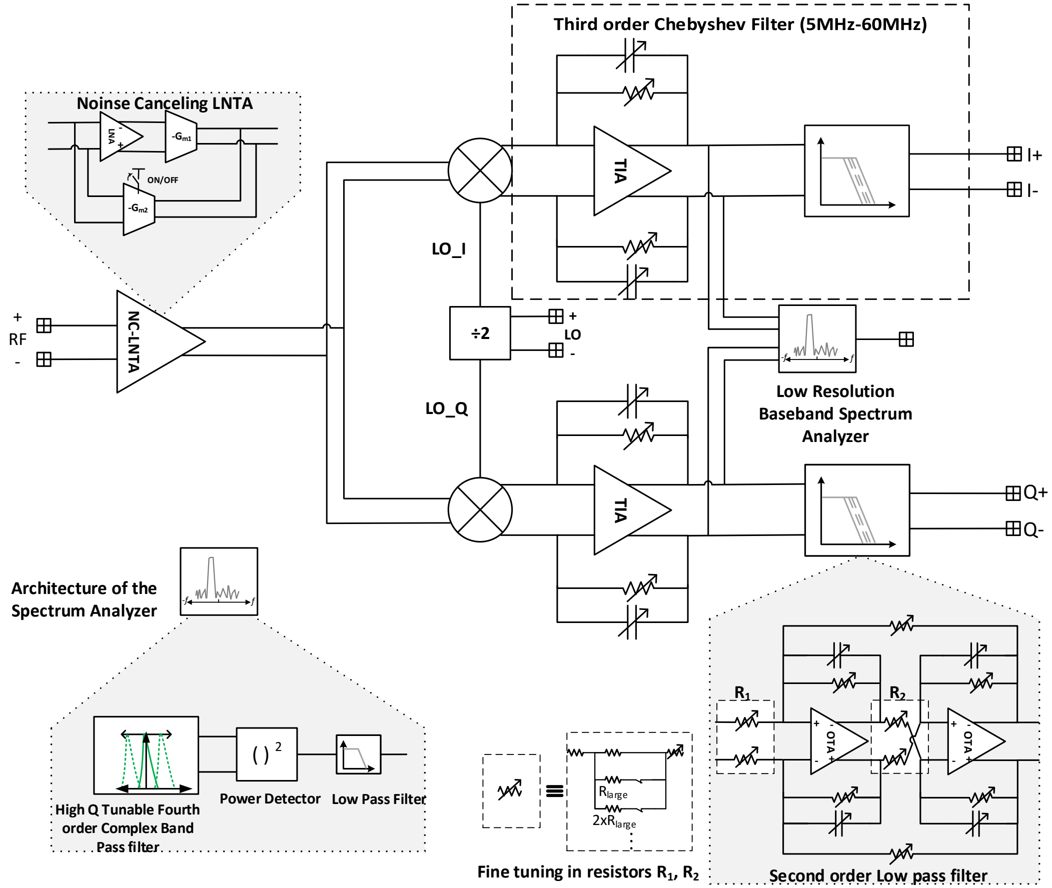


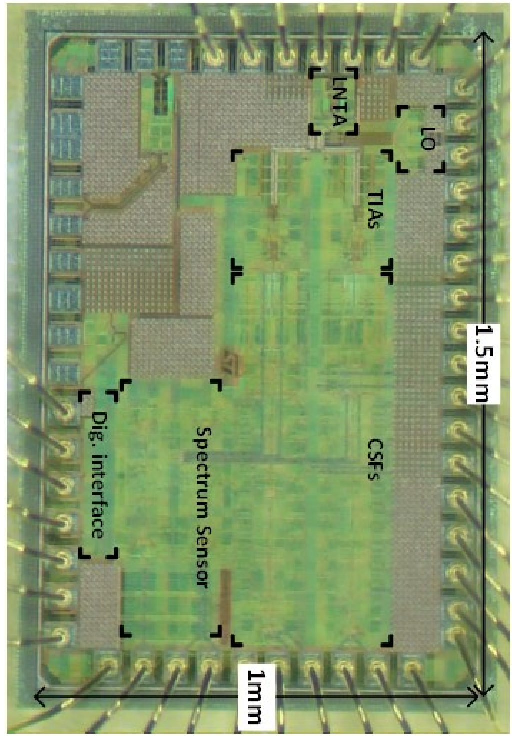
RFIC 2013
TCAS-II 2014

RX Front-End with Blocker Sensing

Swedish Foundation for Strategic Research

Mohammed Abdulaziz





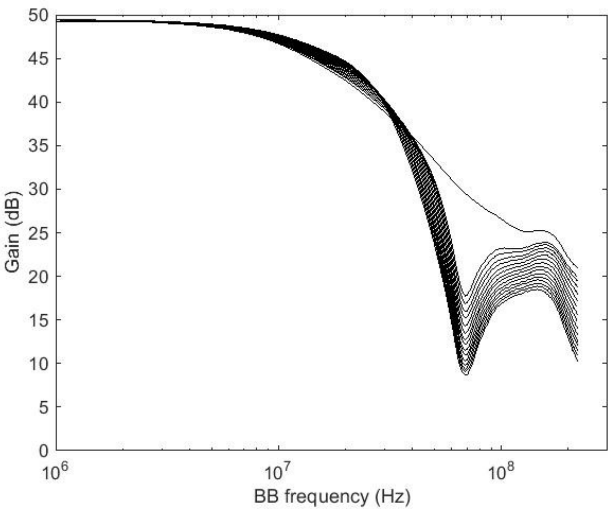
RFIC 2016

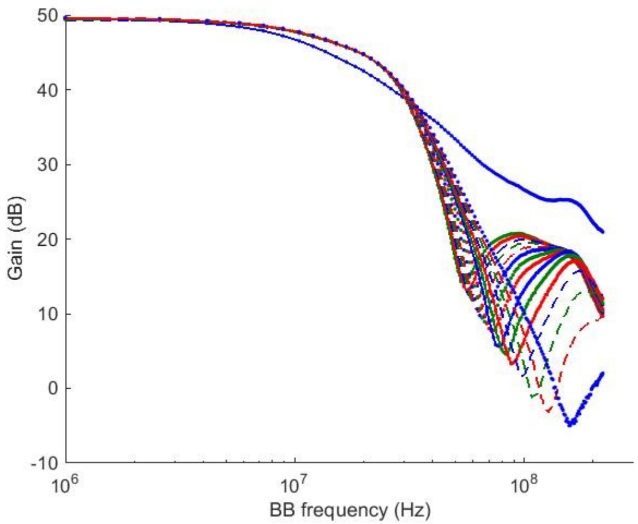
Mohammed Abdulaziz

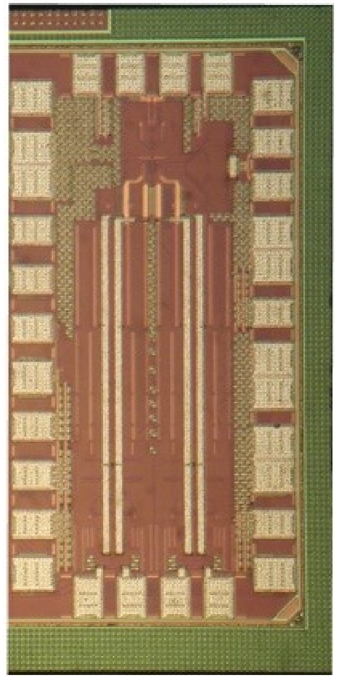
Swedish Foundation for Strategic Research

A Blocker-Tolerant Front-End

Improved gain compression and NF vs. blocker



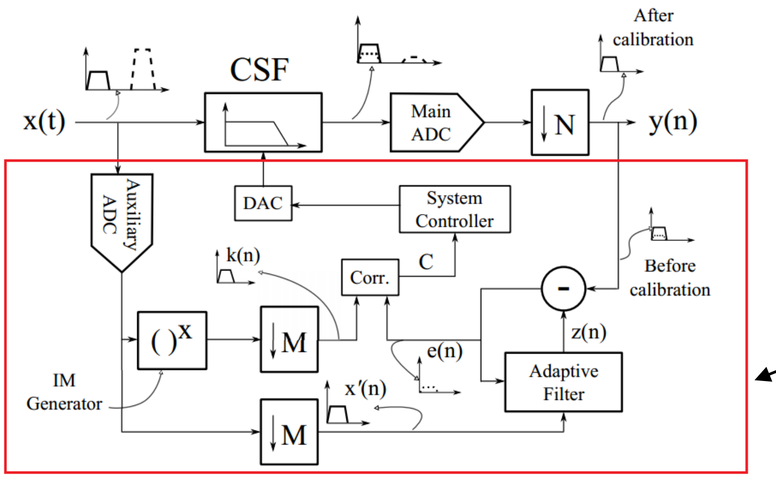




unpublished

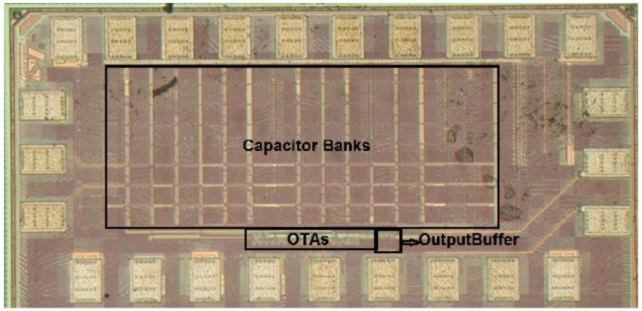
Digitally-Assisted Linearity Improvement in CSF

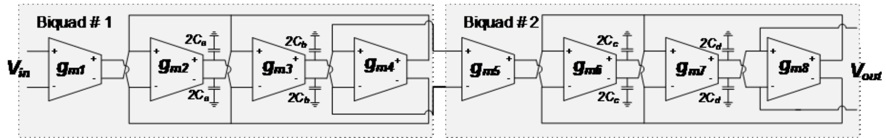
Rakesh Gangarajaiah
Mohammed Abdulaziz

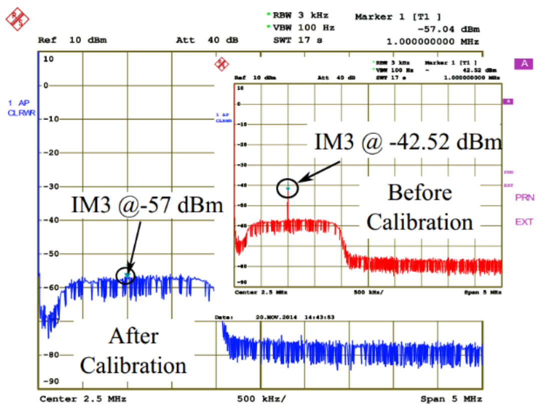


Proposed non-linearity suppression receiver with a tunable CSF

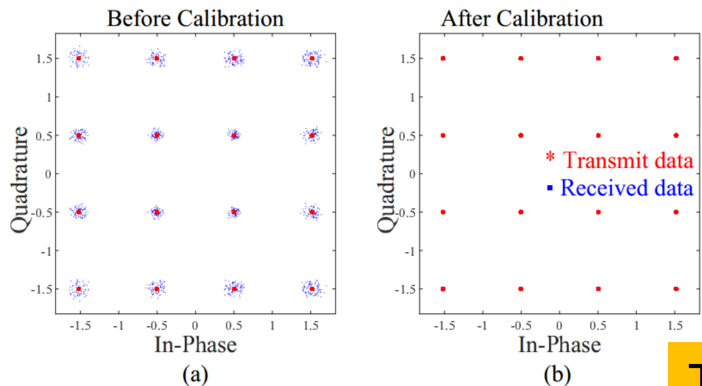
Xilinx FPGA







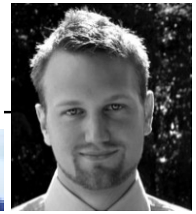
CSF output before and after calibration



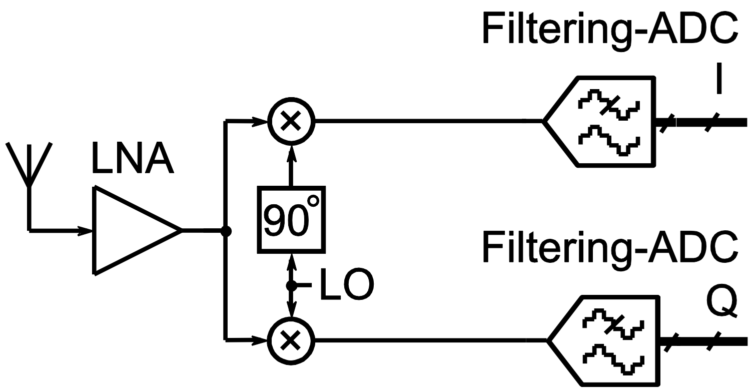
TCAS-II 2016

LTE Receiver Front-End – III

Xiaodong Liu
Anders Nejdel

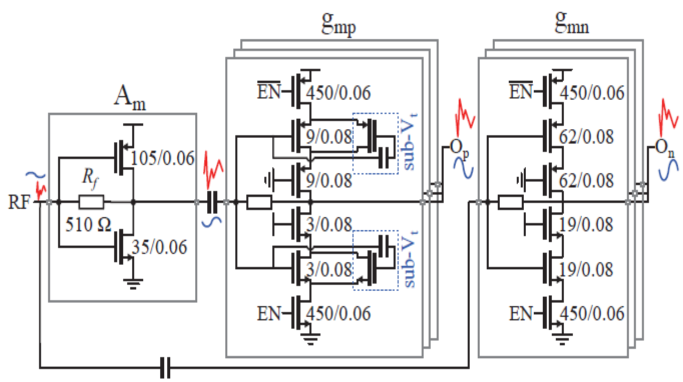



RX front-end with A/D-converting CSF

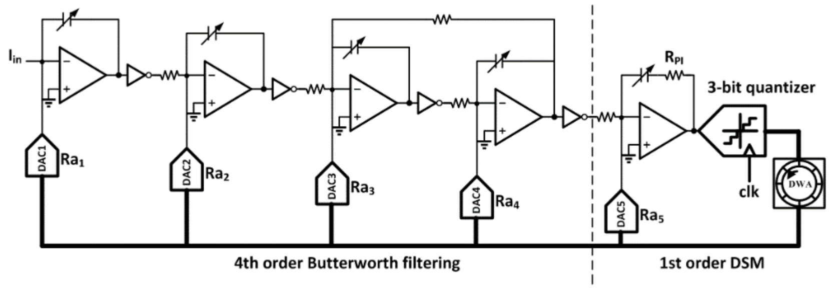


ESSCIRC 2015
JSSC 2016

Front-end

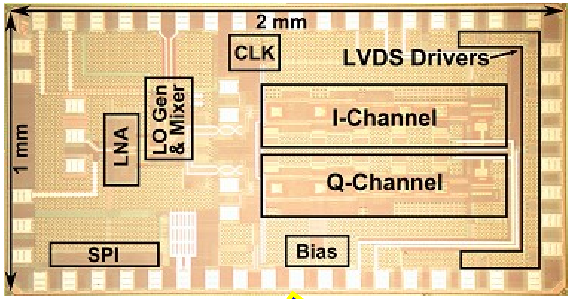


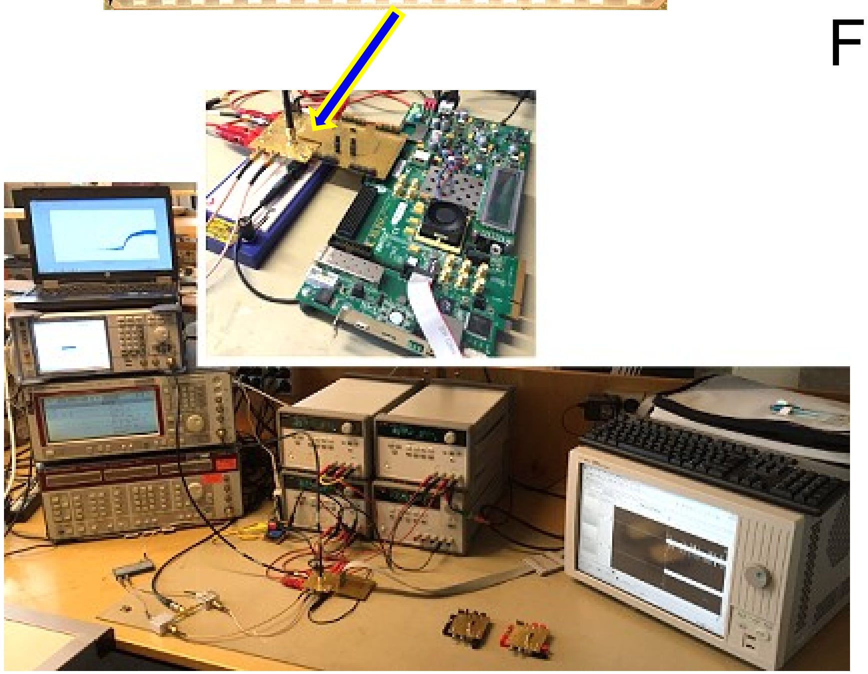
A/D-converting channel-select filter



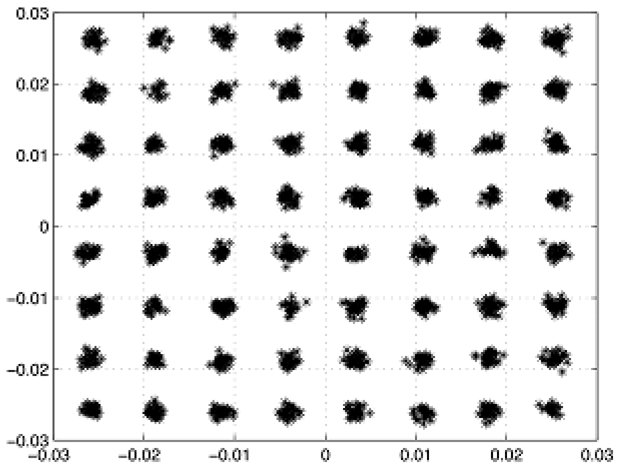
Demonstrator of Complete RX

Xiaodong Liu
Rakesh G.
Michal Stala
Anders Nejdel



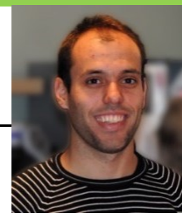


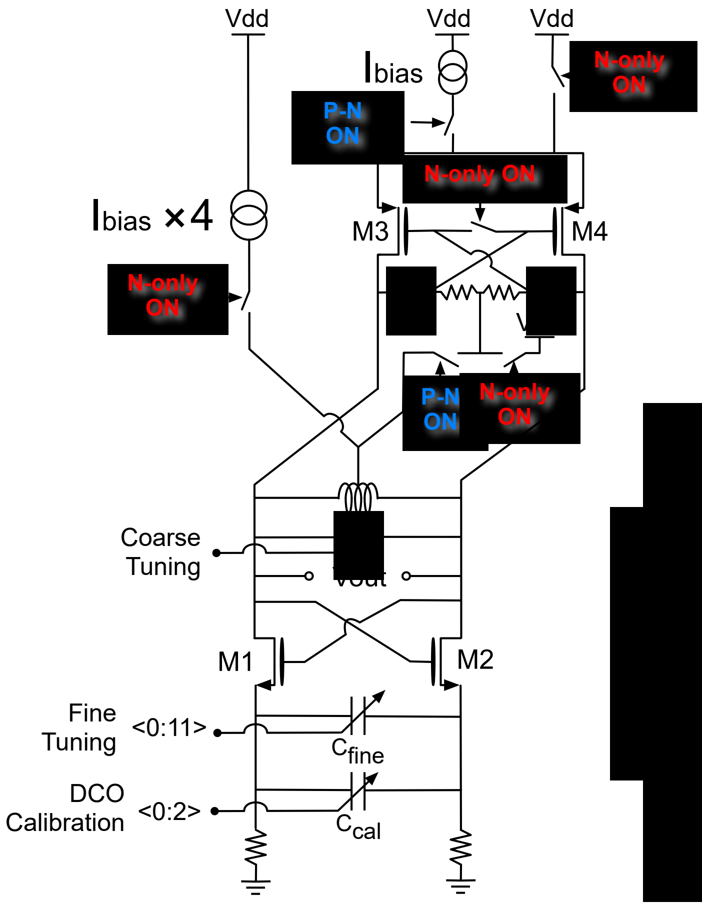
From antenna to constellation!

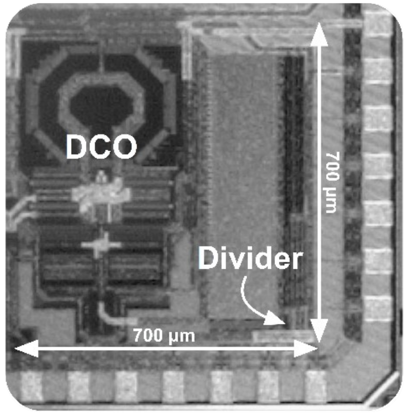


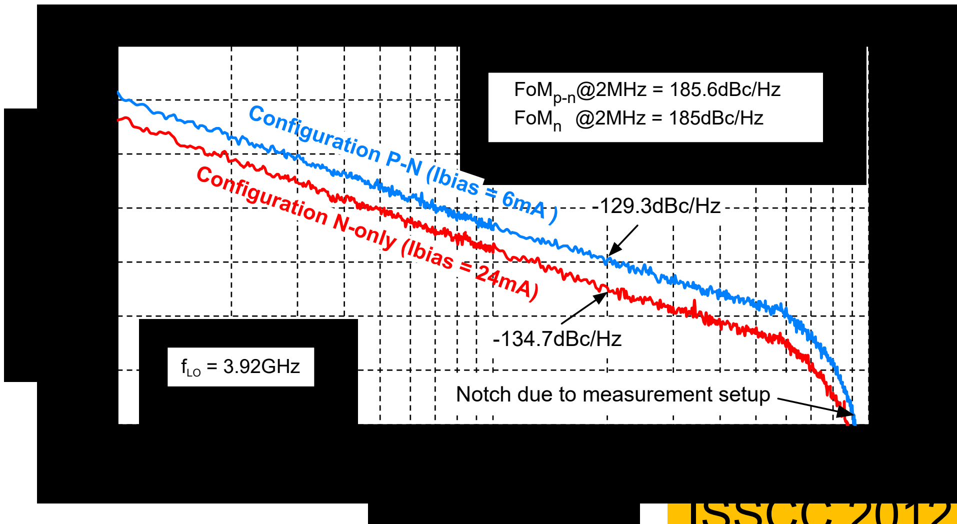
A Power-Reconfigurable DCO

Luca Fanori







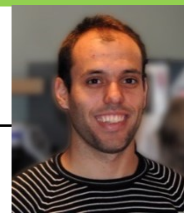


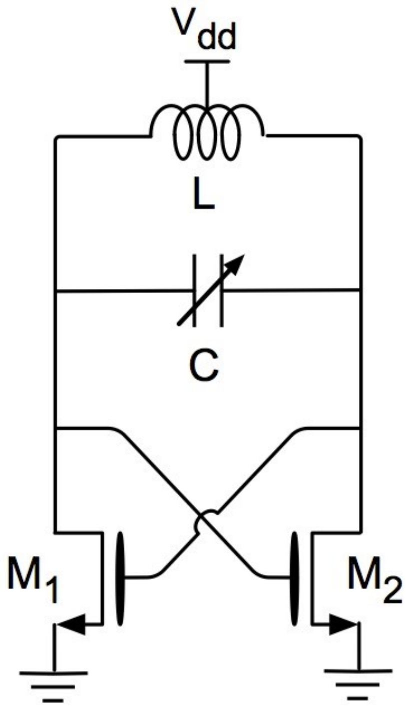
ISSCC 2012

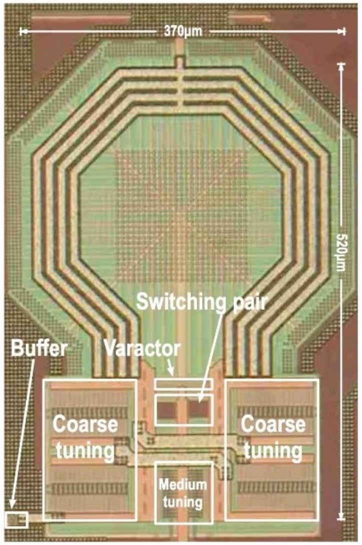
A 2.5-3.3GHz CMOS Class-D VCO

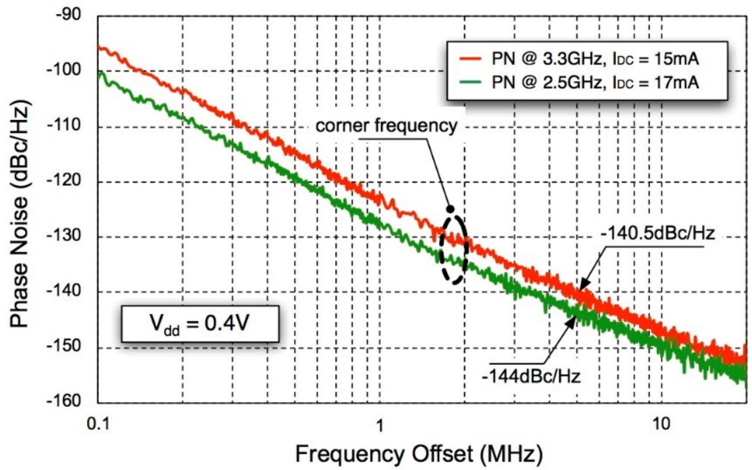
Swedish Foundation for Strategic Research

Luca Fanori







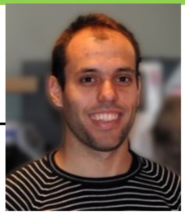


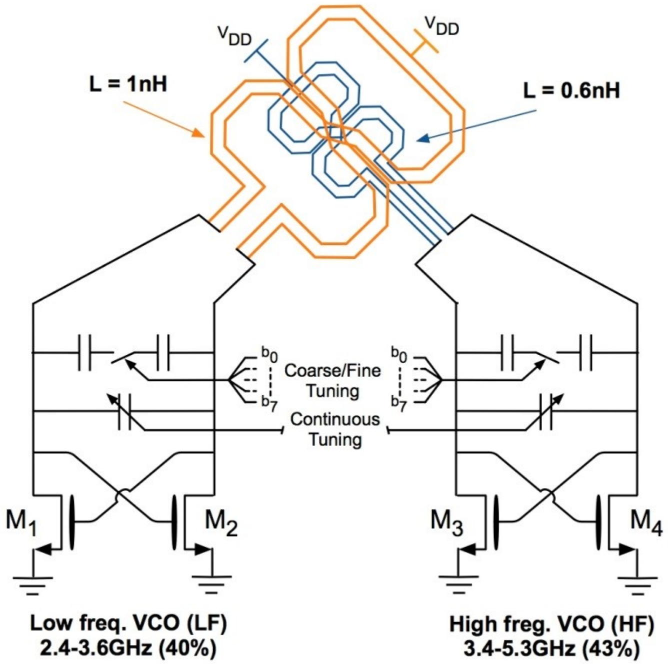
STM 65nm CMOS

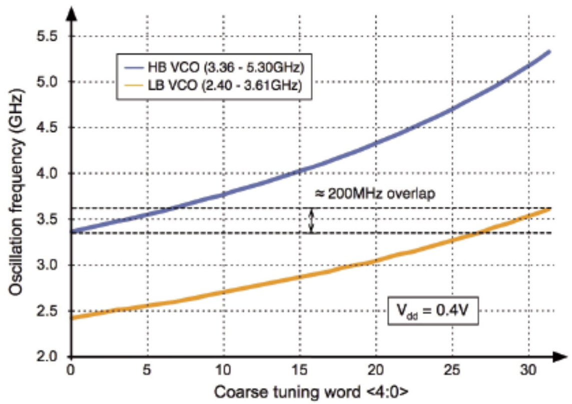
ISSCC 2013
JSSC 2014

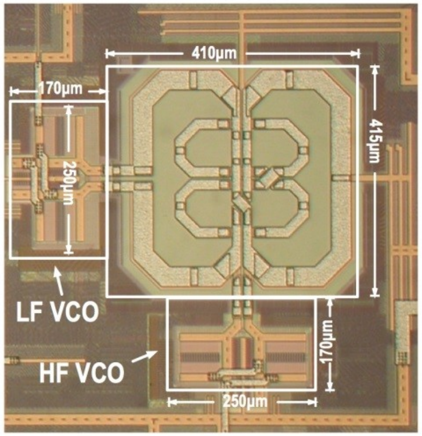
2.4-5.4 GHz double-core VCO

Luca Fanori









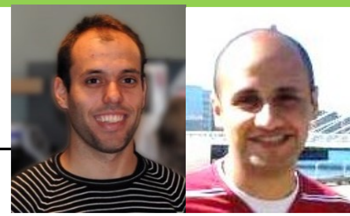
STM 65nm CMOS

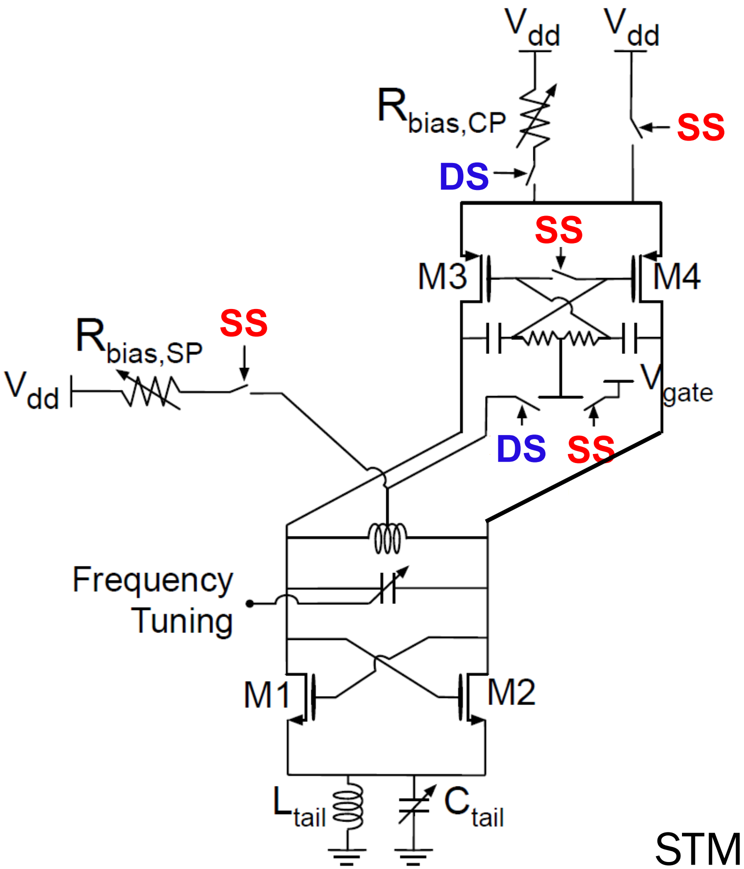
ISSCC 2014

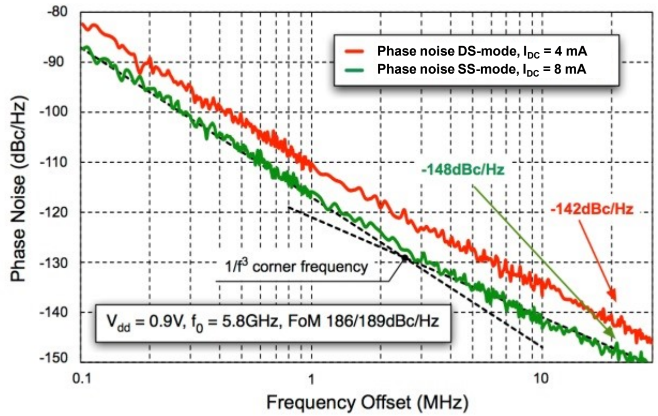
SWEDISH FOUNDATION for STRATEGIC RESEARCH

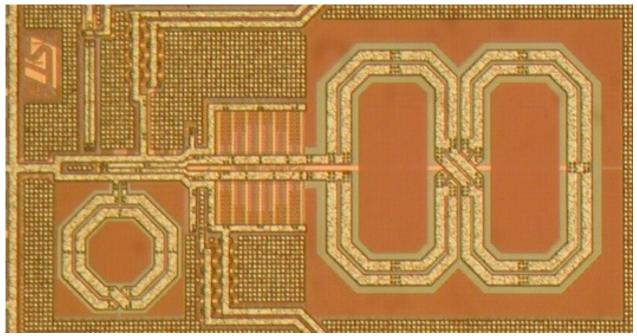
.8-5.8GHz reconfigurable VCO

Luca Fanori
Ahmed Mahmoud









STM 28nm UTBB FD-SOI CMOS

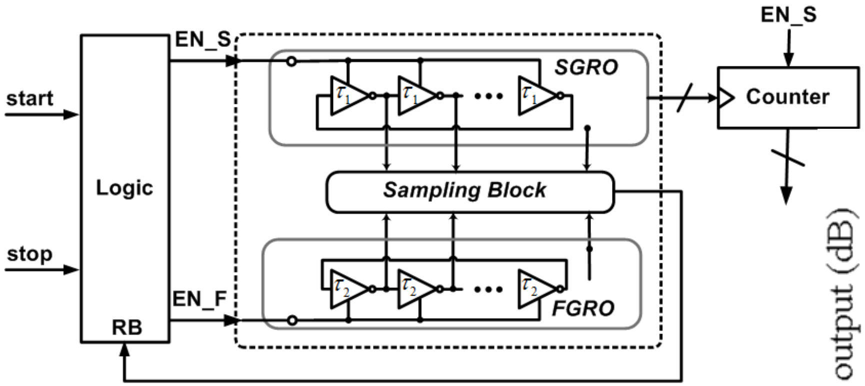
RFIC 2015
Springer 2016

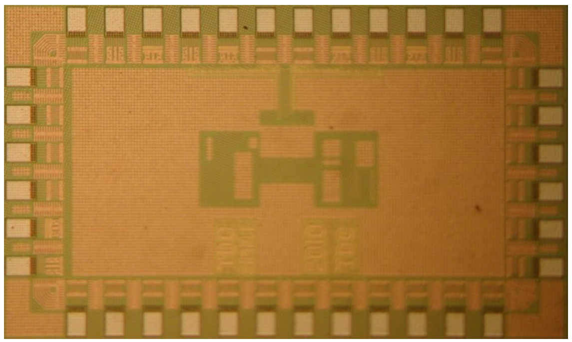
SWEDISH FOUNDATION for STRATEGIC RESEARCH

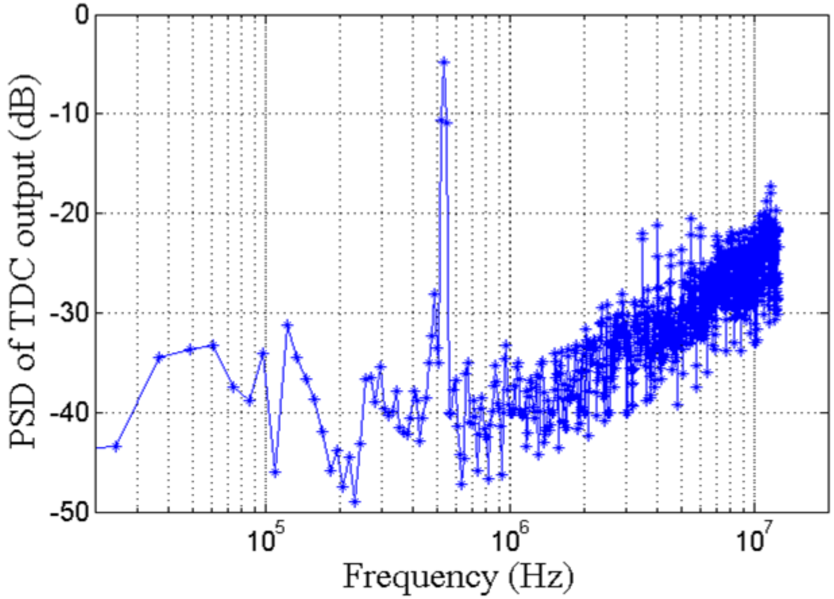
A 90nm CMOS Gated-Ring-Oscillator-Based Vernier TDC

Ping Lu

Combines Vernier TDC and gated-ring-oscillator TDC







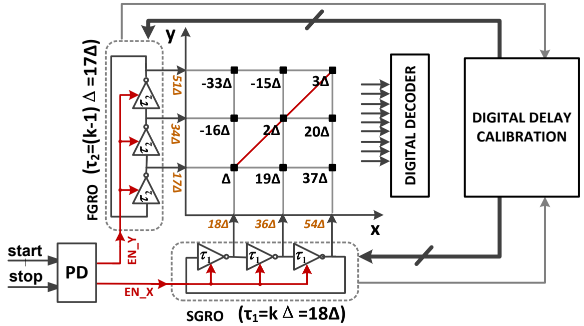
High Vernier time resolution + First-order noise shaping

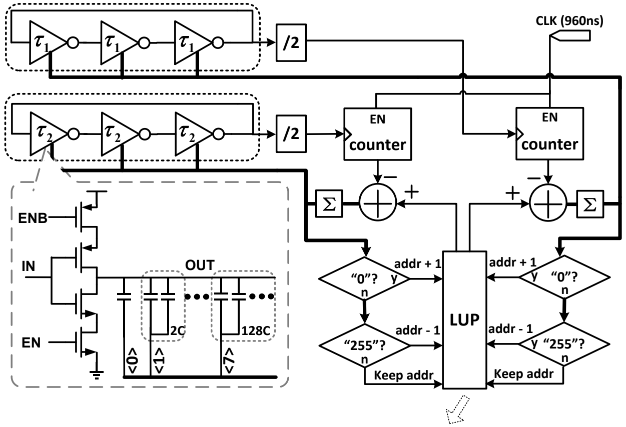
ESSCIRC 2011
JSSC 2012

A 2.2ps 2-D Gated-Vernier TDC

SWEDISH FOUNDATION *for* STRATEGIC RESEARCH

Ping Lu

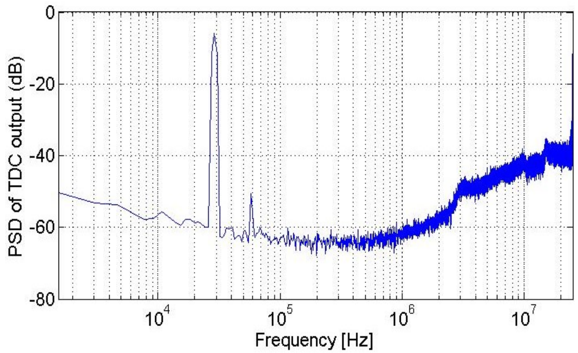




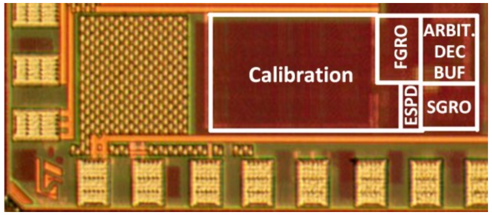
address	$Delay_{SGRO}$ (ps)	$Delay_{FGRO}$ (ps)	$\Delta = \tau_1 - \tau_2$ (ps)	k	No. of SGRO Cycles (C_S)	No. of FGRO Cycles (C_F)
0	250.000	235.294	14.706	5	17	16
...	...	...	...	...	...	...
8	185.185	175.439	9.747	19	912	864
9	178.571	166.667	11.905	15	960	896
10	170.940	158.730	12.210	14	1008	936
11	165.289	151.515	13.774	12	984	968
12	158.730	148.148	10.582	15	1080	1008
...	...	...	...	...	...	...
27	88.888	80.000	8.888	25	10	9

− / default addr / +

$C_S = 960ns/(Delay_{FGRO} \times 3 \times 2)$; $C_F = 960ns/(Delay_{SGRO} \times 3 \times 2)$



1st order shaping of delay quantization

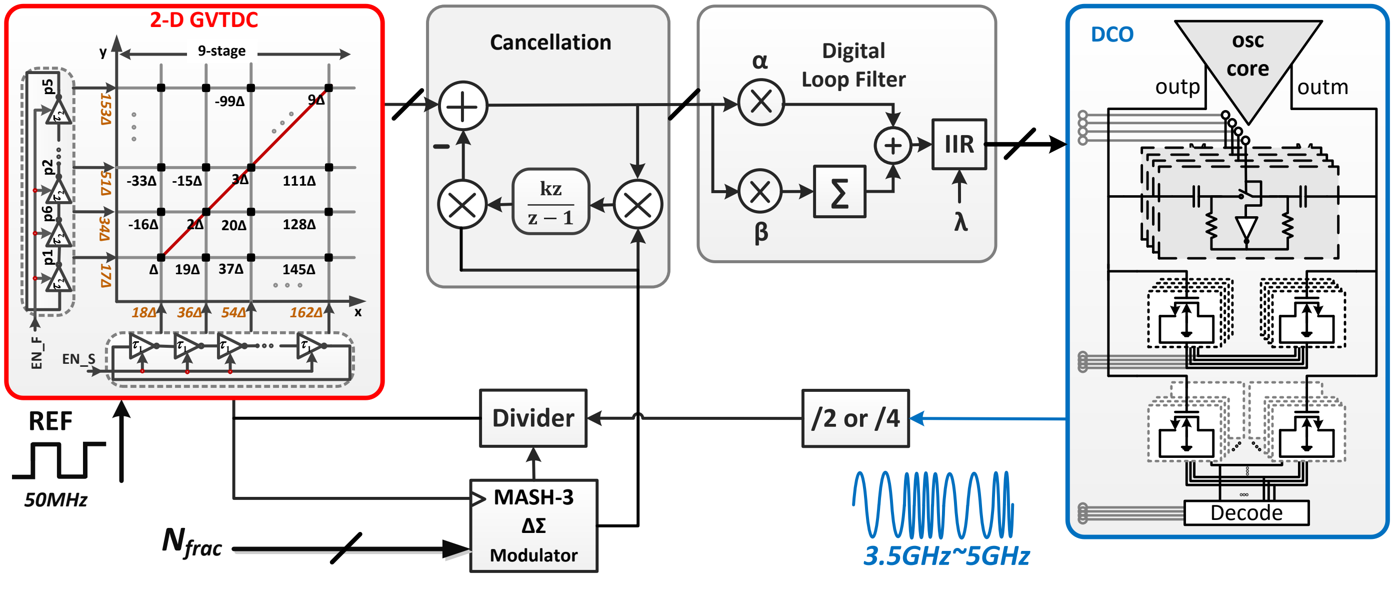


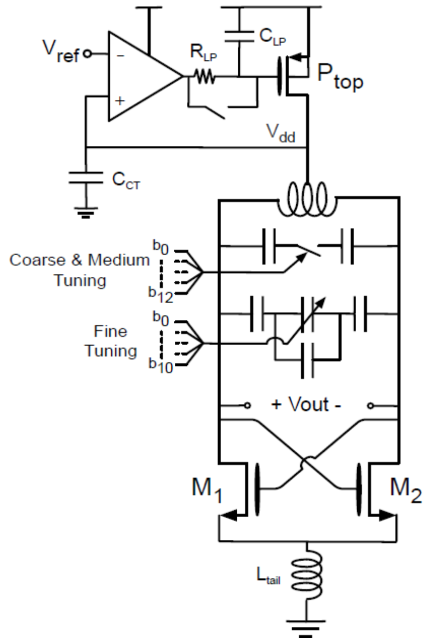
STM 65nm CMOS

RFIC 2013
TCAS-II 2016

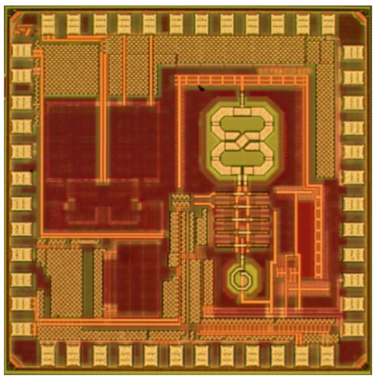
Digital PLL with 2-D TDC

Ping Lu
Ahmed Mahmoud





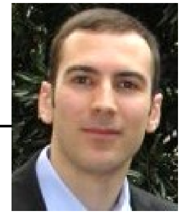
Class-D DCO



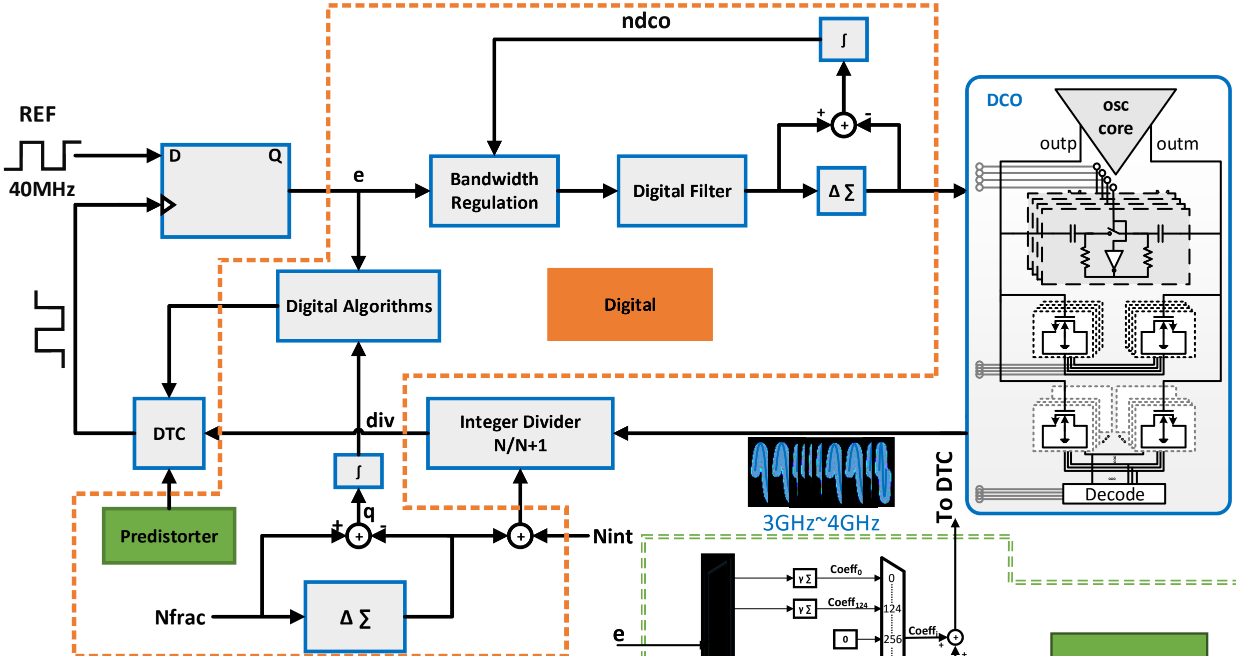
STM 65nm CMOS

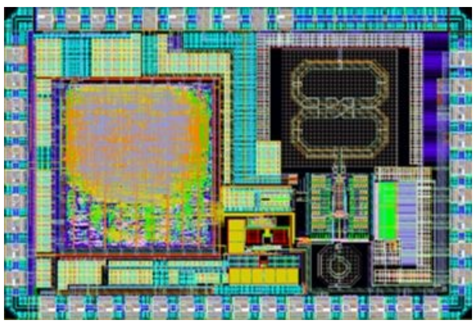
Springer 2016

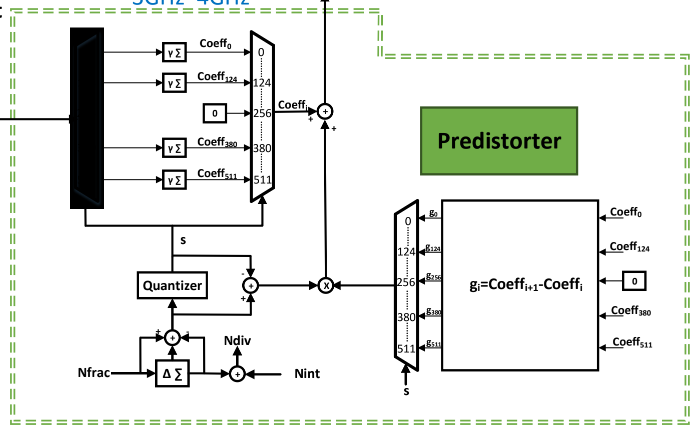
Ahmed Mahmoud
Federico Pepe

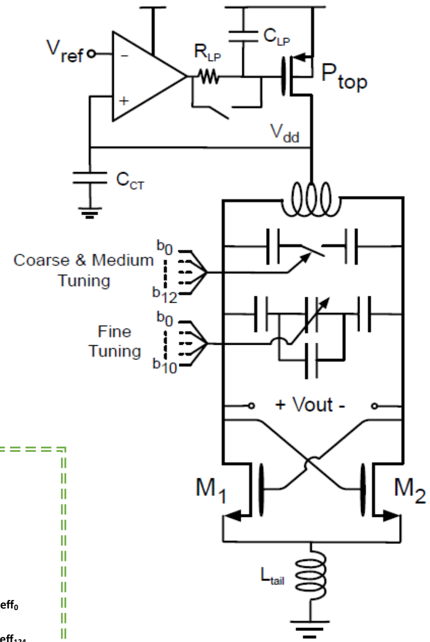


Digital PLL with DTC









Class-D DCO

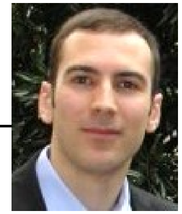
STM 65nm CMOS

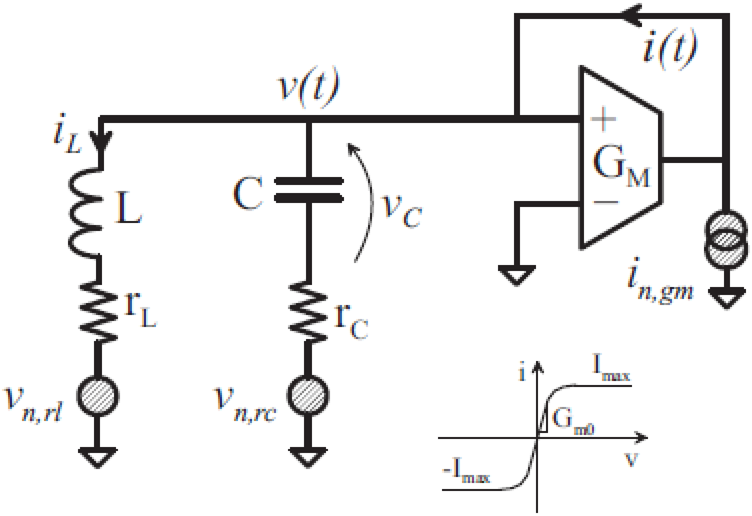
under fabrication

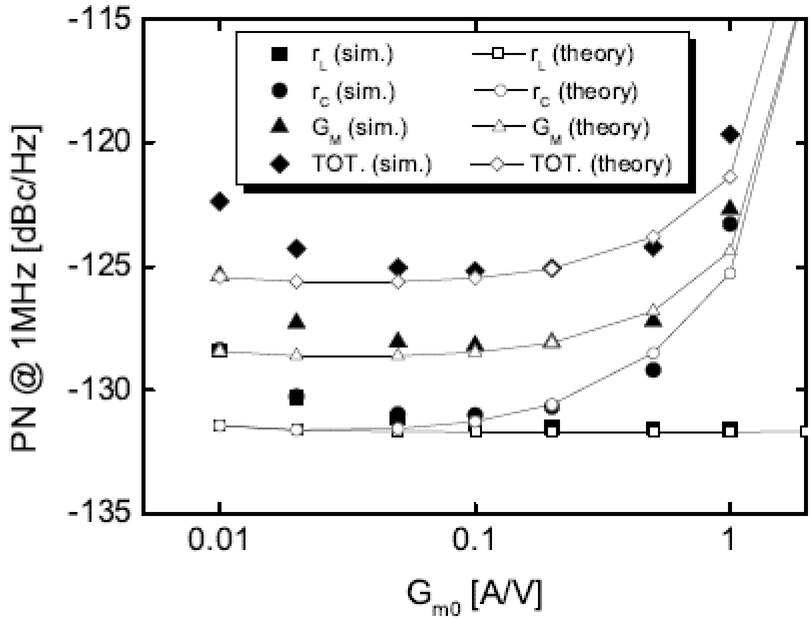
mproved phase noise analysis of harmonic oscillators

SWEDISH FOUNDATION for STRATEGIC RESEARCH

Federico Pepe







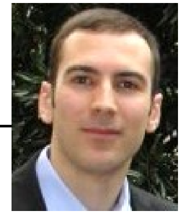
Asymmetry between inductive and capacitive losses

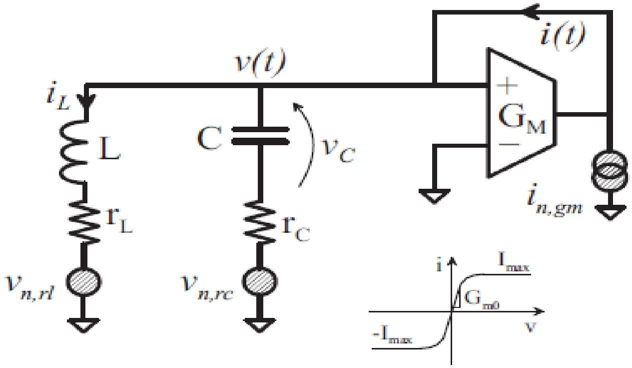
Phase noise caused by capacitive losses may be much higher

TCAS-II 2016

General phase noise analysis of harmonic oscillators

Federico Pepe





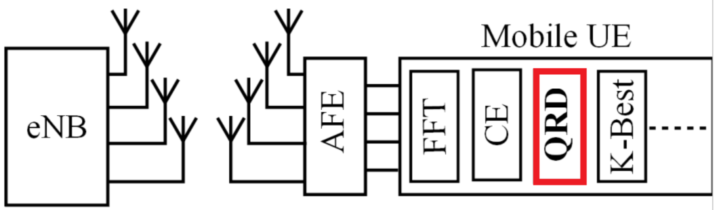
$$\mathcal{L}_{tot} = 10\log_{10}\left[2k_B T\frac{(1+\gamma)\omega_0^2}{\|D\vec{V}\|^2}\left|\frac{1}{\delta\lambda_1}\right|^2 L\vec{V}_1^{\,\mathrm{T}}\cdot \mathrm{Re}\left(\mathbf{Y}\right)\cdot L\vec{V}_1^{\,*}\right]$$

General phase noise equation

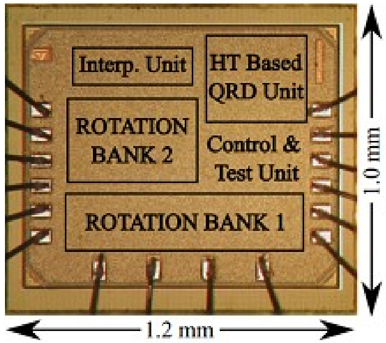
TCAS-I 2017

Adaptive QR Matrix Decomposition for LTE-A MIMO

Rakesh Gangarajaiah

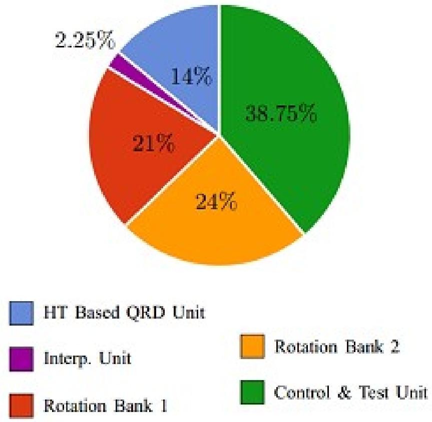


A typical LTE-A MIMO system with a QRD unit

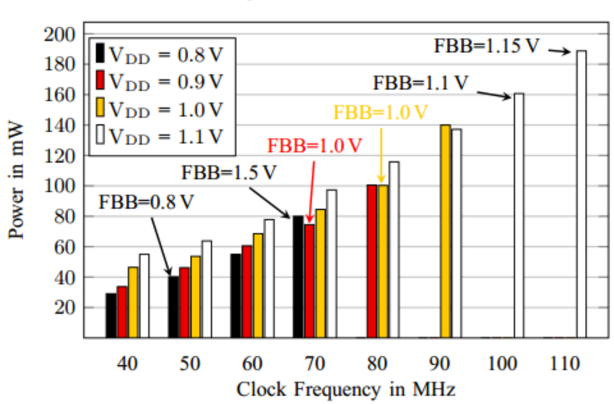


Max Freq. : 110 MHz
Max Power : 190 mW

Chip microphotograph



Area Breakdown



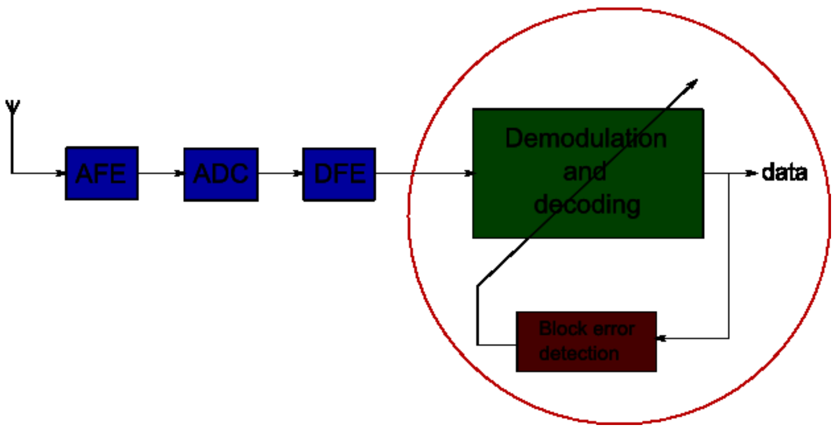
STM 28nm UTBB FD-SOI CMOS
with forward body bias (FBB)

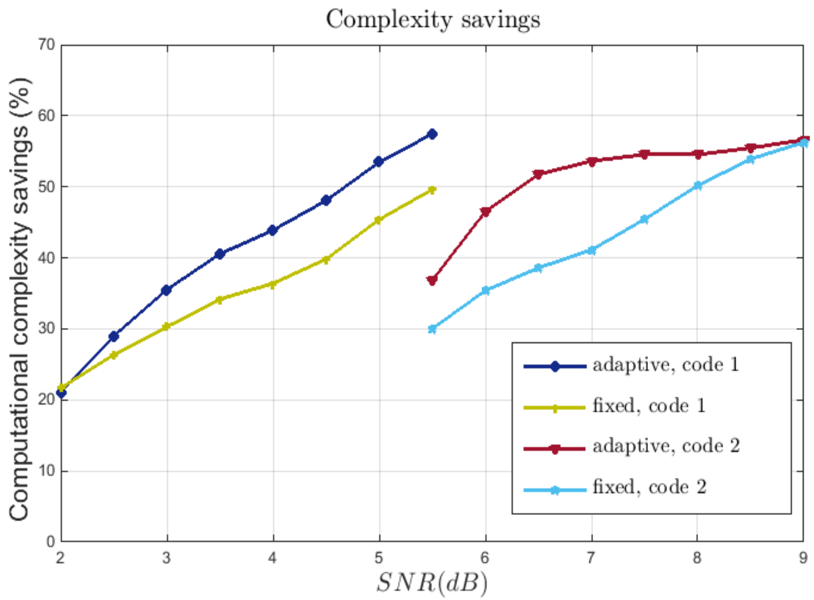
unpublished

Muris Sarajlić

unable LDPC Decoder Algorithm

LDPC = low-density parity-check





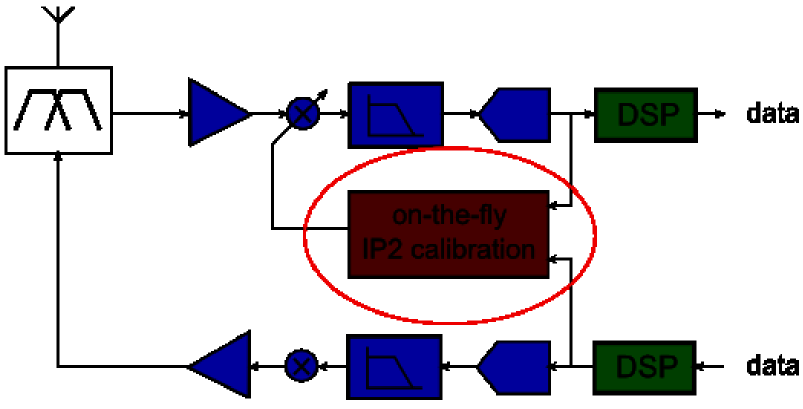
5 – 12 % additional complexity savings with adaptation to channel conditions

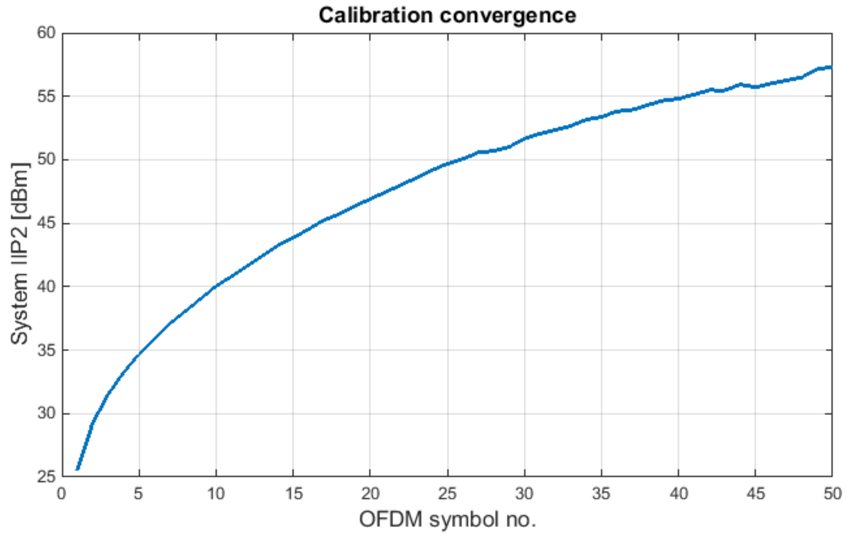
PIMRC 2014
PIMRC 2015

Muris Sarajlić

IP2 Improvement

On-the-fly algorithm for IP2 calibration in frequency mixer





Ongoing work: comparison of calibration vs compensation in digital baseband

unpublished

Michal Stala

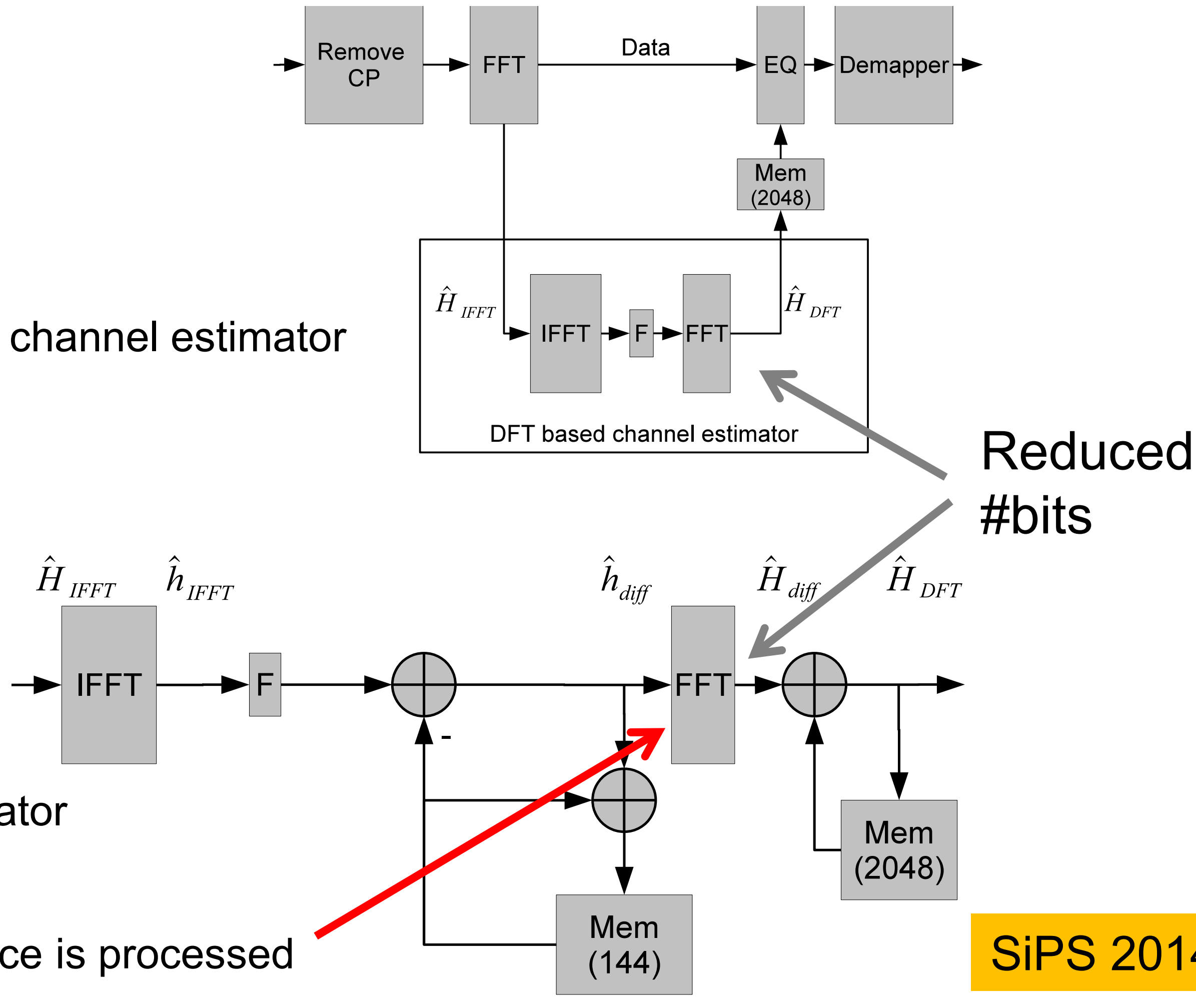
Swedish Foundation for Strategic Research

DFT-Based Channel Estimators for OFDM

original DFT channel estimator

new DFT channel estimator

only the difference is processed

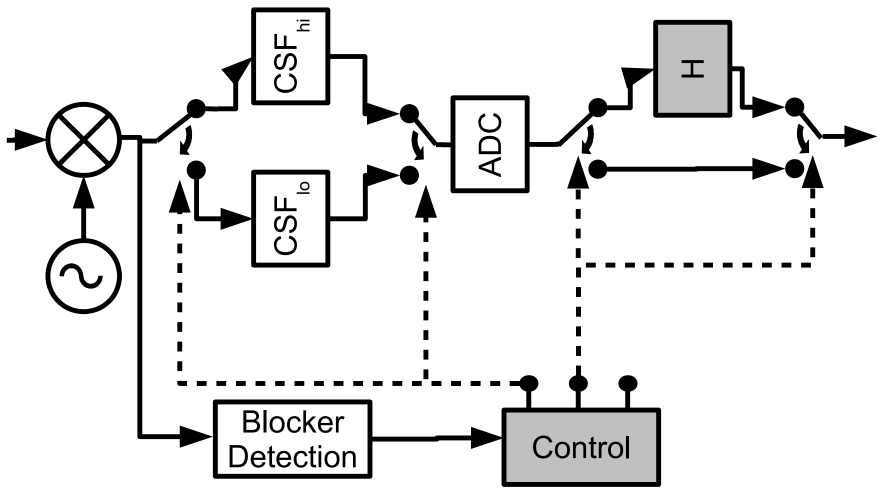


SiPS 2014

Michal Stala

SF Reconfiguration in Analog BB

Two CSFs: high-performance and low-performance



Block H (digital) compensates the phase distortion occurring when switching between the two CSFs

unpublished

Swedish Foundation for Strategic Research

Michal Stala

Company spin-off: MISTBASE

- MISTBASE founded in June 2015 by:
  - Michal Stala (DARE PhD Student)
  - Magnus Midholt
  - Lund University Innovation Systems (LUIS)
- Modem development for cellular IoT – NB-IoT
- LTH/EIT collaboration through internships and Master’s theses
- Currently:
  - 10 employees
  - 6 Master’s thesis students
- Partners: ARM and NextG-Com (more coming soon!)

Conclusions

DARE has produced a large amount of excellent results