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# *A 26GHz 22.2dBm Variable Gain Power Amplifier in 28nm FD-SOI CMOS for 5G Antenna Arrays*

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# Presentation Outline

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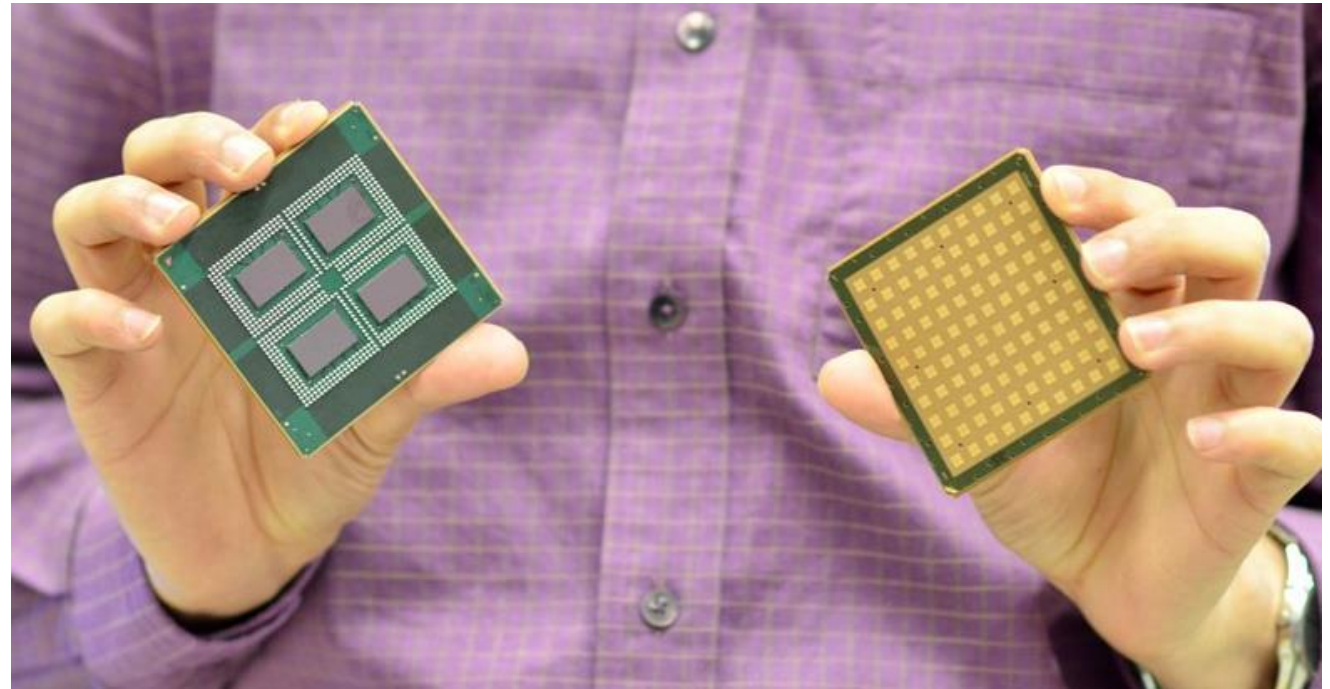


- Motivation and Scope
- Architecture
- Design
- Simulation and measurement results
- Conclusions

# Motivation and Scope

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- Targeting 5G mmW base station
- Large antenna array
- High integration
  - Not possible with external PAs
  - Many transceivers per chip
  - Including digital baseband
- State of the art CMOS



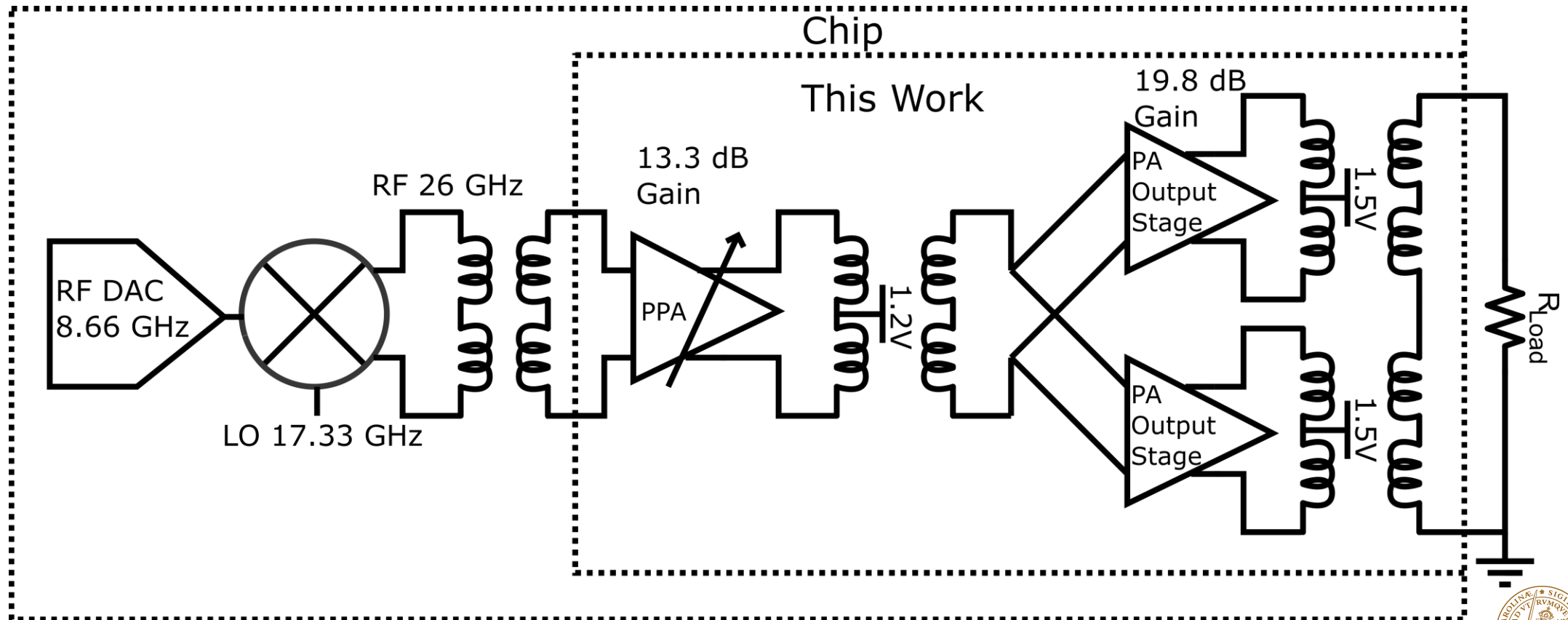
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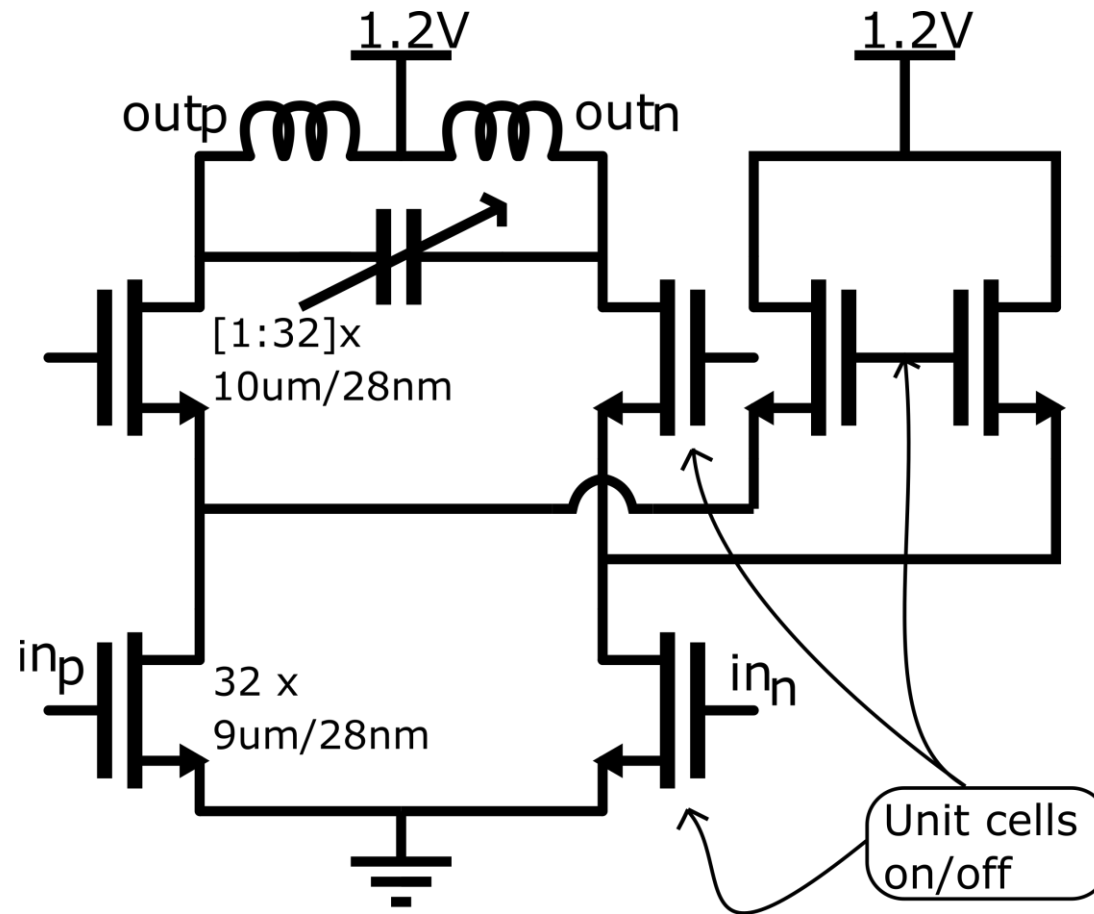
- 5G mmW PA for Antenna Array System (AAS)
  - High output power
    - » For coverage at mmW
  - 28 nm FD-SOI CMOS process
  - High Power Added Efficiency (PAE)
  - 10-year reliability



# PA Architecture –Part of a fully integrated transmitter

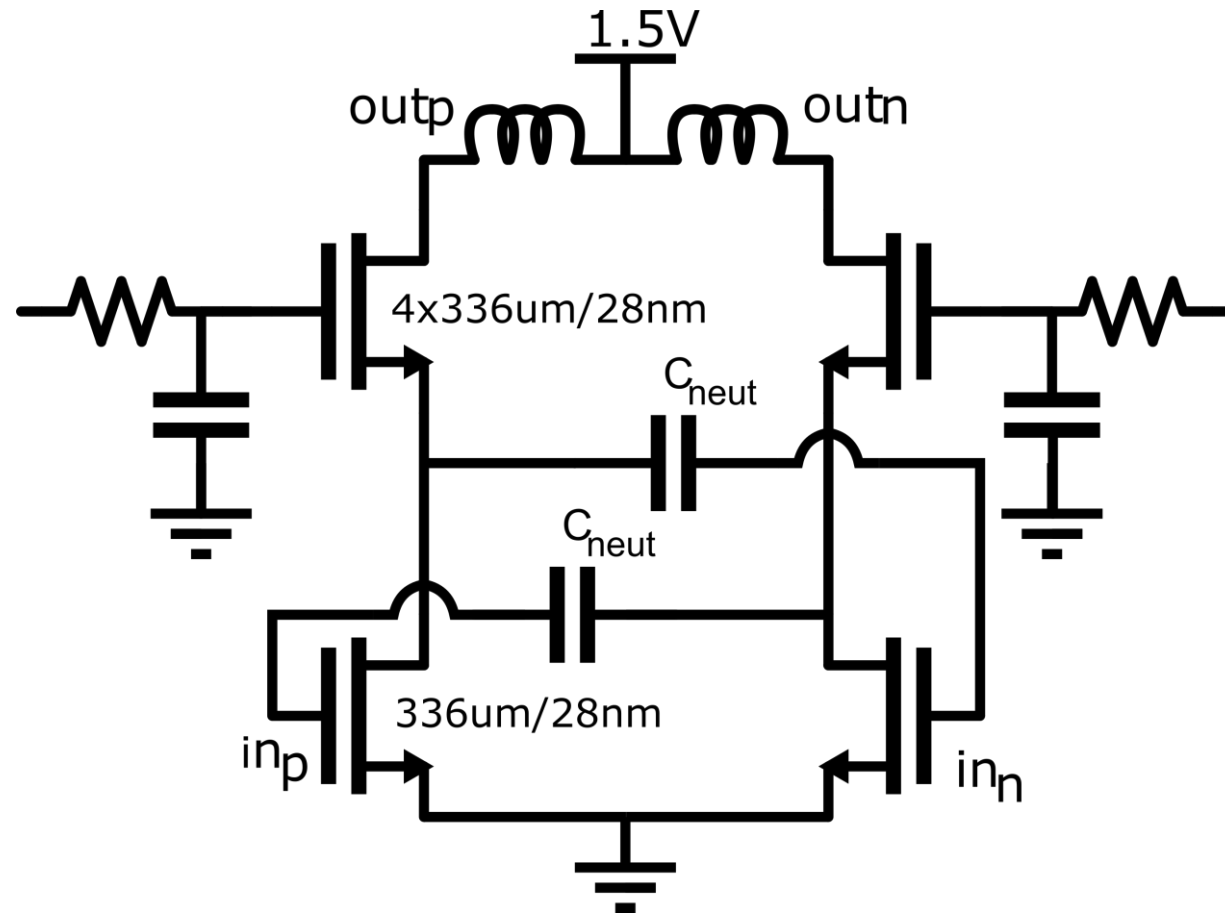


# PPA Design



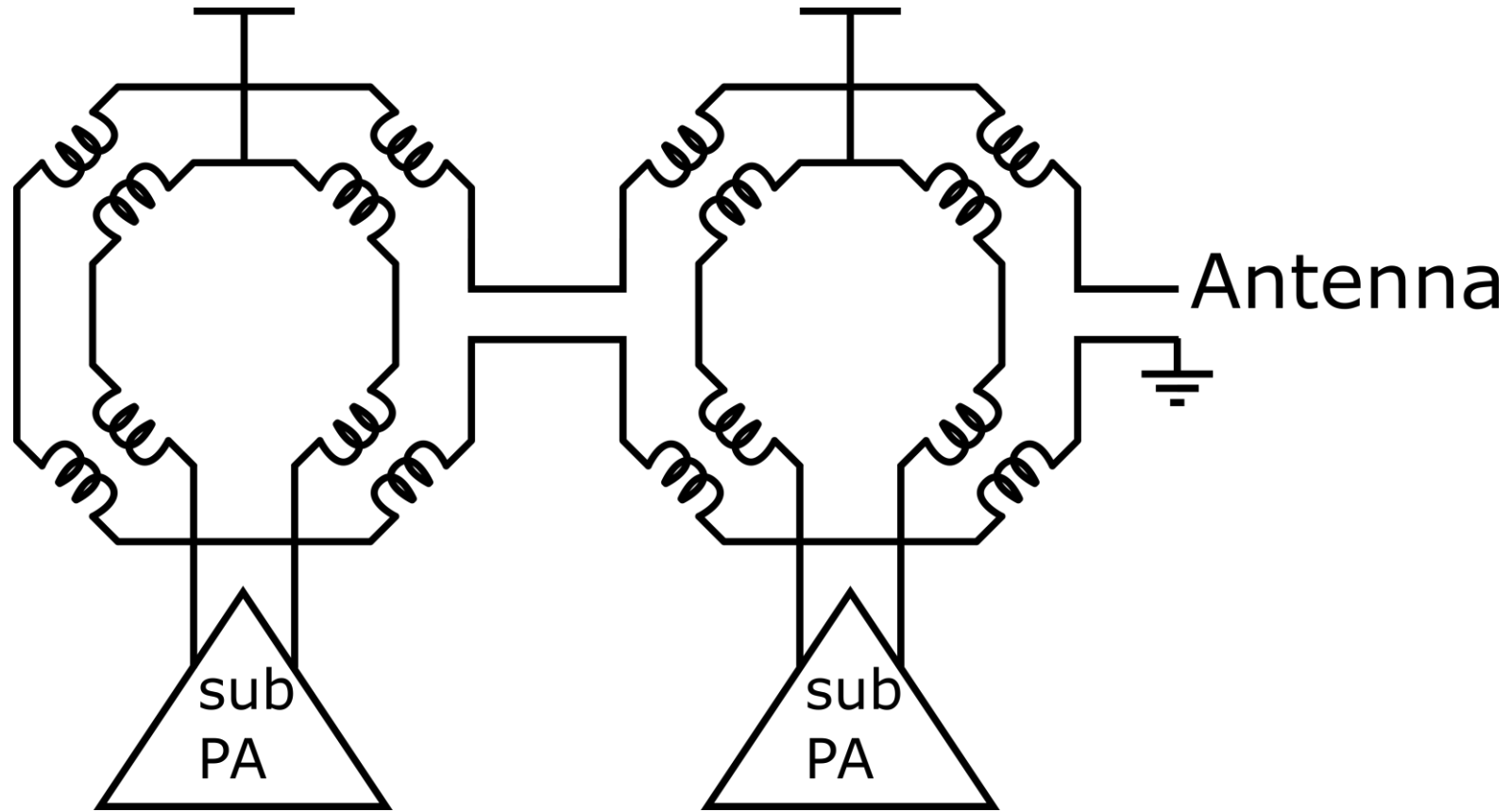
# Sub-PA Design

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# Output Combiner Design

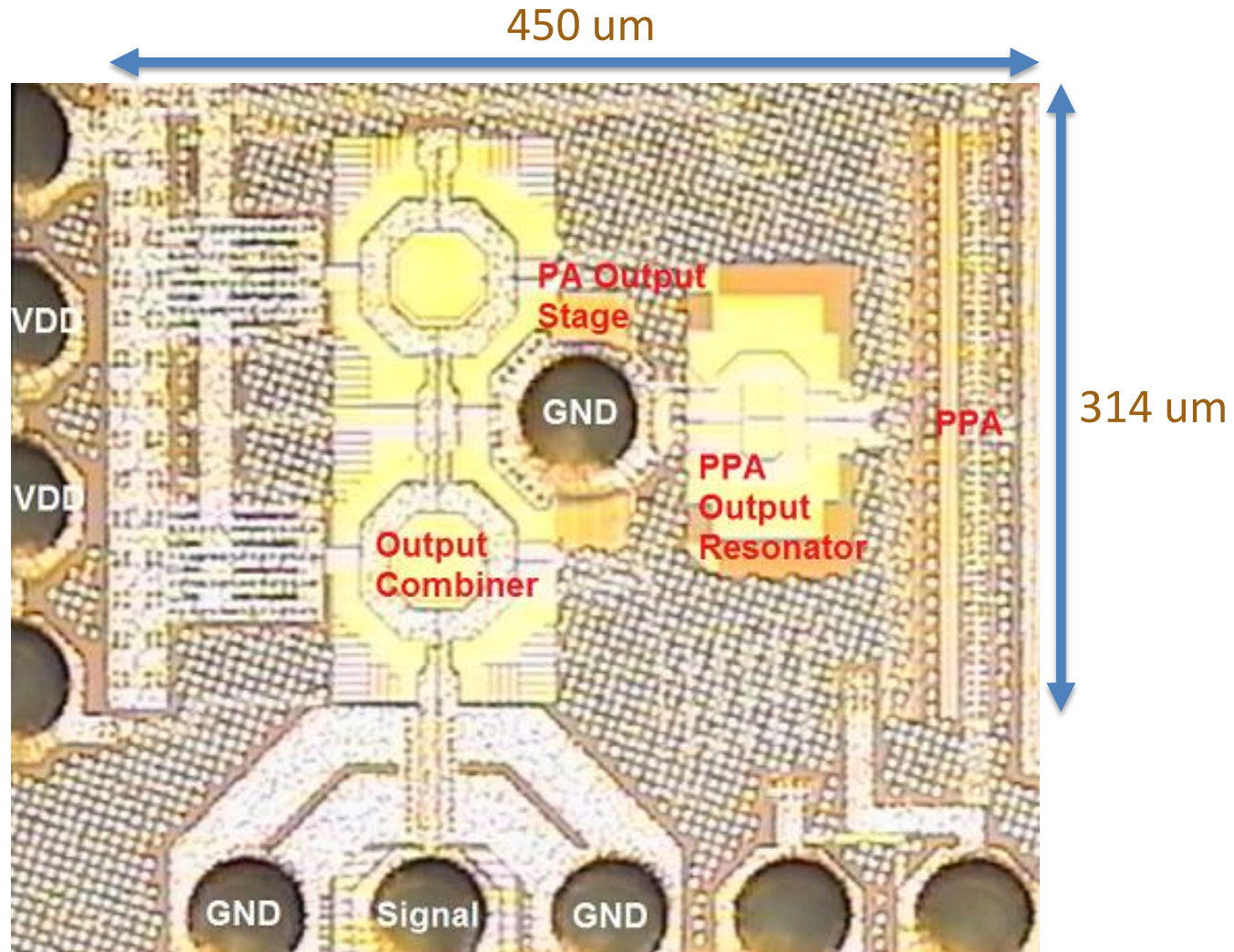
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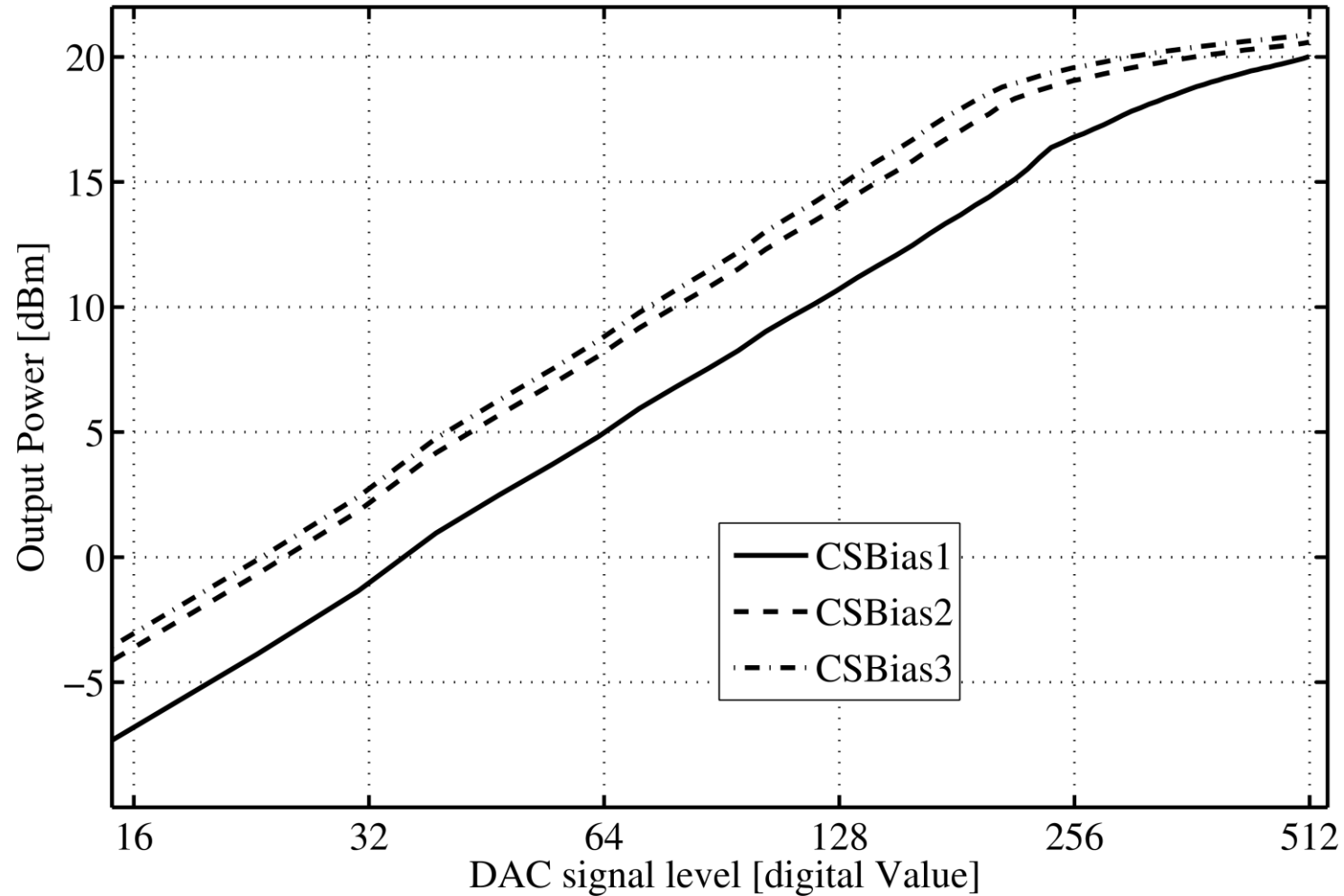


# Chip Photo

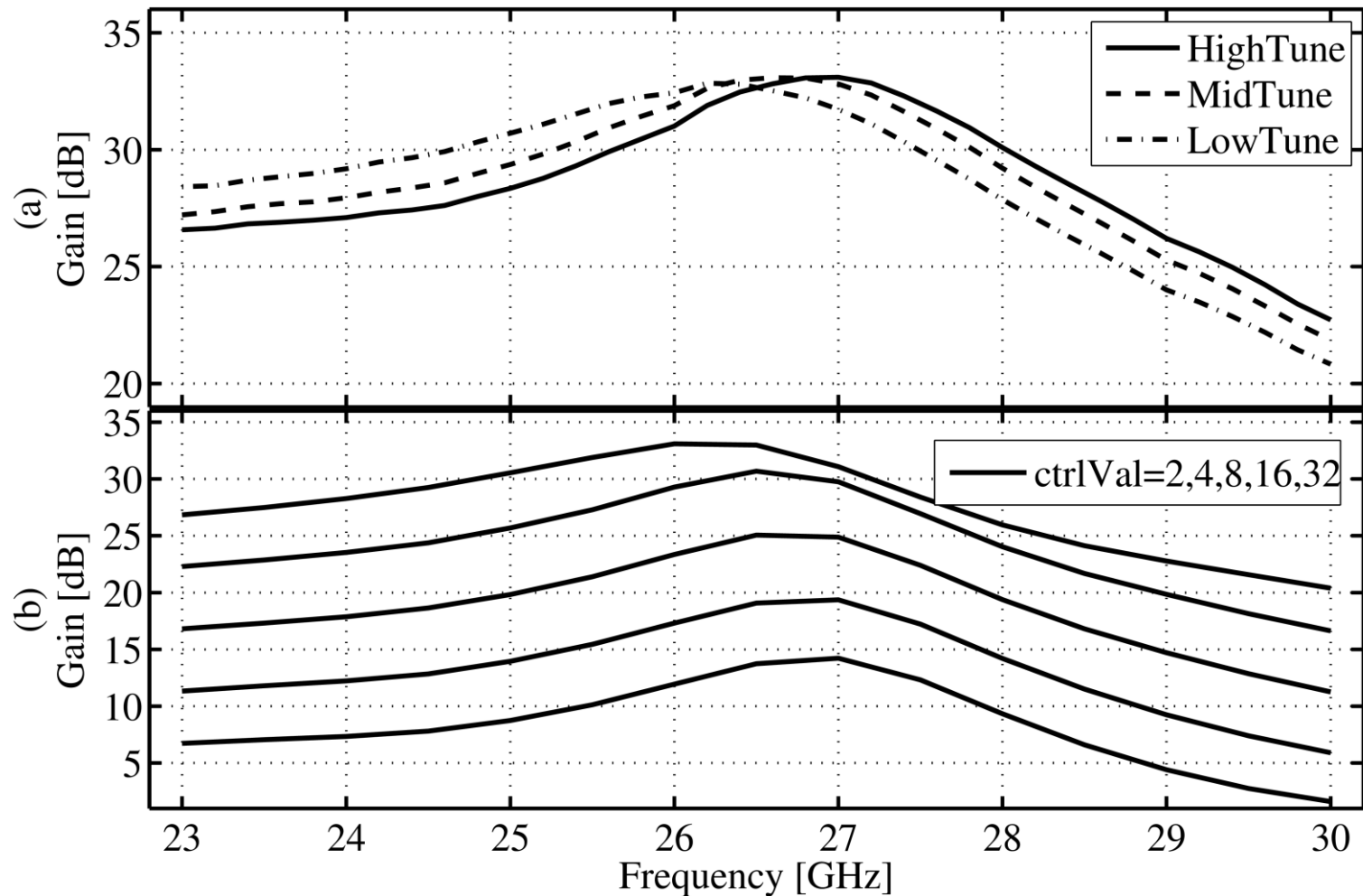
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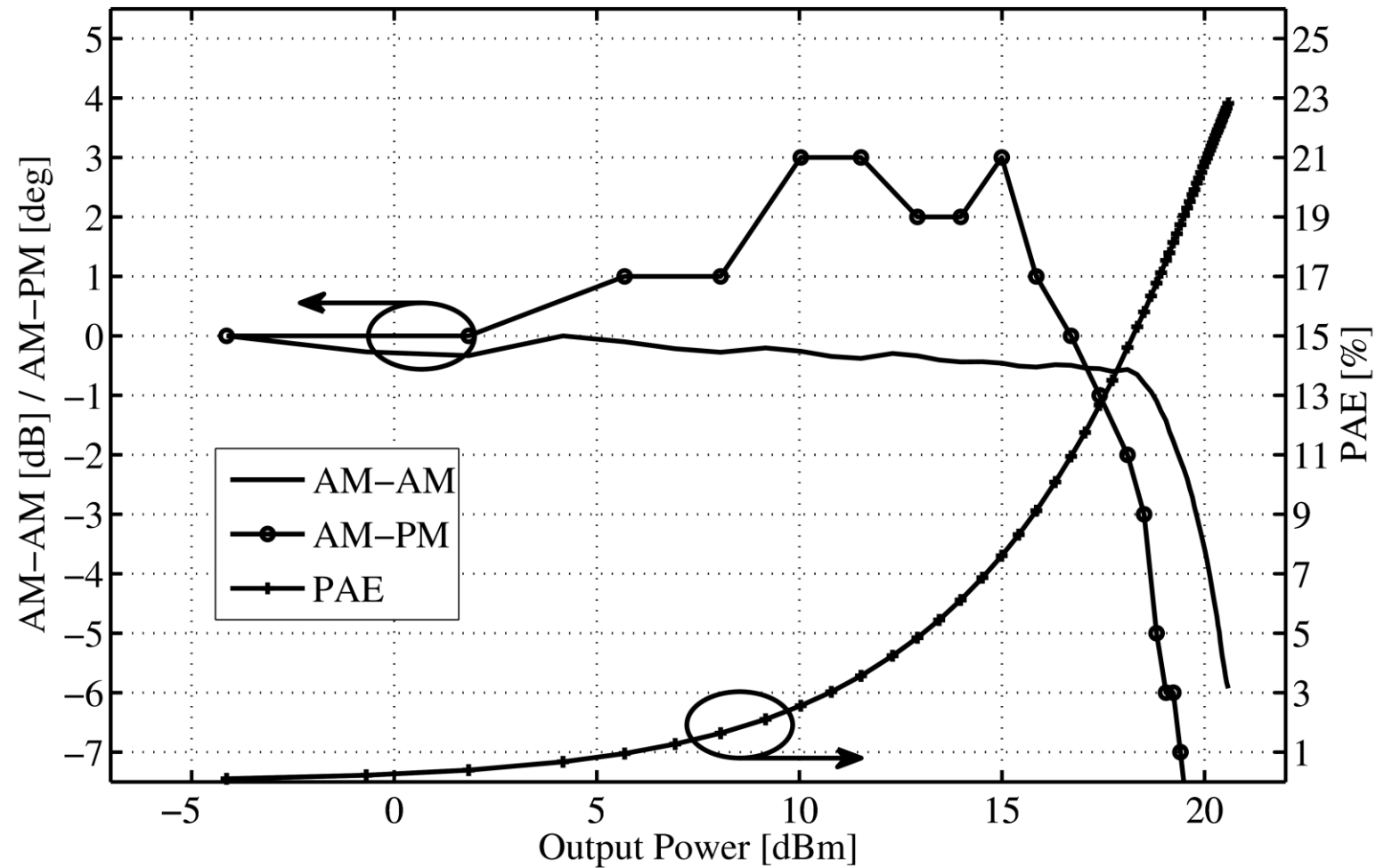
# Pout vs DAC value



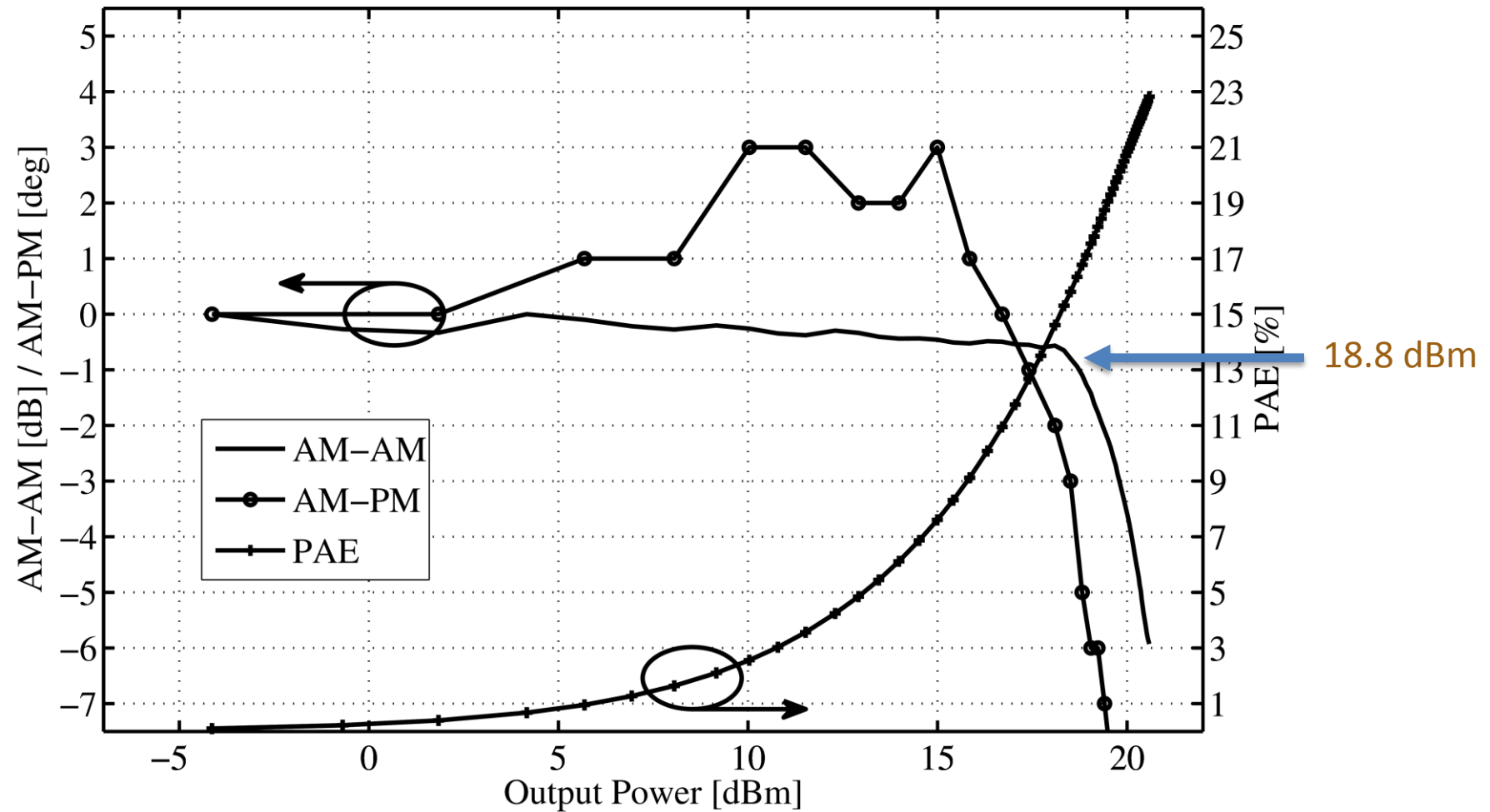
# Small Signal Measurement



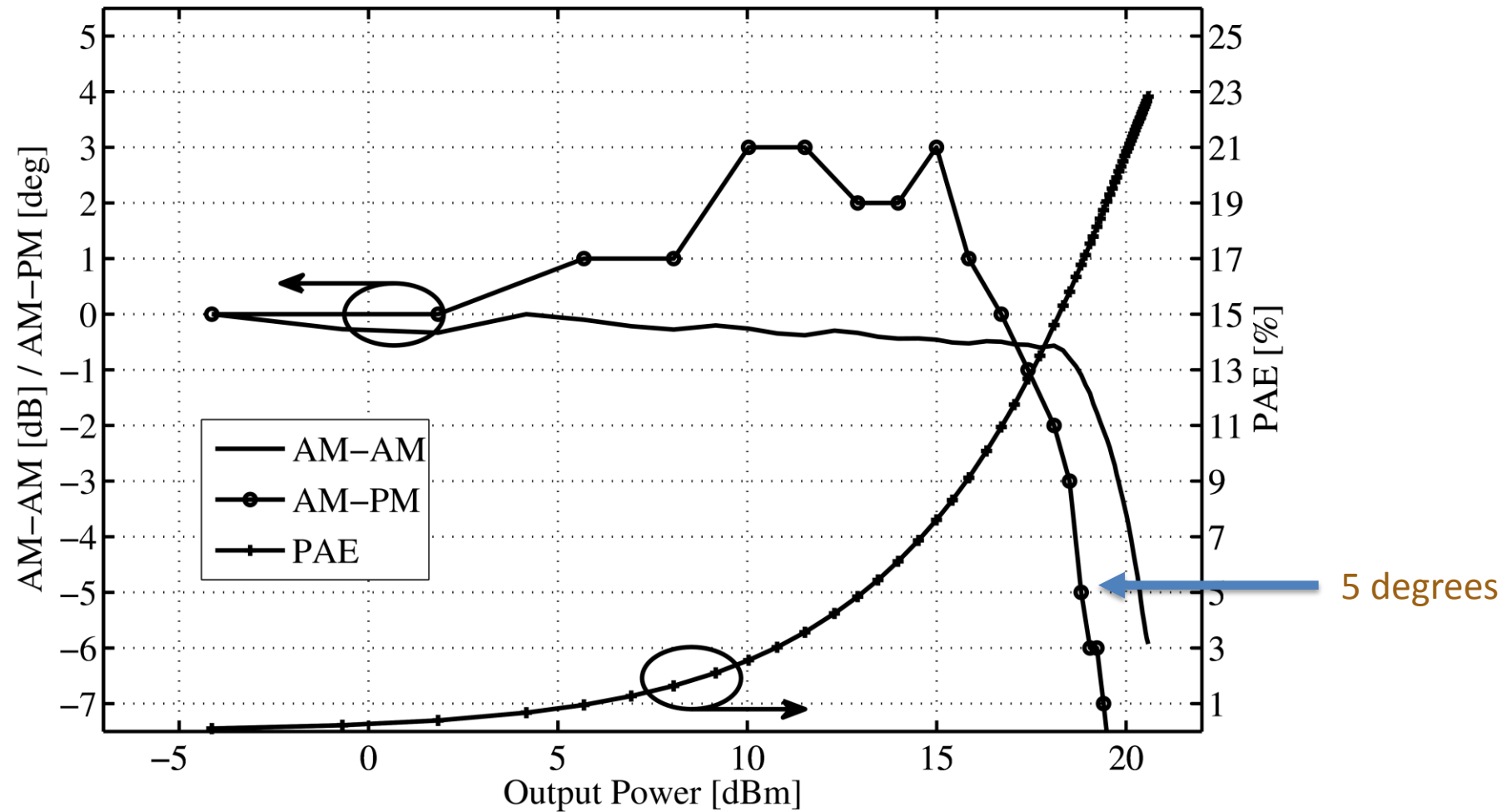
# AM-AM, AM-PM and PAE



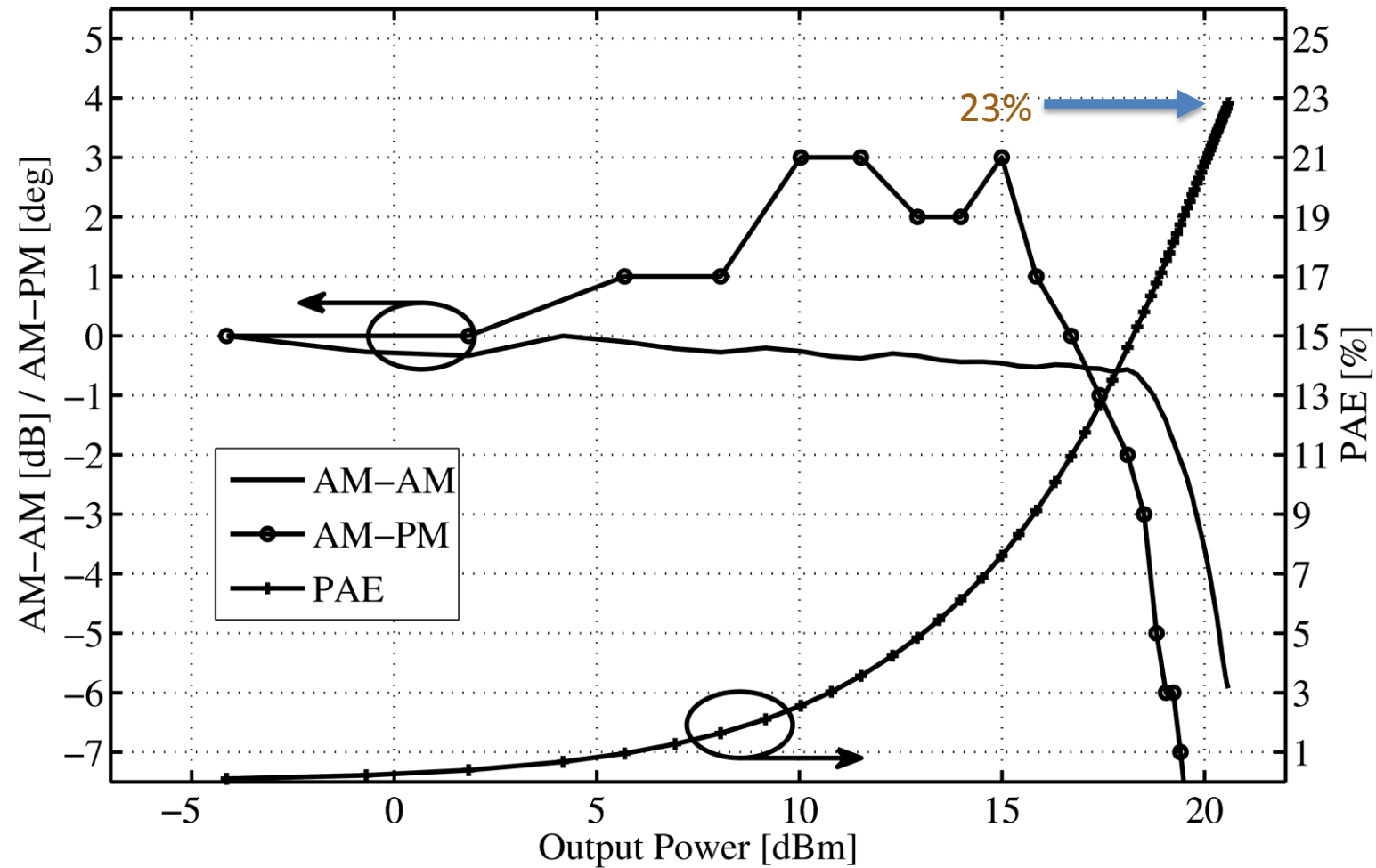
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# Performance Summary and Comparison

Parameter	This Work		RFIC'17 [3]	RFIC'17 [4]	ISSCC'16 [5]		IMS'16 [6]	
Tech. [nm]	28 SOI CMOS		28 Bulk CMOS	28 Bulk CMOS	28 Bulk CMOS		28 Bulk CMOS	
Freq. [GHz]	26		27	32	30		28	
Pwr.Comb.	2		2	2	1		1	
Gain Control	5 bits, 19dB		None	None	None		None	
No. of Stages	2		2	2	2		1	
Vdd [V]	1.5	1.8	1	1	1	1.15	1.1	2.2
$P_{sat}$ [dBm]	20.6	22.2	18.1	19.8	14	15.3	14.8	19.8
$P_{1dB}$ [dBm]	18.8	20.7	16.8	16	13.2	14.3	14.0	18.6
$PAE_{max}$ [%]	22.6 <sup>(1)</sup>	21.3 <sup>(1)</sup>	41.5	21	35.5	36.6	36.5	43.3
$PAE_{1dB}$ [%]	16.6 <sup>(1)</sup>	14.6 <sup>(1)</sup>	37.6	12.8	34.3	35.8	35.2	41.4
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Gain [dB]	33.1 <sup>(3)</sup>	33.9 <sup>(3)</sup>	20.5	22	15.7	16.3	10.0	13.6
Area [ $mm^2$ ]	0.144		0.361	0.59	0.16		0.28	

(1) Not including PPA power consumption.

(2) Including PPA power consumption.

(3) Simulated value since input signal is generated internally. Also used for calculating PAE values.





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  - Smallest die area





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