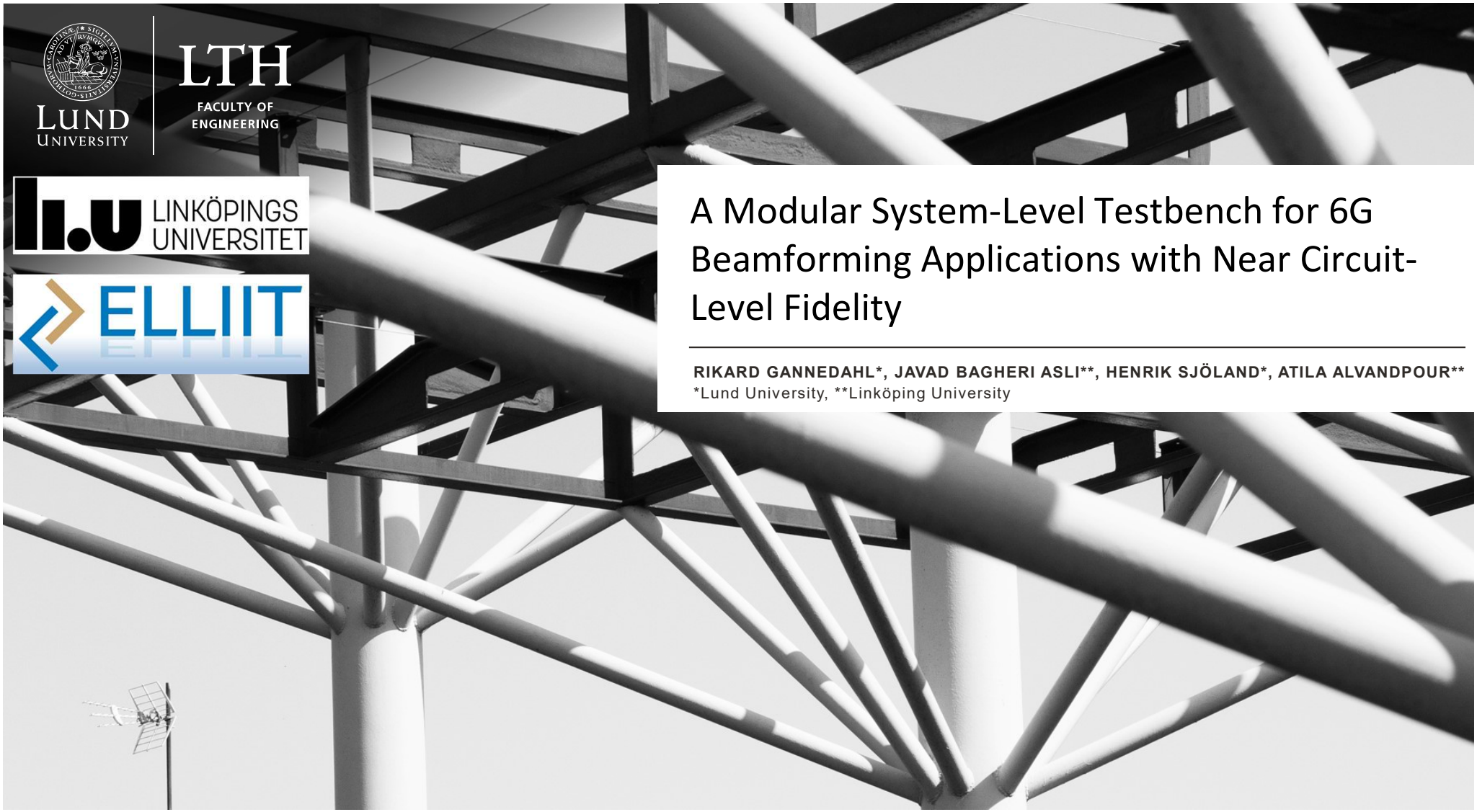

A Modular System-Level Testbench for 6G Beamforming Applications with Near Circuit-Level Fidelity

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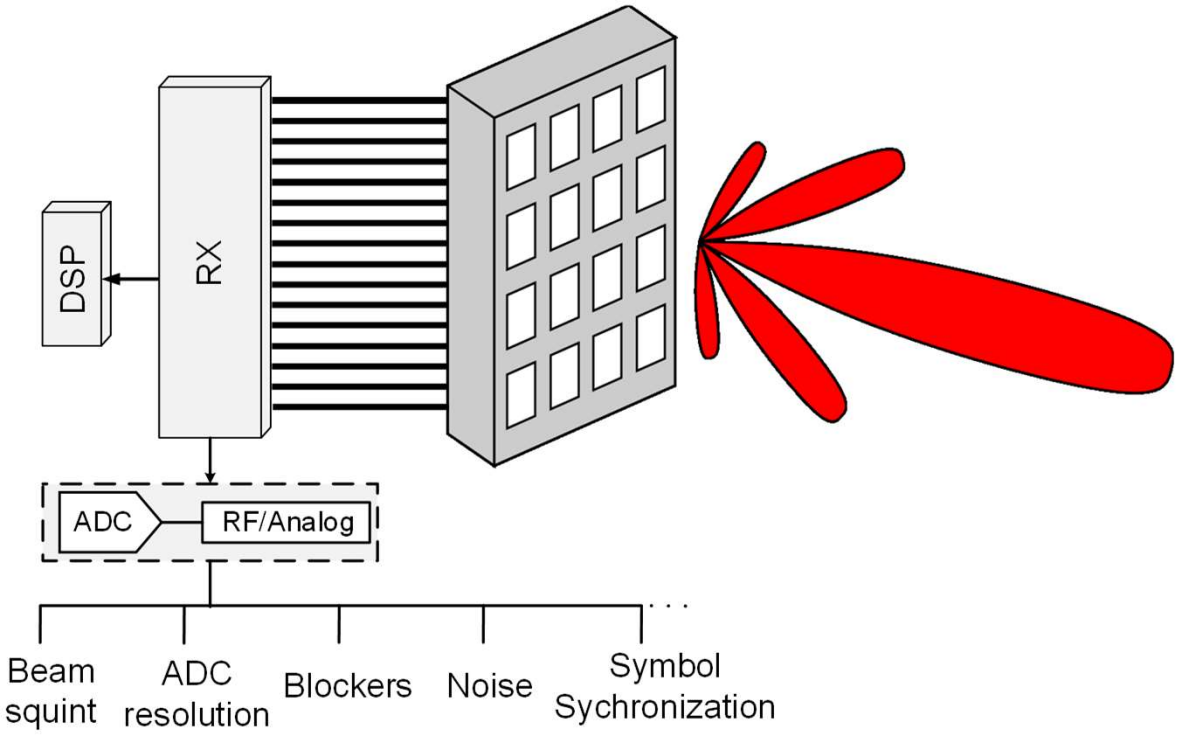
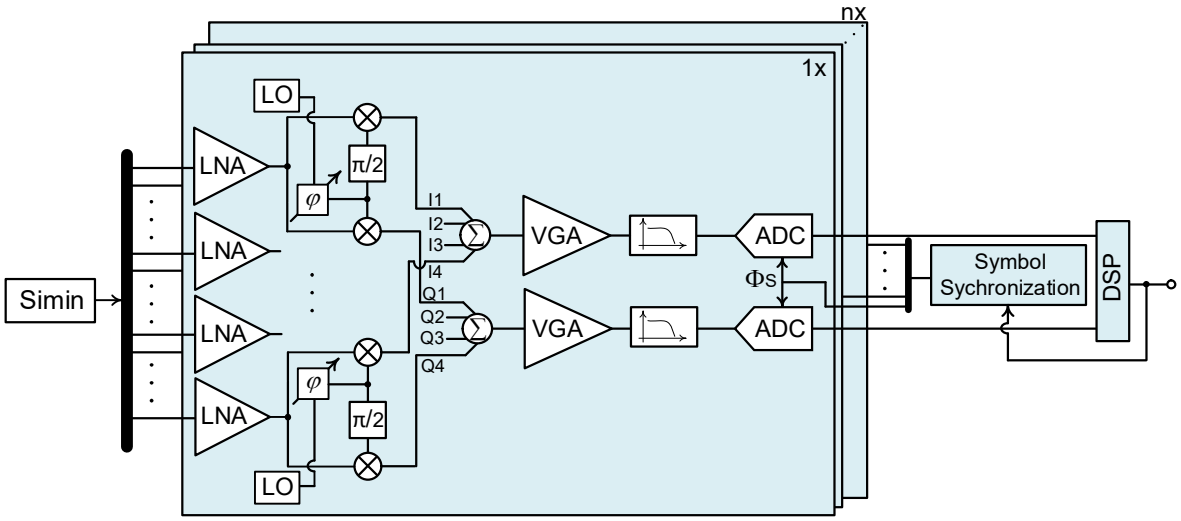
Background & Motivation

- 6G is around the corner!
- Beamforming using massive antenna arrays are required
  - Lots of degrees of freedom
- System analysis using black box modelling
  - Inaccurate simulations
  - Limited insight for circuit designers
- A user-friendly and accurate testbench is needed



MATLAB/Simulink Testbench

- MATLAB script generates signals and parameters
- Receiver implemented in Simulink
  - *RF blockset* for analog frontend
  - Pipeline ADC
- Sent back to MATLAB for post-processing



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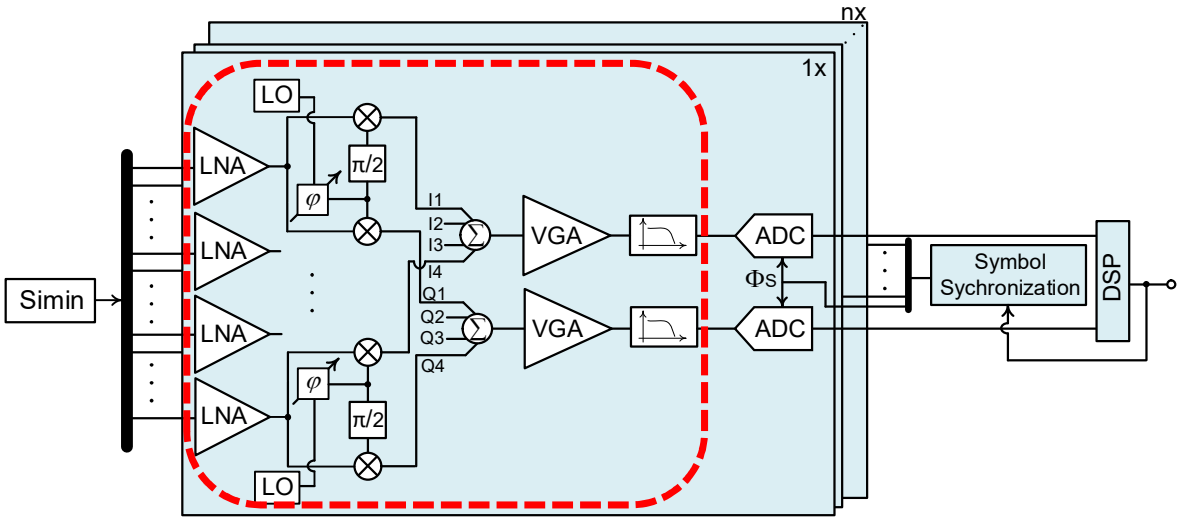

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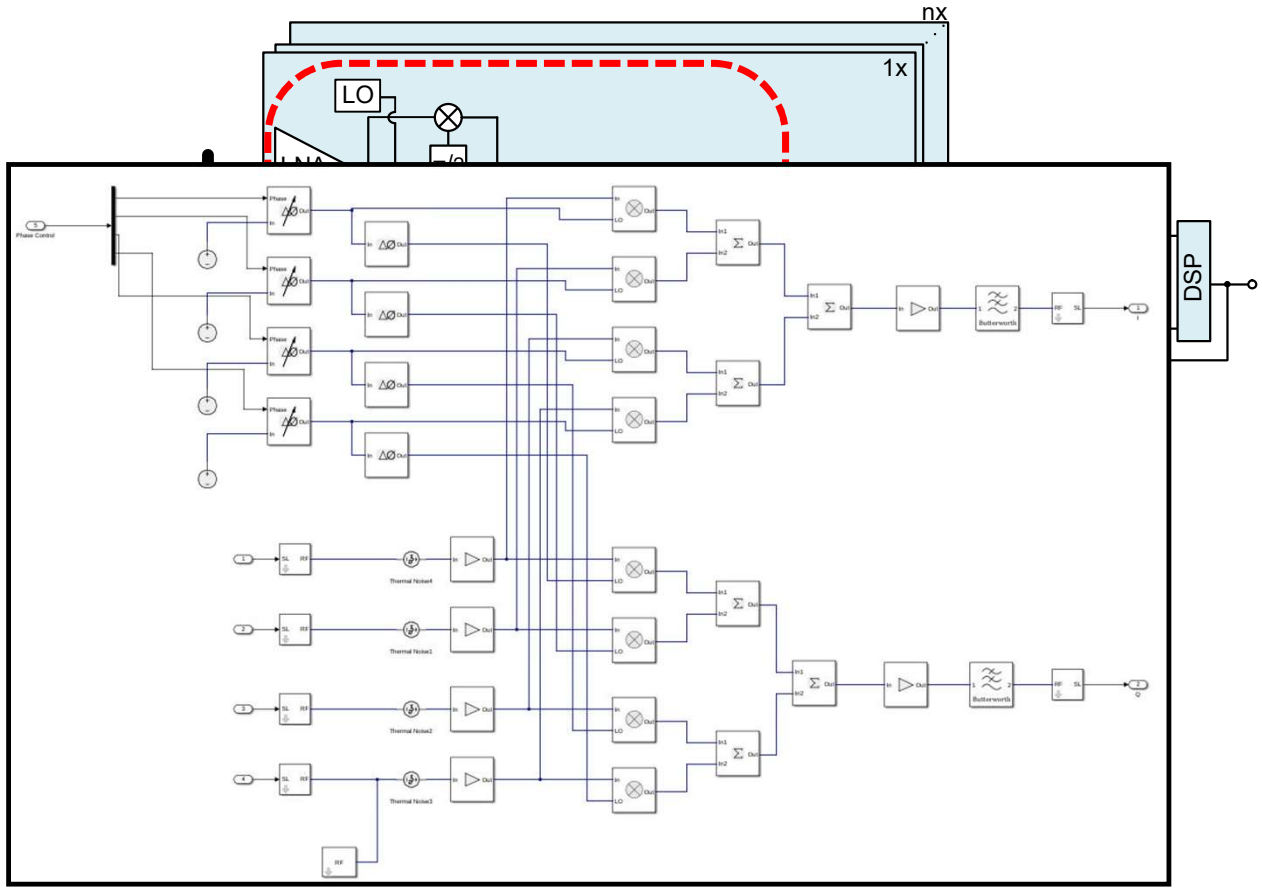

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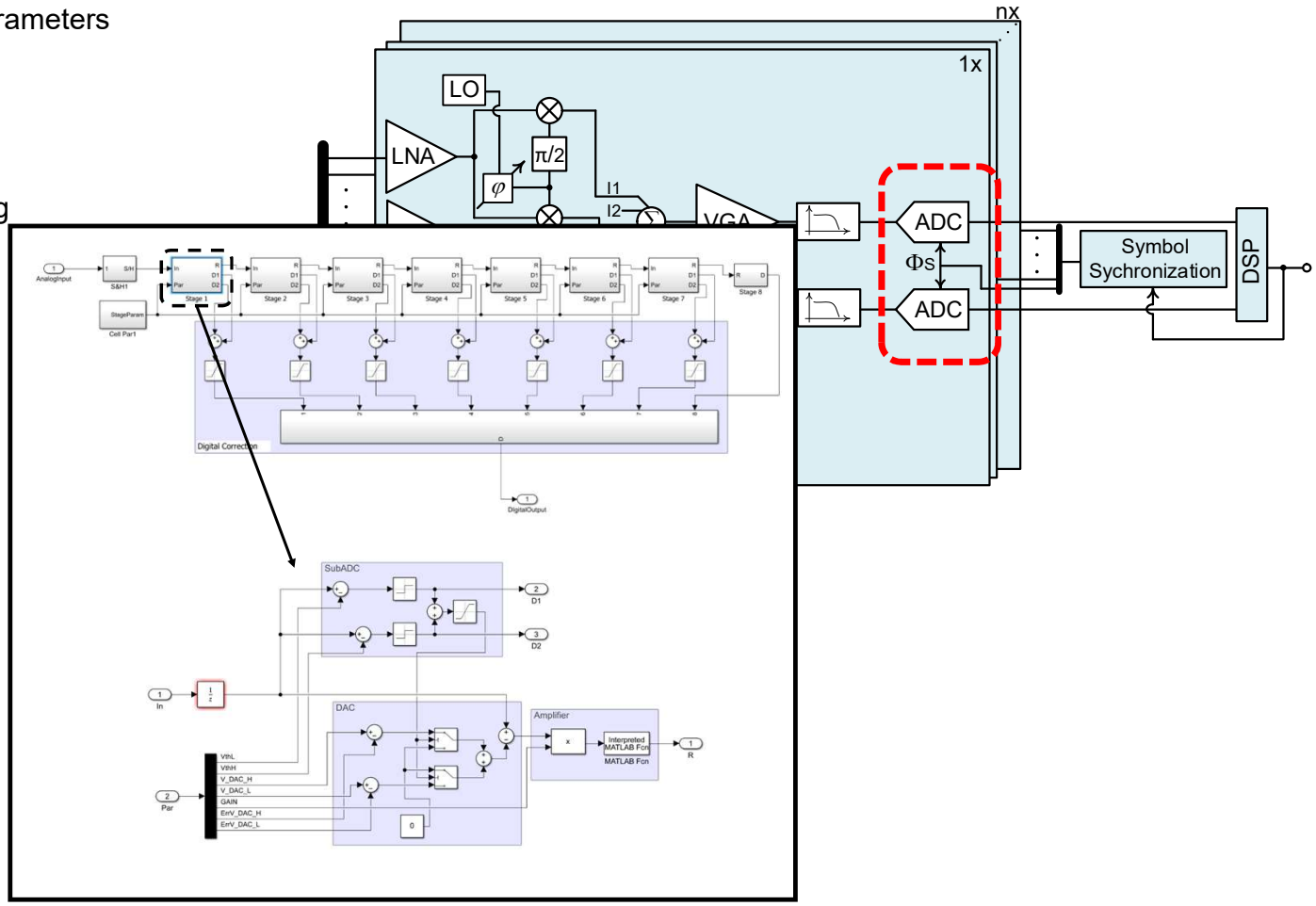
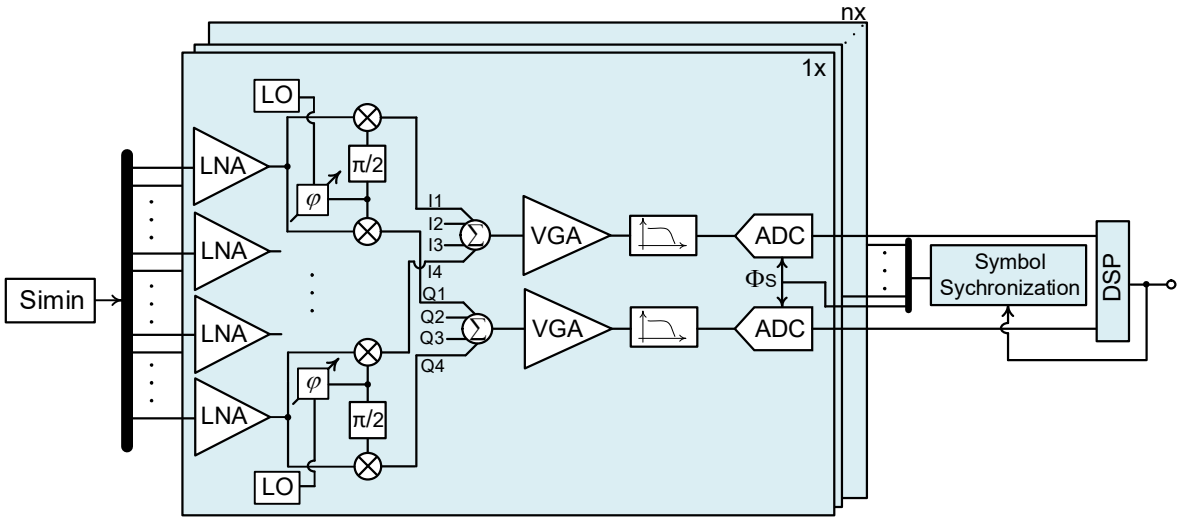
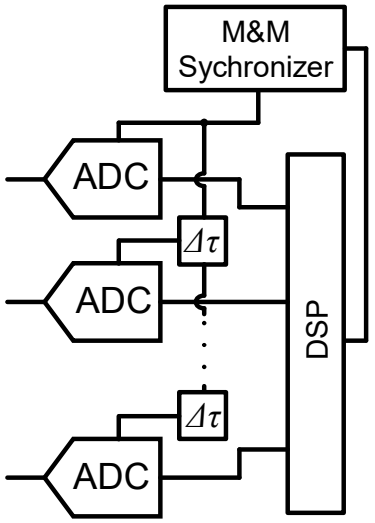


Simulation results

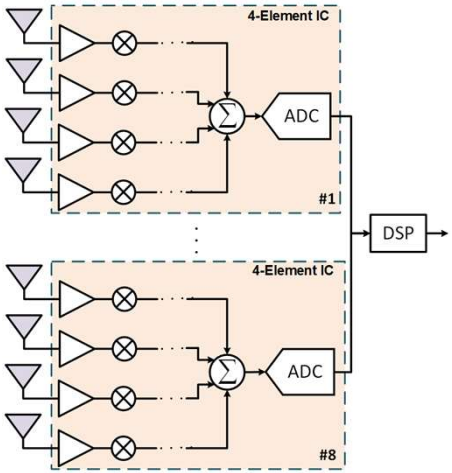
- 4-element IC tile
- 10 GHz bandwidth, 16-QAM, 100 GHz carrier
- 1 complex sample per symbol, symbol synchronizer
- Disclaimer: Only specific scenarios

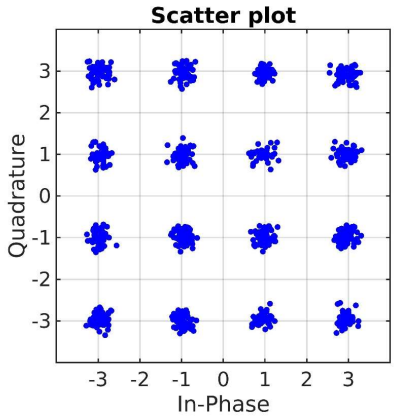


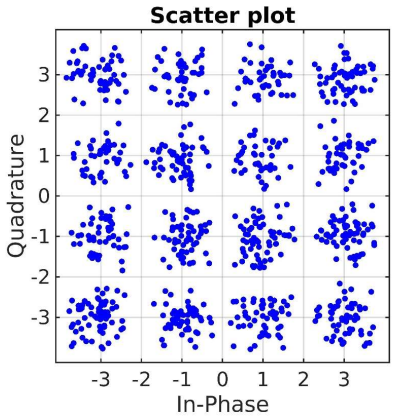


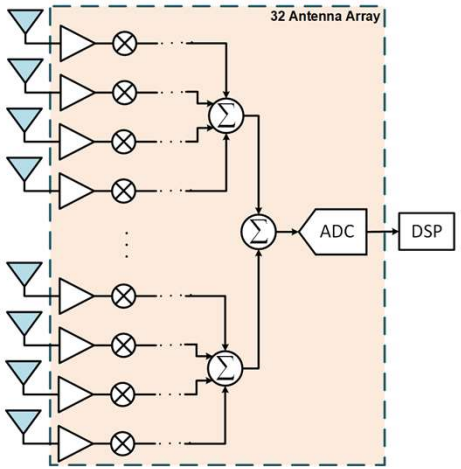
Beam squint

- Beam squint due to phase shifters
- Worse for large arrays
- Solved by using small sub-arrays and digital delays



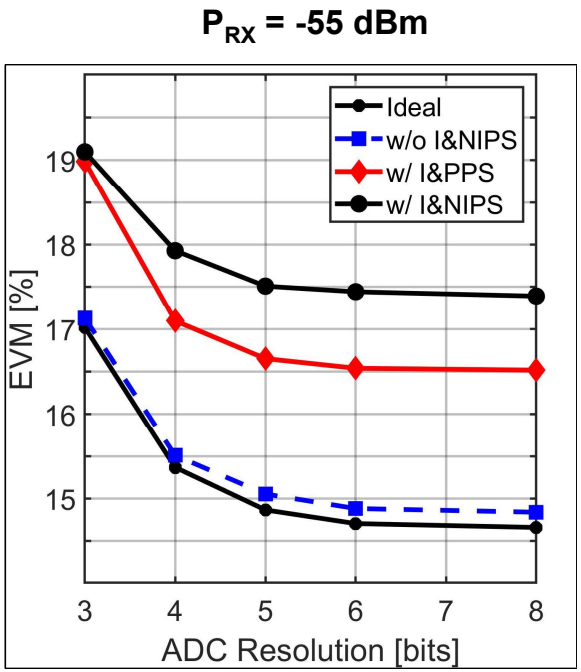






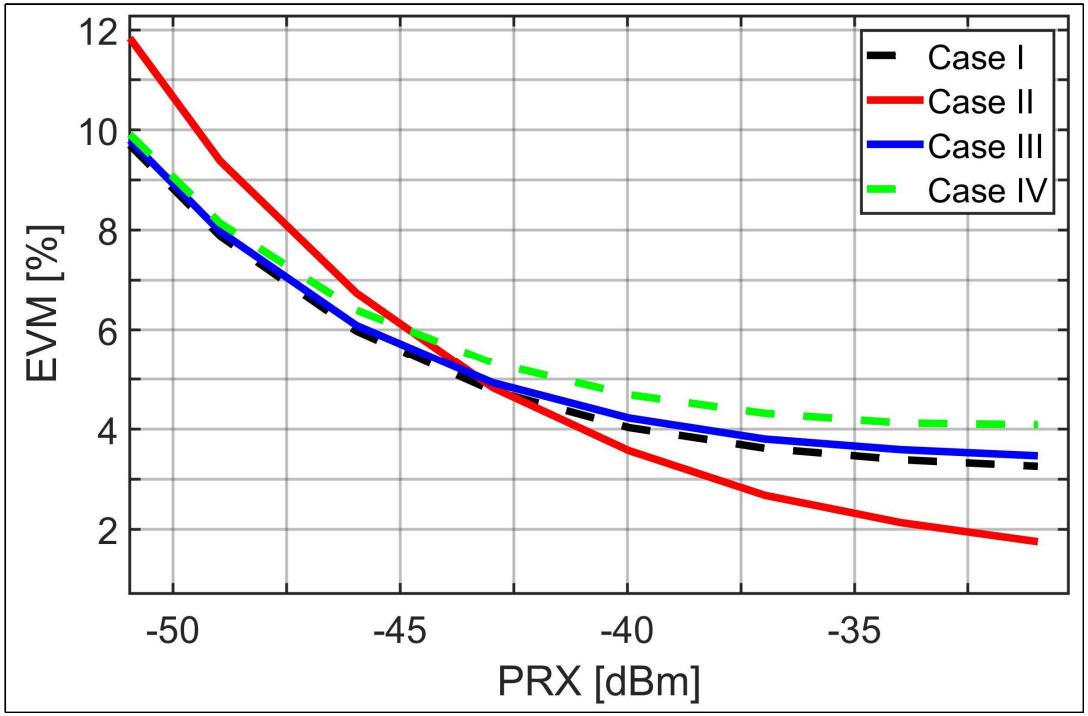
EVM vs ADC resolution

- ADC resolution is a critical parameter
- Impact of interferer?
- Six 4-element tiles
- Interferer 20 dB stronger than desired
- Desired AoA 15º, interferer AoA -20º
- Non-ideal PS: 5 bits, 2º rms error



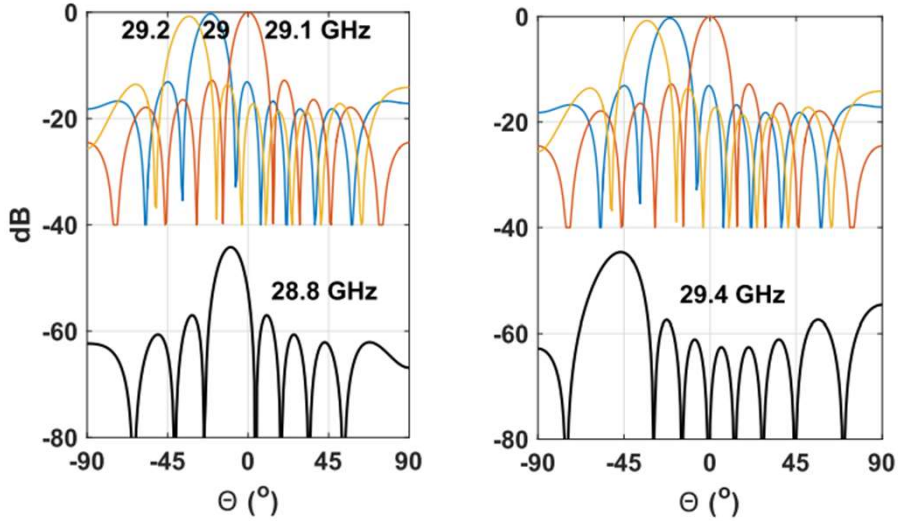
EVM vs received power

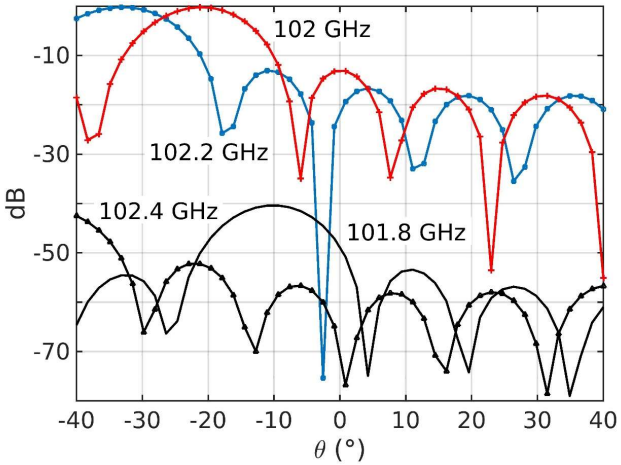
- 8-bit ADC, no interferer
- Four cases:
  - Case I: Only thermal noise, Butterworth
  - Case II: Only thermal noise, Bessel
  - Case III: Uncorrelated phase noise
  - Case IV: Correlated phase noise



Non-linearity vs interfering angle

- Recreated the results from other work [1]
  - Two interferers, AoA: -21º and -33º
  - Received power: -37 dBm
  - Total IIP3 of receiver: -17 dBm





This work

[1] B. Rupakula and G. M. Rebeiz, “Third-Order Intermodulation Effects and System Sensitivity Degradation in Receive-Mode 5G Phased Arrays in the Presence of Multiple Interferers“, IEEE TMTT, 2018

What’s next?

- More general results
- Power estimations
- More focus on ADC imperfections
- Testbench will be made available once journal paper accepted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